

TIP32C

Power transistor

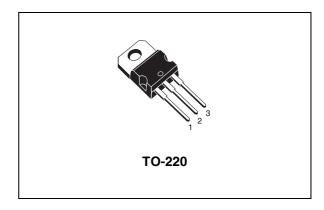
Applications

■ Linear and swithing industrial equipment

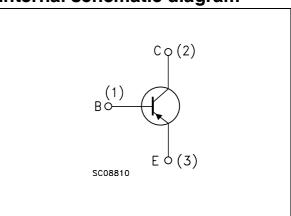
Description

The TIP32C is a silicon Epitaxial-base PNP power transistor in Jedec TO-220 plastic package. It is intented for use in medium power linear and switching applications.

The complementary NPN type is TIP31C.



Internal schematic diagram



Order codes

Part number	Marking	Package	Packing
TIP32C	TIP32C	TO-220	Tube

1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CBO}	Collector-base voltage (I _E = 0)	-100	V
V _{CEO}	Collector-emitter voltage (I _B = 0)	-100	V
V _{EBO}	Emitte-base voltage (I _C = 0)	-5	V
I _C	Collector current	-3	Α
I _{CM}	Collector peak current (t _P < 5ms)	-5	Α
Ι _Β	Base current	-1	Α
P _{TOT}	Total dissipation at T _{case} = 25°C T _{amb} = 25°C	40 2	W W
T _{stg}	Storage temperature	-65 to 150	°C
TJ	Max. operating junction temperature	150	°C

2 Electrical characteristics

 $(T_{case} = 25^{\circ}C; unless otherwise specified)$

Table 2. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{CEO}	Collector cut-off current (I _B = 0)	V _{CB} =-60V			-0.3	mA
I _{CES}	Collector cut-off current (V _{BE} = 0)	V _{CB} =-100V			-0.2	mA
I _{EBO}	Emitter cut-off current (I _C = 0)	V _{EB} =-5V			-1	mA
V _{CEO(sus}	Collector-emitter sustaining voltage (I _B = 0)	I _C = -30mA	-100			V
V _{CE(sat)} ⁽¹⁾	Collector-emitter saturation voltage	$I_C = -3A$ $I_B = 375mA$			-1.2	V
V _{BE(on)} ⁽¹⁾	Base-emitter voltage	$I_C = -3A$ $V_{CE} = -4V$			-1.8	٧
h _{FE} ⁽¹⁾	DC current gain	$I_C = -1A$ $V_{CE} = -4V$ $I_C = -3A$ $V_{CE} = -4V$	25 10		50	

^{1.} Pulsed duration = 300 ms, duty cycle \geq 1.5%.

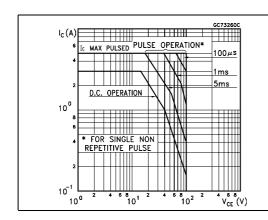
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Electrical characteristics TIP32C

2.1 Typical characteristic

Figure 1. Safe operating area

Figure 2. Derating Curves



Ptot (%)

100

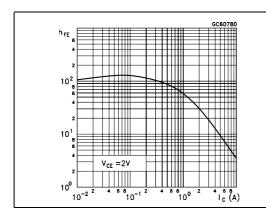
Ptot | Is/B |

50

0 50 100 T_C (°C)

Figure 3. DC current gain

Figure 4. Collector-emitter saturation voltage



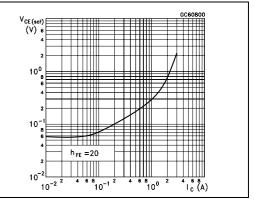
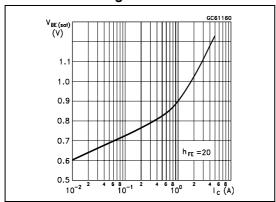


Figure 5. Base-emitter saturation voltage



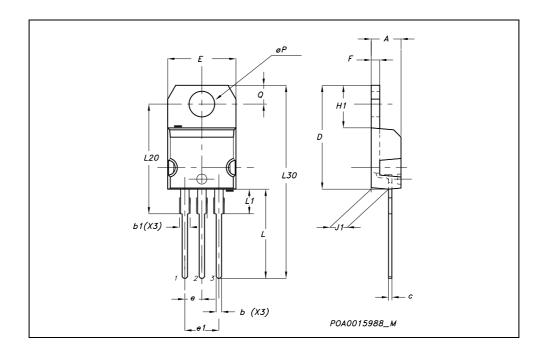
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3 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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DIM		mm.		inch		
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
Е	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øΡ	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TIP32C Revision History

4 Revision History

Table 3. Revision history

Date	Revision	Changes	
10-Oct-1999	1	Initial Release	
15-Nov-2006	2	The document has been reformatted	

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