

# FDP075N15A\_F102 / FDB075N15A

## N-Channel PowerTrench® MOSFET

150V, 130A, 7.5mΩ



### Features

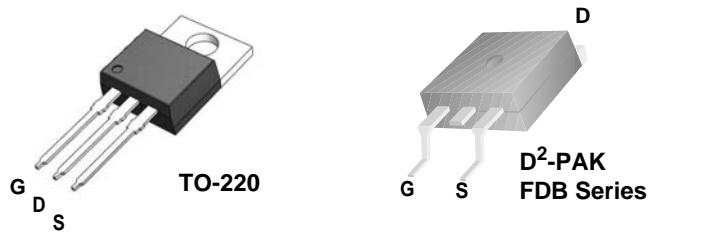
- $R_{DS(on)} = 6.25\text{m}\Omega$  (Typ.) @  $V_{GS} = 10\text{V}$ ,  $I_D = 100\text{A}$
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted\*

Symbol	Parameter		FDP075N15A_F102 FDB075N15A	Units
$V_{DSS}$	Drain to Source Voltage		150	V
$V_{GSS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	130	A
		-Continuous ( $T_C = 100^\circ\text{C}$ )	92	
$I_{DM}$	Drain Current	- Pulsed	(Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy		(Note 2)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$		(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	333	W
		- Derate above $25^\circ\text{C}$	2.22	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +175	°C
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

\*Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	FDP075N15A_F102 FDB075N15A	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max	62.5	
	Thermal Resistance, Junction to Ambient D2-PAK (1 in <sup>2</sup> pad of 2 oz copper), Max	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP075N15A	FDP075N15A_F102	TO-220	F102: Trimmed Leads	50

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB075N15A	FDB075N15A	D2-PAK	330mm	24mm	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	-	0.1	-	$\text{V}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 120\text{V}, T_C = 150^\circ\text{C}$	-	-	500	
$I_{\text{GSS}}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	$\mu\text{A}$

### On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 100\text{A}$	-	6.25	7.5	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 100\text{A}$	-	164	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5525	7350	pF
$C_{oss}$	Output Capacitance		-	516	685	pF
$C_{rss}$	Reverse Transfer Capacitance		-	21	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$	-	909	-	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V		-	77	100	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = 75\text{V}, I_D = 100\text{A}$ $V_{GS} = 10\text{V}$	-	26	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	11	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	16	nC
ESR	Equivalent Series Resistance(G-S)	$f = 1\text{MHz}$	-	2.29	-	$\Omega$

### Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 75\text{V}, I_D = 100\text{A}$ $V_{GS} = 10\text{V}, R_{\text{GEN}} = 4.7\Omega$	-	28	66	ns
$t_r$	Turn-On Rise Time		-	37	84	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	62	134	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	21	52

### Drain-Source Diode Characteristics

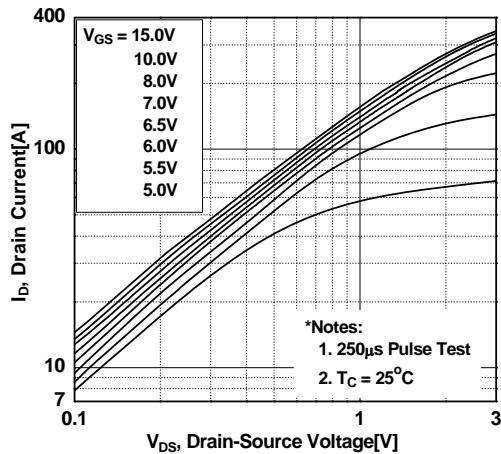
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	130	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	520	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 100\text{A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, V_{DD} = 75\text{V}, I_{SD} = 100\text{A}$ $dI_f/dt = 100\text{A}/\mu\text{s}$	-	97	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	264	-	nC

#### Notes:

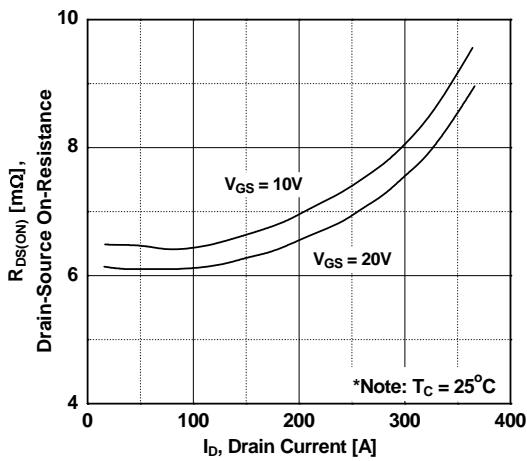
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 19.8\text{ A}$
3.  $I_{SD} \leq 100\text{ A}$ ,  $dI/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq \text{BV}_{\text{DSS}}$ . Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

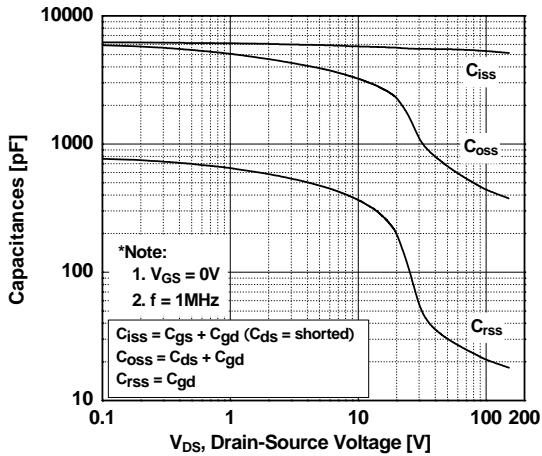
**Figure 1. On-Region Characteristics**



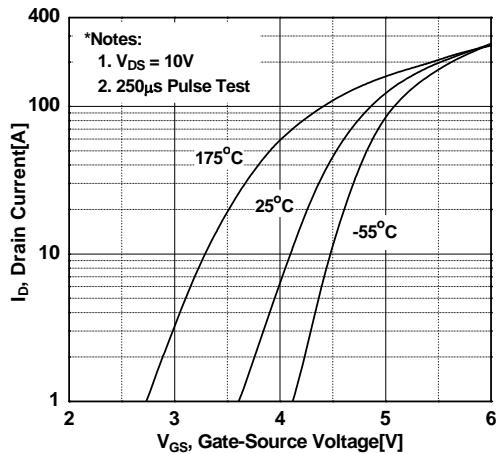
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



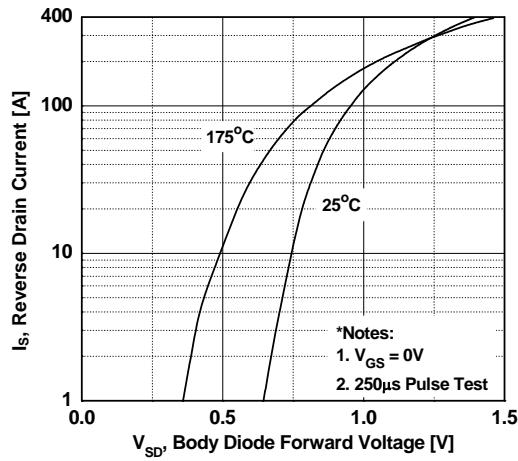
**Figure 5. Capacitance Characteristics**



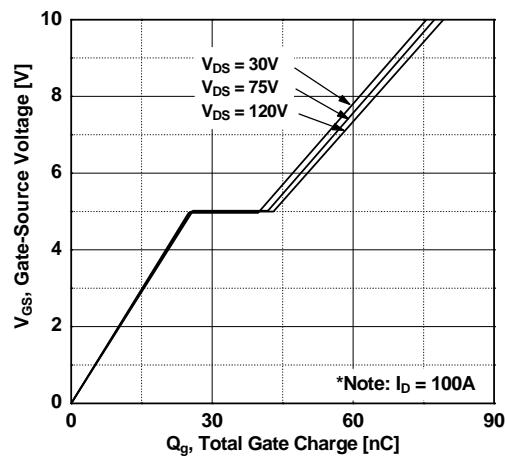
**Figure 2. Transfer Characteristics**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

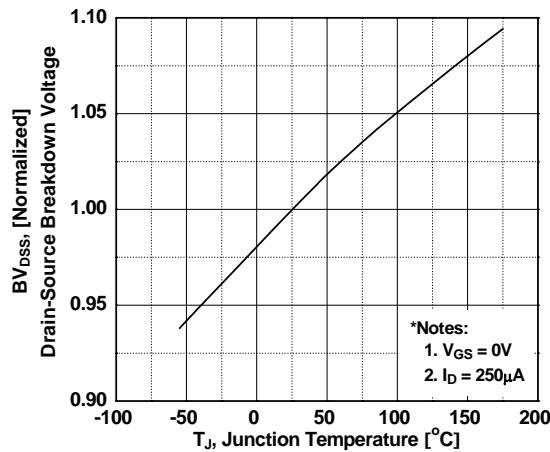


**Figure 6. Gate Charge Characteristics**

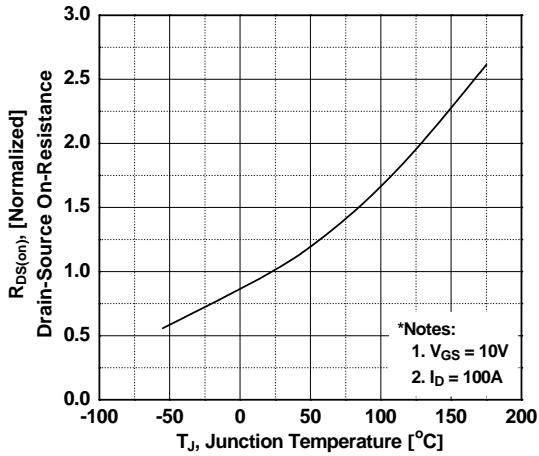


## Typical Performance Characteristics (Continued)

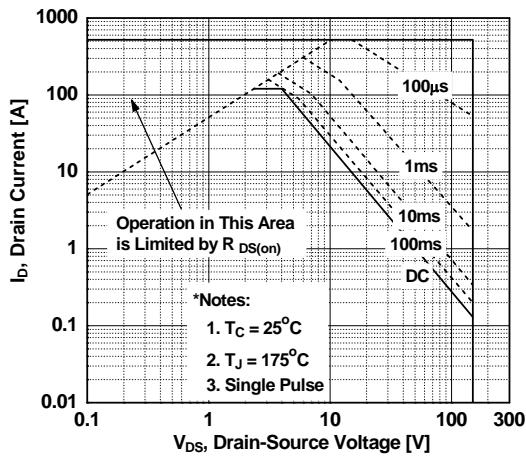
**Figure 7. Breakdown Voltage Variation vs. Temperature**



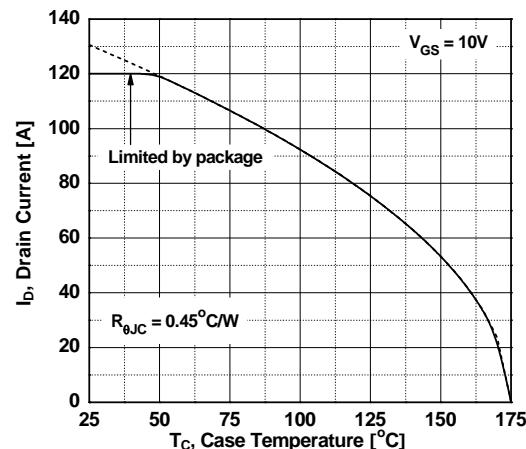
**Figure 8. On-Resistance Variation vs. Temperature**



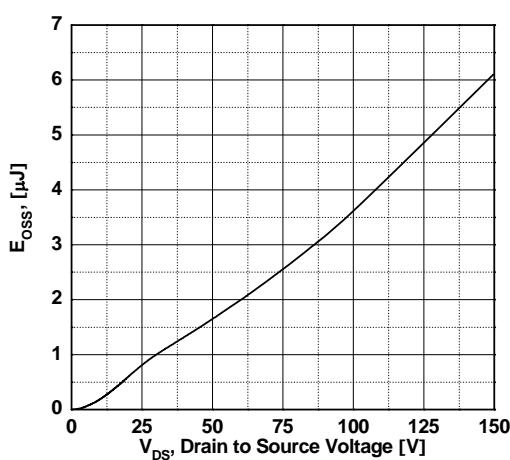
**Figure 9. Maximum Safe Operating Area vs. Case Temperature**



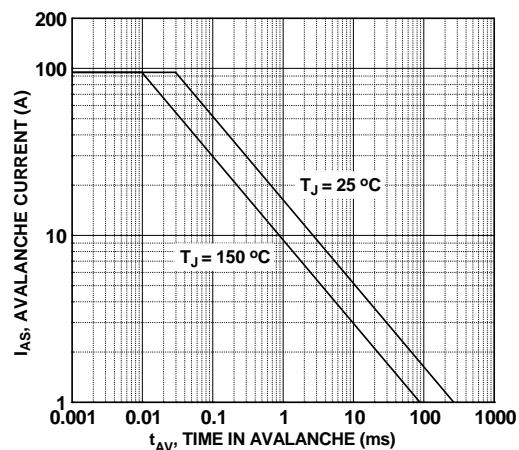
**Figure 10. Maximum Drain Current**



**Figure 11. Eoss vs. Drain to Source Voltage**

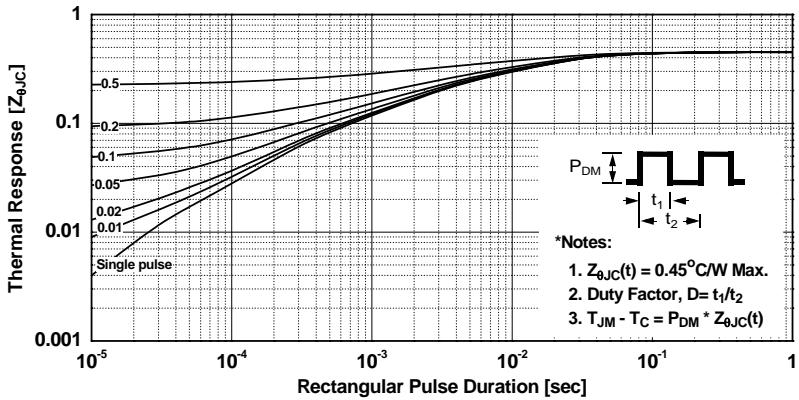


**Figure 12. Unclamped Inductive Switching Capability**

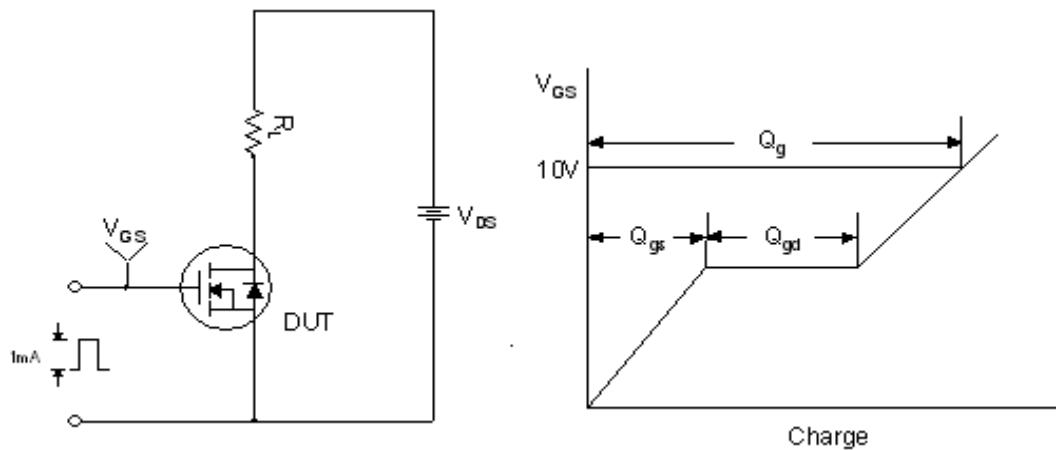


## Typical Performance Characteristics (Continued)

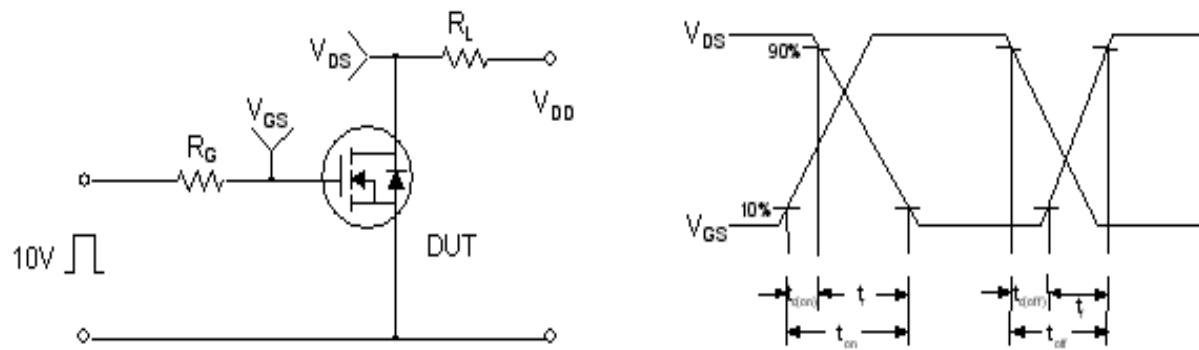
Figure 13. Transient Thermal Response Curve



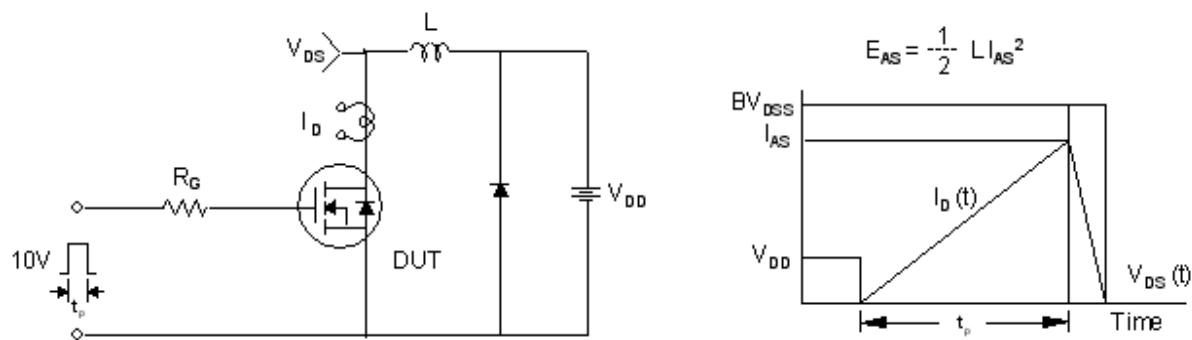
Gate Charge Test Circuit & Waveform



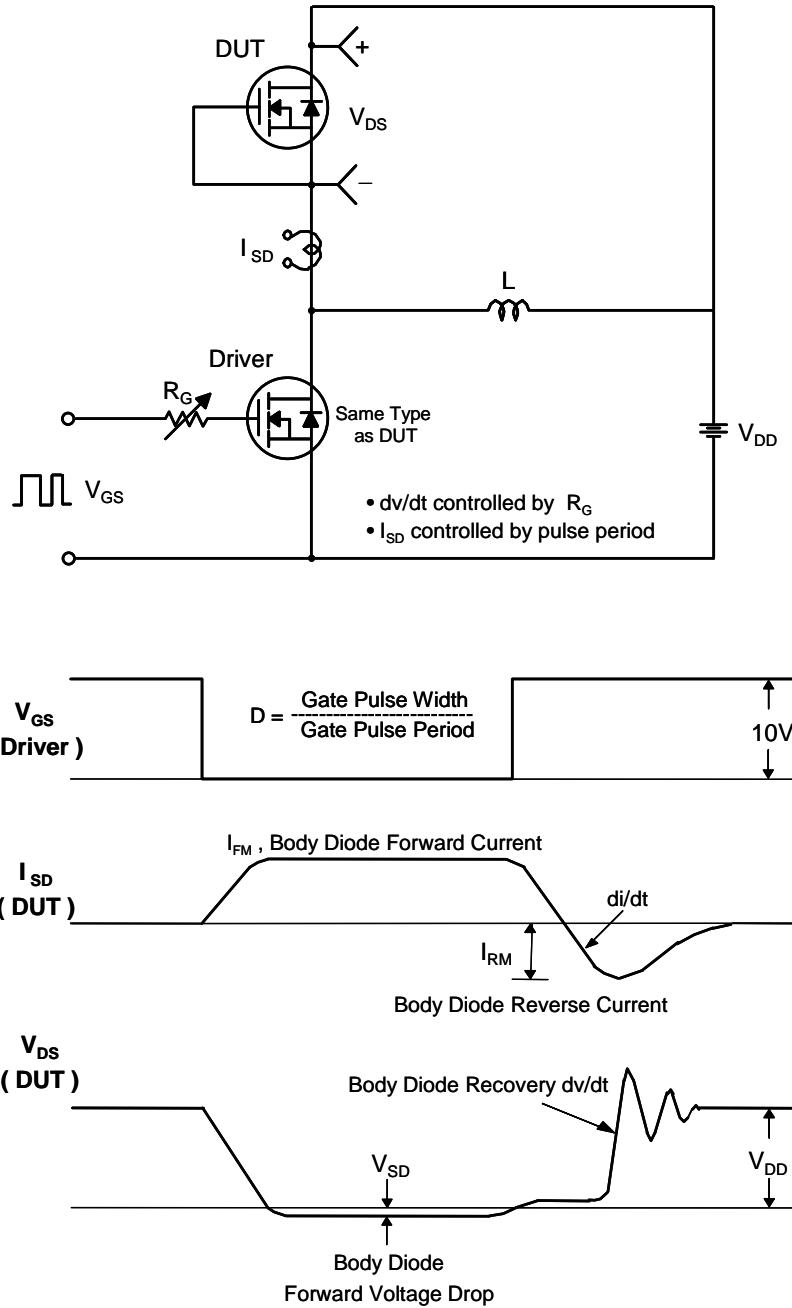
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



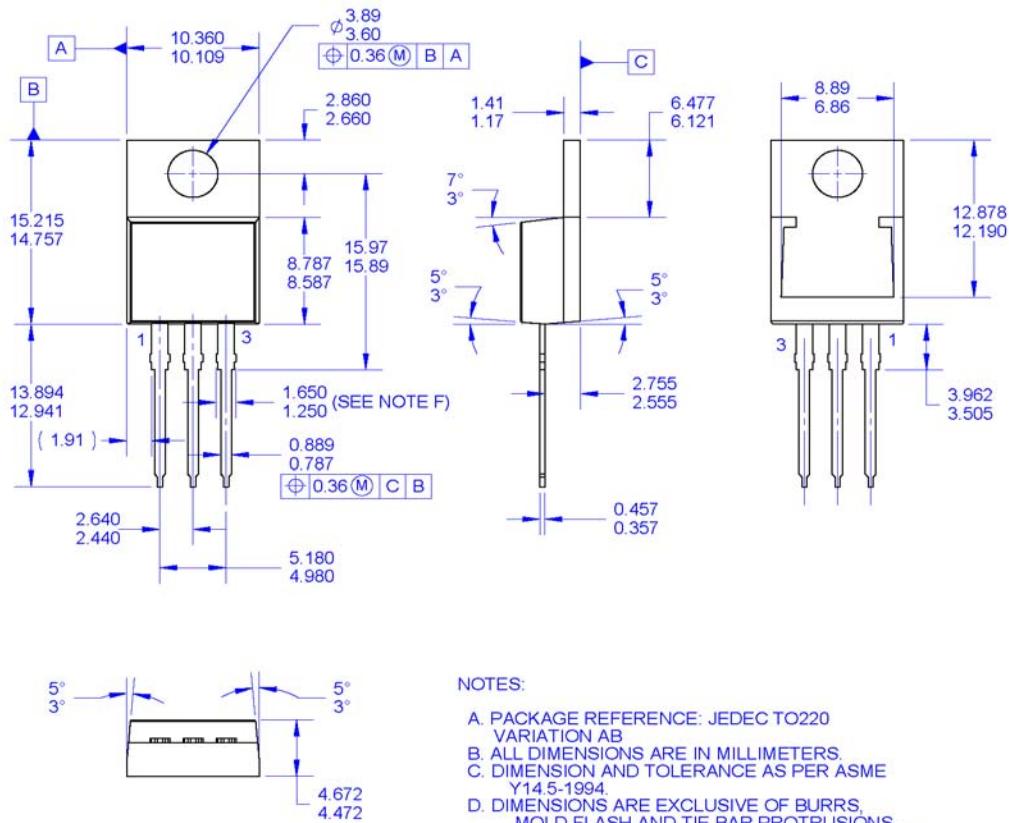
Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### TO-220

(F102: Trimmed Leads)



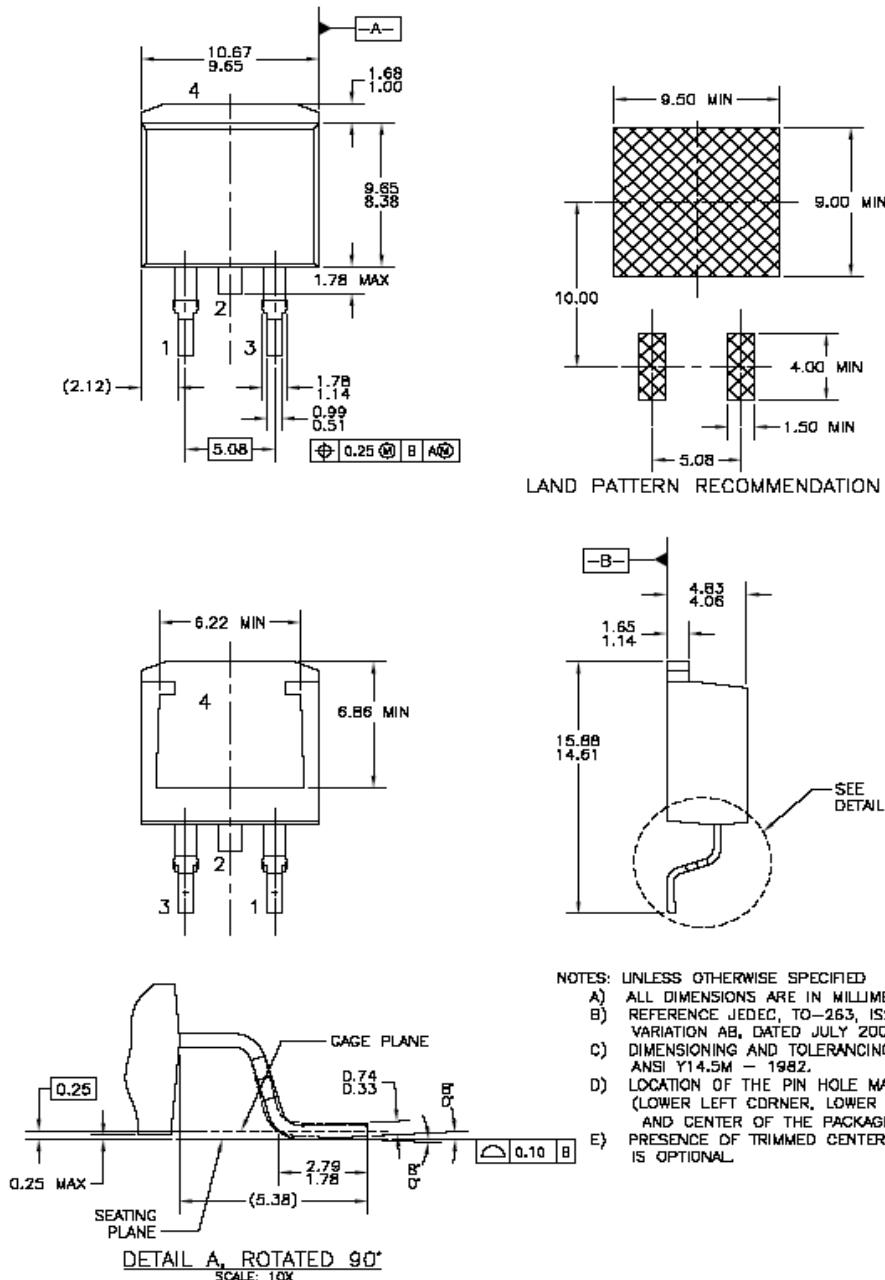
#### NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. THIS PACKAGE IS FSZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
- F. MAX WIDTH FOR F102 DEVICE = 1.35mm.
- G. DRAWING FILE NAME: TO220T03REV3

Dimensions in Millimeters

## Mechanical Dimensions

### D<sup>2</sup>PAK





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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