G4.4.17 PMXEVCNTR, Performance Monitors Selected Event Count Register

The PMXEVCNTR characteristics are:

Purpose

Reads or writes the value of the selected event counter, PMEVCNTR<x>. PMSELR.SEL determines which event counter is selected.

This register is part of the Performance Monitors registers functional group.

Usage constraints

This register is accessible as shown below:

EL0 (NS)	EL0 (S)	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS=1)	EL3 (SCR.NS=0)
Config-RW	Config-RW	RW	RW	RW	RW	RW

This register can be read at EL0 when PMUSERENR.EN or PMUSERENR.ER is set to 1, and can be written at EL0 when PMUSERENR.ER is set to 1.

If PMSELR.SEL selects a counter that is not accessible then reads and writes of PMXEVCNTR are CONSTRAINED UNPREDICTABLE, and must behave as one of the following:

- UNALLOCATED.
- RAZ/WI.
- No-op.
- As if PMSELR.SEL has an UNKNOWN value less than the number of counters accessible at the current exception level and security state.
- As if PMSELR.SEL is 31.
- If the counter is implemented but not accessible at the current exception level and security state, generate a System Register Trap or CP14 Register Trap exception taken to EL2.

This applies:

- If PMSELR.SEL is larger than the number of implemented counters.
- In an implementation that includes EL2, in Non-secure EL1 and EL0 modes, if PMSELR.SEL >= HDCR.HPMN.

Configurations

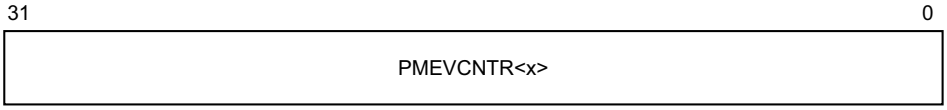
PMXEVCNTR is architecturally mapped to AArch64 register PMXEVCNTR_EL0.

There is one instance of this register that is used in both Secure and Non-secure states.

Attributes

PMXEVCNTR is a 32-bit register.

The PMXEVCNTR bit assignments are:



PMEVCNTR<x>, bits [31:0]

Value of the selected event counter, PMEVCNTR<x>, where x is the value stored in PMSELR.SEL.

Accessing the PMXEVCNTR:

To access the PMXEVCNTR:

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```
MRC p15,0,<Rt>,c9,c13,2 ; Read PMXEVCNTR into Rt
MCR p15,0,<Rt>,c9,c13,2 ; Write Rt to PMXEVCNTR
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Register access is encoded as follows:

coproc	opc1	CRn	CRm	opc2
1111	000	1001	1101	010

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