G4.4.6 PMCNTENSET, Performance Monitors Count Enable Set register

The PMCNTENSET characteristics are:

Purpose

Enables the Cycle Count Register, PMCCNTR, and any implemented event counters PMEVCNTR<x>. Reading this register shows which counters are enabled.

This register is part of the Performance Monitors registers functional group.

Usage constraints

This register is accessible as shown below:

EL0 (NS)	EL0 (S)	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS=1)	EL3 (SCR.NS=0)
Config-RW	Config-RW	RW	RW	RW	RW	RW

This register is accessible at EL0 when PMUSERENR.EN is set to 1.

If EL2 is implemented, in Non-secure EL1 and EL0 modes, the value of HDCR.HPMN can change the behavior of accesses to PMCNTENSET. See the description of the Px bit.

PMCNTENSET is used in conjunction with the PMCNTENCLR register.

Configurations

PMCNTENSET is architecturally mapped to AArch64 register PMCNTENSET_EL0.

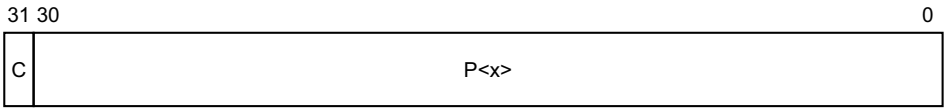
PMCNTENSET is architecturally mapped to external register PMCNTENSET_EL0.

There is one instance of this register that is used in both Secure and Non-secure states.

Attributes

PMCNTENSET is a 32-bit register.

The PMCNTENSET bit assignments are:



C, bit [31]

PMCCNTR enable bit. Enables the cycle counter register. Possible values are:

`0` When read, means the cycle counter is disabled. When written, has no effect.

`1` When read, means the cycle counter is enabled. When written, enables the cycle counter.

On Warm reset, the field reset value is architecturally UNKNOWN.

P<x>, bit [x] for x = 0 to (N - 1)

Event counter enable bit for PMEVCNTR<x>.

When EL2 is implemented, in Non-secure EL1 and EL0, N is the value in HDCR.HPMN. Otherwise, N is the value in PMCR.N.

Bits [30:N] are RAZ/WI.

Possible values of each bit are:

`0` When read, means that PMEVCNTR<x> is disabled. When written, has no effect.

`1` When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

Copyright © 2013 ARM Limited. All rights reserved.
Non-Confidential - Beta

On Warm reset, the field reset value is architecturally UNKNOWN.

Accessing the PMCNTENSET:

To access the PMCNTENSET:

```
MRC p15,0,<Rt>,c9,c12,1 ; Read PMCNTENSET into Rt
MCR p15,0,<Rt>,c9,c12,1 ; Write Rt to PMCNTENSET
```

Register access is encoded as follows:

coproc	opc1	CRn	CRm	opc2
1111	000	1001	1100	001

Copyright © 2013 ARM Limited. All rights reserved.
Non-Confidential - Beta