G4.4.14 PMSELR, Performance Monitors Event Counter Selection Register

The PMSELR characteristics are:

Purpose

Selects the current event counter PMEVCNTR<x> or the cycle counter, CCNT.

This register is part of the Performance Monitors registers functional group.

Usage constraints

This register is accessible as shown below:

EL0 (NS)	EL0 (S)	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS=1)	EL3 (SCR.NS=0)
Config-RW	Config-RW	RW	RW	RW	RW	RW

This register is accessible at EL0 when PMUSERENR.EN or PMUSERENR.ER is set to 1.

PMSELR is used in conjunction with PMXEVTYPER to determine the event that increments a selected event counter, and the modes and states in which the selected counter increments.

It is also used in conjunction with PMXEVCNTR, to determine the value of a selected event counter.

Configurations

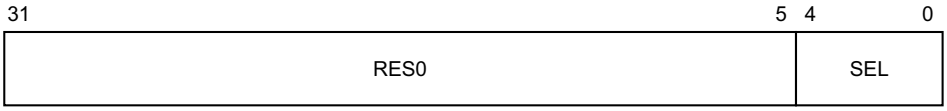
PMSELR is architecturally mapped to AArch64 register PMSELR_EL0.

There is one instance of this register that is used in both Secure and Non-secure states.

Attributes

PMSELR is a 32-bit register.

The PMSELR bit assignments are:



Bits [31:5]

Reserved, RES0.

SEL, bits [4:0]

Selects event counter, PMEVCNTR<x>, where x is the value held in this field. This value identifies which event counter is accessed when a subsequent access to PMXEVTYPER or PMXEVCNTR occurs.

This field can take any value from 0 (`0b00000`) to (PMCR.N)-1, or 31 (`0b11111`).

When PMSELR.SEL is `0b11111` it selects the cycle counter and:

- A read of the PMXEVTYPER returns the value of PMCCFILTR.
- A write of the PMXEVTYPER writes to PMCCFILTR.
- A read or write of PMXEVCNTR has CONSTRAINED UNPREDICTABLE effects, that can be one of the following:
  - Access to PMXEVCNTR is UNDEFINED.
  - Access to PMXEVCNTR behaves as a NOP.
  - Access to PMXEVCNTR behaves as if the register is RAZ/WI.

— Access to PMXEVCNTR behaves as if the PMSELR.SEL field contains an UNKNOWN value.

If this field is set to a value greater than or equal to the number of implemented counters, but not equal to 31, the results of access to PMXEVTYPER or PMXEVCNTR are CONSTRAINED UNPREDICTABLE, and can be one of the following:

- Access to PMXEVTYPER or PMXEVCNTR is UNDEFINED.
- Access to PMXEVTYPER or PMXEVCNTR behaves as a NOP.
- Access to PMXEVTYPER or PMXEVCNTR behaves as if the register is RAZ/WI.
- Access to PMXEVTYPER or PMXEVCNTR behaves as if the PMSELR.SEL field contains an UNKNOWN value.
- Access to PMXEVTYPER or PMXEVCNTR behaves as if the PMSELR.SEL field contains `0b11111`.

On Warm reset, the field reset value is architecturally UNKNOWN.

Accessing the PMSELR:

To access the PMSELR:

```
MRC p15,0,<Rt>,c9,c12,5 ; Read PMSELR into Rt
MCR p15,0,<Rt>,c9,c12,5 ; Write Rt to PMSELR
```

Register access is encoded as follows:

coproc	opc1	CRn	CRm	opc2
1111	000	1001	1100	101