# Appendix E – Design Vision Synthesis Report

**Listing 1 Area Report of ZS Design**

```
****************************************
Report : area
Design : srp
Version: A-2007.12
Date   : Tue Jan 20 16:40:17 2009
****************************************

Library(s) Used:

    fast (File: /home/ias122/data/StandCell/aci/sc/synopsys/fast.db)

Number of ports:              142
Number of nets:               769
Number of cells:                8
Number of references:           8

Combinational area:       112342.507139
Noncombinational area:    113859.348114
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          226201.855253
Total area:                 undefined
```

**Listing 2 Timing Report of ZS Design**

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : srp
Version: A-2007.12
Date   : Tue Jan 20 16:40:17 2009
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast   Library: fast
Wire Load Model Mode: top

  Startpoint: idStage/PIPE_aluInA/outp_reg[2]
              (rising edge-triggered flip-flop)
  Endpoint: Dadd[5] (output port)
  Path Group: (none)
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  idStage/PIPE_aluInA/outp_reg[2]/CK (DFFRHQX1)           0.00 #     0.00 r
  idStage/PIPE_aluInA/outp_reg[2]/Q (DFFRHQX1)            0.27       0.27 r
  idStage/PIPE_aluInA/outp[2] (delay32_5)                 0.00       0.27 r
  idStage/aluInA[2] (idStage)                             0.00       0.27 r
  exStage/aluInA[2] (exStage)                             0.00       0.27 r
  exStage/ksAdder/x32[2] (ksAdder)                        0.00       0.27 r
  exStage/ksAdder/stage0/x2 (stage0)                      0.00       0.27 r
  exStage/ksAdder/stage0/g_p2/xi (g_p_30)                 0.00       0.27 r
  exStage/ksAdder/stage0/g_p2/U1/Y (XOR2X1)               0.13       0.40 f
```

```
  exStage/ksAdder/stage0/g_p2/pi (g_p_30)                 0.00       0.40 f
  exStage/ksAdder/stage0/p2_2 (stage0)                    0.00       0.40 f
  exStage/ksAdder/stage1/pi1 (stage1)                     0.00       0.40 f
  exStage/ksAdder/stage1/ksOpBlack1/pi (ksOpBlack_128)
                                                          0.00       0.40 f
  exStage/ksAdder/stage1/ksOpBlack1/U1/Y (AND2X1)         0.11       0.52 f
  exStage/ksAdder/stage1/ksOpBlack1/pik (ksOpBlack_128)
                                                          0.00       0.52 f
  exStage/ksAdder/stage1/p1_1 (stage1)                    0.00       0.52 f
  exStage/ksAdder/stage2/pi0 (stage2)                     0.00       0.52 f
  exStage/ksAdder/stage2/ksOpBlack0/pi (ksOpBlack_98)     0.00       0.52 f
  exStage/ksAdder/stage2/ksOpBlack0/U3/Y (AOI21X1)        0.08       0.59 r
  exStage/ksAdder/stage2/ksOpBlack0/U2/Y (INVX1)          0.06       0.65 f
  exStage/ksAdder/stage2/ksOpBlack0/gik (ksOpBlack_98)
                                                          0.00       0.65 f
  exStage/ksAdder/stage2/g0_0 (stage2)                    0.00       0.65 f
  exStage/ksAdder/ksOpGray3/Gg (ksOpGray_29)              0.00       0.65 f
  exStage/ksAdder/ksOpGray3/U2/Y (AOI21X1)                0.05       0.70 r
  exStage/ksAdder/ksOpGray3/U1/Y (INVX1)                  0.06       0.76 f
  exStage/ksAdder/ksOpGray3/G (ksOpGray_29)               0.00       0.76 f
  exStage/ksAdder/ksOpGray7/Gc (ksOpGray_25)              0.00       0.76 f
  exStage/ksAdder/ksOpGray7/U2/Y (AOI21X1)                0.08       0.84 r
  exStage/ksAdder/ksOpGray7/U1/Y (INVX1)                  0.05       0.89 f
  exStage/ksAdder/ksOpGray7/G (ksOpGray_25)               0.00       0.89 f
  exStage/ksAdder/U3/Y (XOR2X1)                           0.11       1.00 r
  exStage/ksAdder/s32[7] (ksAdder)                        0.00       1.00 r
  exStage/dMemWRAddr[5] (exStage)                         0.00       1.00 r
  Dadd[5] (out)                                           0.00       1.00 r
  data arrival time                                                  1.00
  ---------------------------------------------------------------------------
  (Path is unconstrained)
```

**Listing 3 Area Report of Parity**

```
****************************************
Report : area
Design : PARITY
Version: A-2007.12
Date   : Tue Dec 16 16:47:34 2008
****************************************

Library(s) Used:

    fast (File: /home/ias122/data/StandCell/aci/sc/synopsys/fast.db)

Number of ports:               51
Number of nets:                99
Number of cells:               49
Number of references:           2

Combinational area:       1303.948816
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          1303.948816
Total area:                 undefined
```

**Listing 4 Timing Report of Parity**

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : PARITY
Version: A-2007.12
Date   : Tue Dec 16 16:47:34 2008
****************************************

Operating Conditions: fast   Library: fast
Wire Load Model Mode: top

  Startpoint: A[4] (input port)
  Endpoint: Y (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  A[4] (in)                                0.00       0.00 r
  U91/Y (XNOR2X1)                          0.11       0.11 f
  U90/Y (XOR2X1)                           0.12       0.23 r
  U89/Y (XOR2X1)                           0.11       0.34 f
  U88/Y (XOR2X1)                           0.11       0.45 r
  U86/Y (XOR2X1)                           0.09       0.54 f
  U82/Y (XOR2X1)                           0.11       0.65 r
  U81/Y (XOR2X1)                           0.09       0.74 f
  U79/Y (XOR2X1)                           0.11       0.86 r
  U75/Y (XOR2X1)                           0.09       0.95 f
  U74/Y (XOR2X1)                           0.11       1.06 r
  U72/Y (XOR2X1)                           0.09       1.15 f
  U68/Y (XOR2X1)                           0.11       1.27 r
  U67/Y (XOR2X1)                           0.09       1.36 f
  U65/Y (XOR2X1)                           0.11       1.47 r
  U61/Y (XOR2X1)                           0.09       1.56 f
  U60/Y (XOR2X1)                           0.11       1.67 r
  U58/Y (XOR2X1)                           0.09       1.76 f
  U54/Y (XOR2X1)                           0.11       1.88 r
  U53/Y (XOR2X1)                           0.09       1.97 f
  U51/Y (XOR2X1)                           0.12       2.08 r
  U50/Y (XOR2X1)                           0.09       2.17 f
  Y (out)                                  0.00       2.17 f
  data arrival time                                   2.17
  -----------------------------------------------------------
  (Path is unconstrained)
```