CPEN 211 Introduction to Microcomputers, 2021
Lab Proficiency Test #1

Question 2 [2 marks]: This question is not related to Question 1. Create a file named "**q2.v**" and inside it write **synthesizable** Verilog for the purely combinational logic block labeled "MealyDec" in Figure 2 (block on right) matching the following specification. The expected behavior of the overall circuit in Figure 2 is shown in Figure 3. You do **not** need to write Verilog for the Moore state machine in Figure 2 (block on left) and code for it is **not** provided. You do **not** need to use your solution to Question 1 to answer this question. Instead, your task is writing synthesizable Verilog for only the MealyDec combinational logic block. Upload your q2.v to Canvas as your answer for Question 2 in **"Lab Proficiency Test #1"**.

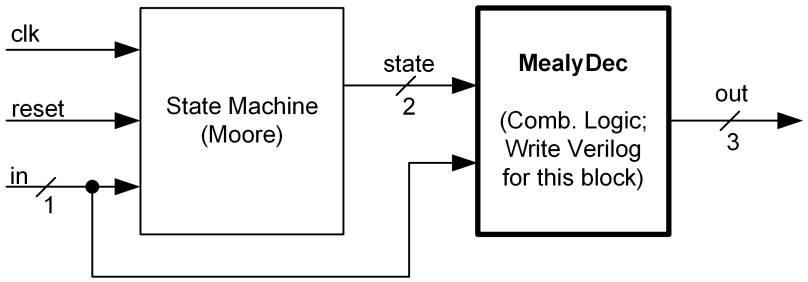

Figure 2

The inputs to `MealyDec` are a 2-bit signal *state* and one-bit single *in.* The signal *state* indicates the present state of the Moore state machine in Figure 2 (block on left). Assume the Moore machine in Figure 2 has the same states and transitions as the Mealy machine in Figure 3 below. Recall the state transitions of a Mealy machine are labeled with <input>/<output>. For example, when in State A if the input is 0 the output should be 3'b111 and the next state will be B. Bits on the left have higher index value. Assume the output *state* of the Moore state machine in Figure 2 is the Moore machine's present state. Specifically, assume *state* is 2'b00 when in State A, 2'b01 when in State B, 2'b10 when in State C, and 2'b11 when in State D. The 3-bit output *out* of `MealyDec` should be the 3-bit output corresponding to each transition in the diagram below. The label `x` in Figure 3 matches either a 0 or 1 value for input *in*.

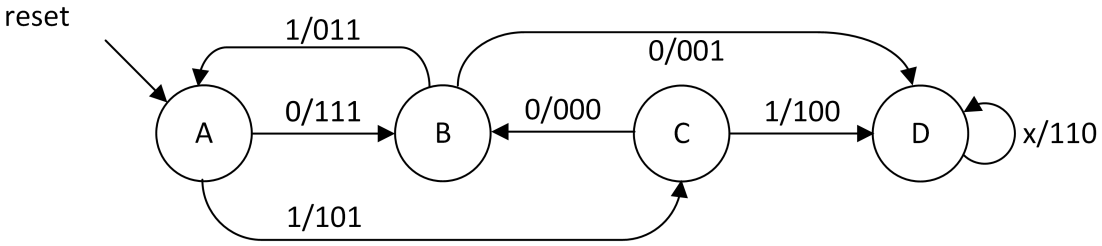

Figure 3

The autograder used to mark your answer will assume your top-level module is called "`MealyDec`" with inputs "`state`" and "`in`", and output "`out`" declared as follows:

```
module MealyDec(state,in,out);
  input [1:0] state;
  input in;
  output [2:0] out;
```

Ensure your final attempt for "Lab Proficiency Test #1" includes both q1.v and q2.v.