CPEN 211 Introduction to Microcomputers, 2018
Lab Proficiency Test #2

Question 1 [3 marks]: Create a file named "**q1.v**" and inside it write **synthesizable** Verilog that implements the finite state machine illustrated in the figure below. Like the examples in class, state transitions occur on the rising edge of input "`clk`" and the reset is synchronous (occurs on the rising edge of clk) and is active high (`reset` equal to `1'b1` means reset). Transitions from a state to itself are not explicitly shown. The condition for an unlabeled edge is always true. The input "`in`" is 2-bits wide. The output "`out`" is 3-bits wide. The output for each state is shown in square brackets. For example, when in state A, `out` should be 101, and if `in` is 11, then the next state should be B. The auto grader used to mark your answer will assume your top-level module is called "`top_module`" with inputs "`clk`", "`reset`" and "`in`", output "`out`", and that "`top_module`" is declared as follows:

```
module top_module(clk,reset,in,out);
```

Your q1.v file **must** include definitions for any modules instantiated inside `top_module` (even those from the slides or textbook). **Upload your Verilog file named "q1.v" via the "Lab Proficiency Test #2" assignment on Canvas <u>before</u> 6:50 pm as the submission site closes at exactly 6:50 pm.** Do **NOT** "zip" your submission. The file you upload for this question **must** be called "q1.v" or the autograder script will not mark it.

Your solution will get zero if any of the following are true:

1. Your **last** "Lab Proficiency Test #2" attempt on Canvas does not include "q1.v",
2. Your q1.v file does not compile using ModelSim (e.g., due to syntax errors),
3. Your q1.v file does not contain a module called `top_module` with inputs/outputs as above,
4. Your `top_module` cannot be simulated (e.g., due to missing module definitions in q1.v),
5. The Verilog used by your `top_module` is not synthesizable by Quartus.
6. The Verilog used by your `top_module` has any inferred latches.
7. Your `top_module` output "`out`" does not exactly match the output of the state machine below for some sequence of values for inputs "`clk`", "`reset`" and "`in`".