



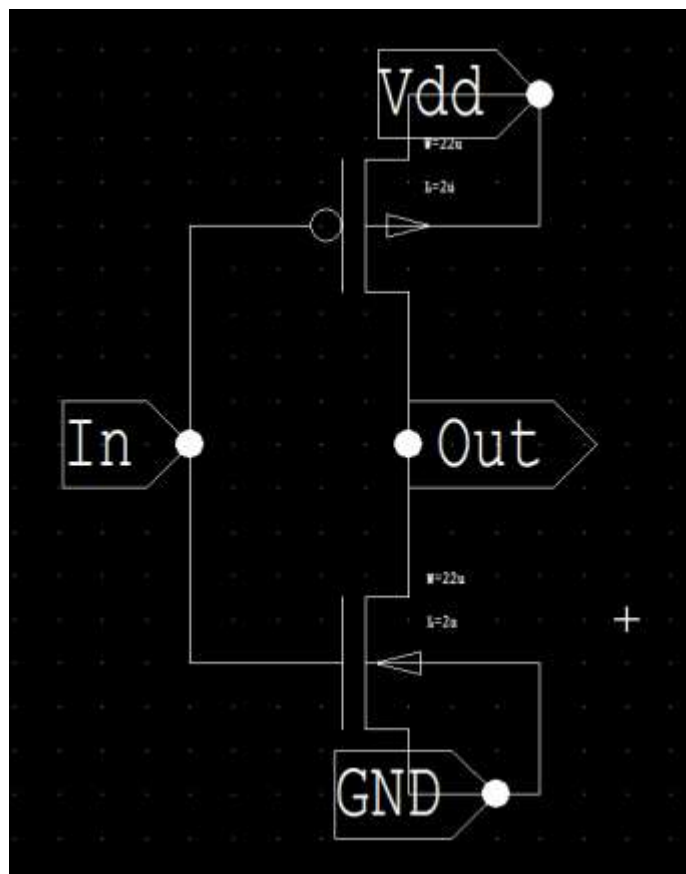
# DIGITAL IC LAB

Name: Rania Hamada Mohammed

ID: 79

## Assignment 1: CMOS Inverter Characteristics

INVERTER SCHEMATIC:





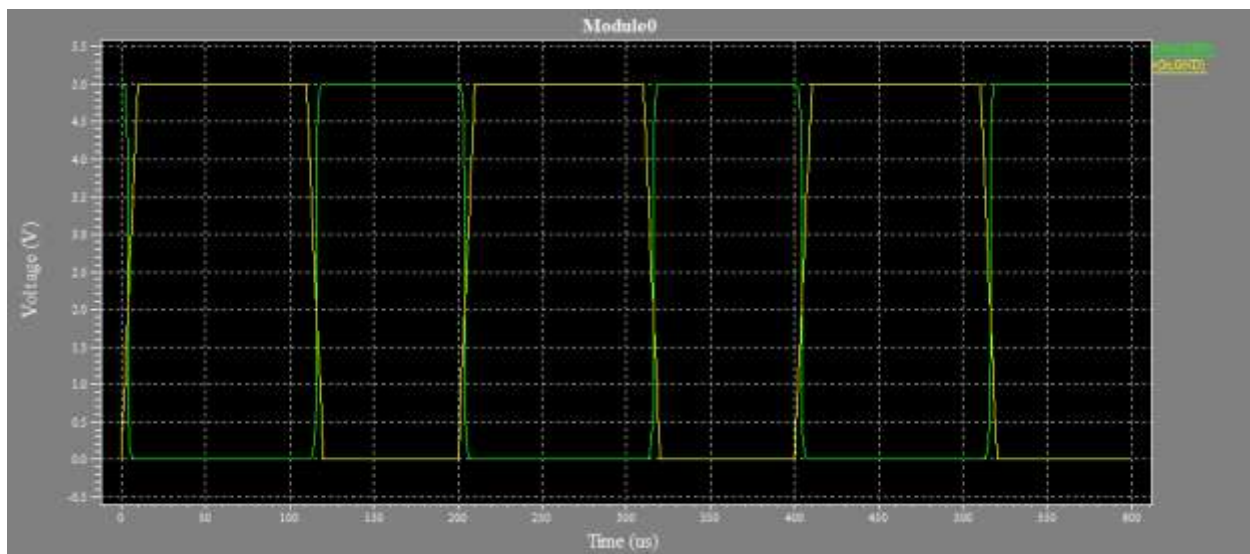
## TRANSIENT RESPONSE:

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 17:01:39
.include "D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab2\m15_20.md"

* Waveform probing commands
.probe
.options probefilename="inverter_schematic.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\inverter_sch.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 Out In GND GND NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
VPULSE In GND PULSE (0 5 0 0 0 100u 200u)
VSupply Vdd GND 5
.tran/op 10u 600u method=bdf
.print tran v(In,GND) v(Out,GND)
```

## OUTPUT:





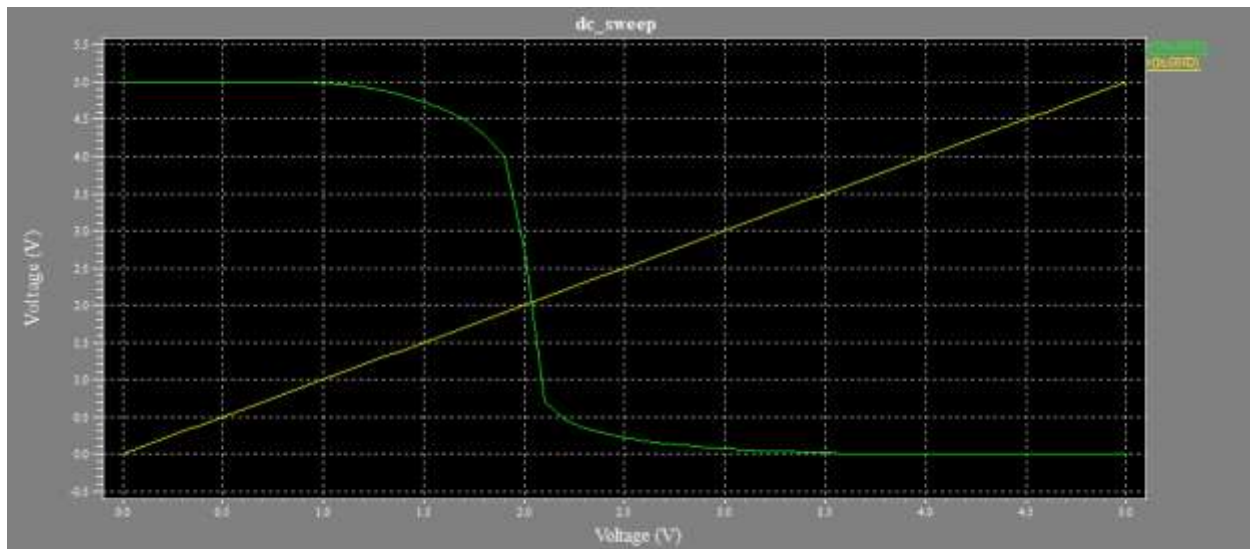
## DC SWEEP:

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 17:15:28
.include "D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\m15_20.md"

* Waveform probing commands
.probe
.options probefilename="inverter_sch.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\Simulation\inverter_sch.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 Out In GND GND NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
VSupply Vdd GND 5
Vin In GND 5
.dc lin source Vin 0 5 0.1
.print dc v(In,GND) v(Out,GND)
```

## OUTPUT:



## COMMENT:

We notice that  $V_{th} = 2.03 \text{ V}$  when  $V_{DD} = 5 \text{ V}$ , NMOS has  $L=2\mu \text{ W}=22\mu$  and PMOS has  $L=2\mu \text{ W}=22\mu$



## REQUIREMENTS:

- 1- RESIZE TRANSISTORS TO GET MATCHING INVERTER  $V_{TH} = V_{DD}/2$  (THIS IS DONE BY DC SWEEP

We resized the transistors by trials until getting the matching inverter where  $V_{th} = 2.5$  V which is  $V_{DD}/2$ , and thus where,

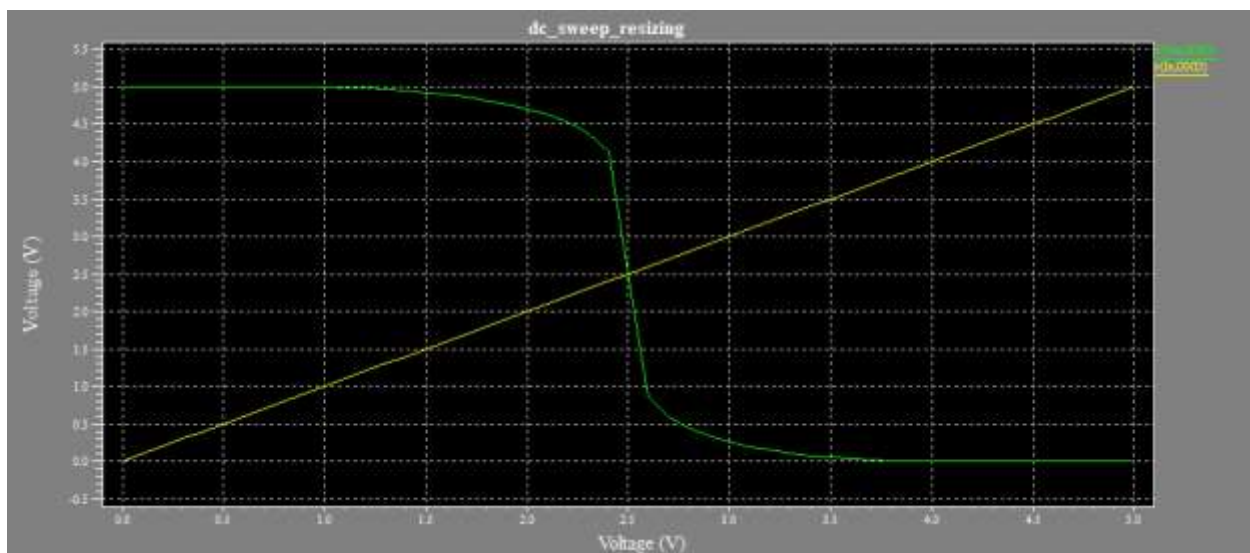
- NMOS has  $L=2\mu$   $W=10.7\mu$
- PMOS has  $L=2\mu$   $W=34.5\mu$

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 17:15:28
.include "D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\m15_20.md"

* Waveform probing commands
.probe
.options probefilename="inverter_sch.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\Simulation\inverter_sch.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 Out In GND GND NMOS L=2u W=10.7u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=34.5u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
VSupply Vdd GND 5
Vin In GND 5
.dc lin source Vin 0 5 0.1
.print dc v(In,GND) v(Out,GND)
```

## OUTPUT:





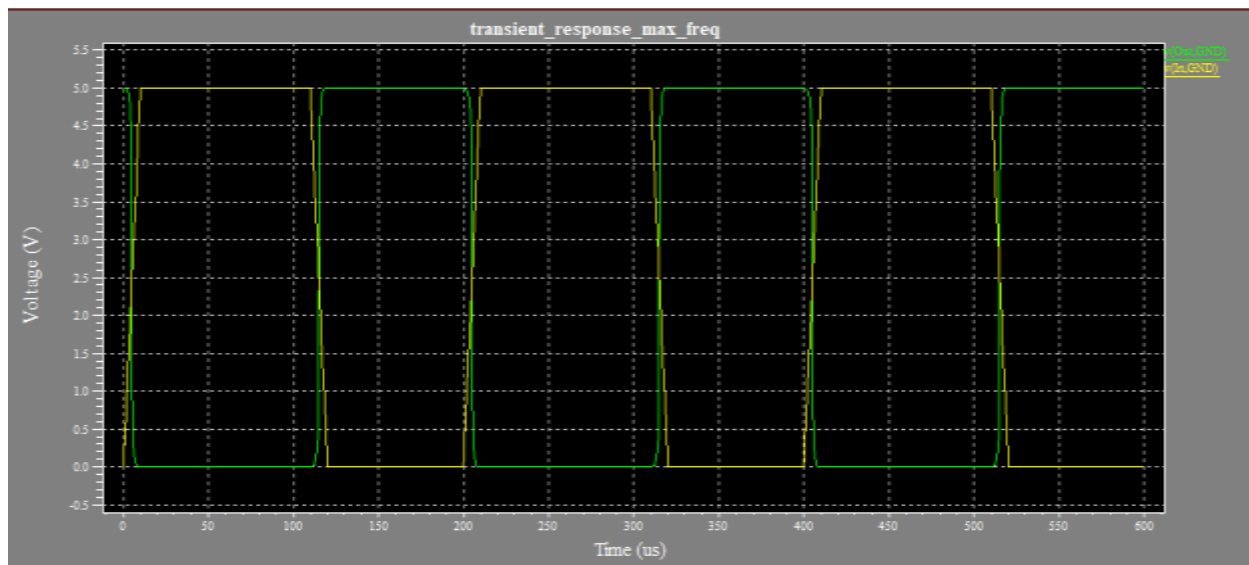
## 2- RESIZE TRANSISTORS TO ENSURE $\tau_{PHL} = \tau_{PLH}$ , ALSO MEASURE THE MAX FREQUENCY (THIS IS DONE BY TRANSIENT ANALYSIS)

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 17:01:39
.include "D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab2\ml5_20.md"

* Waveform probing commands
.probe
.options probefilename="inverter_schematic.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\inverter_sch.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 Out In GND GND NMOS L=2u W=10.7u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=34.5u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
VPulse In GND PULSE (0 5 0 0 0 100u 200u)
VSupply Vdd GND 5
.tran/op 10u 600u method=50f
.print tran v(In,GND) v(Out,GND)
|
```

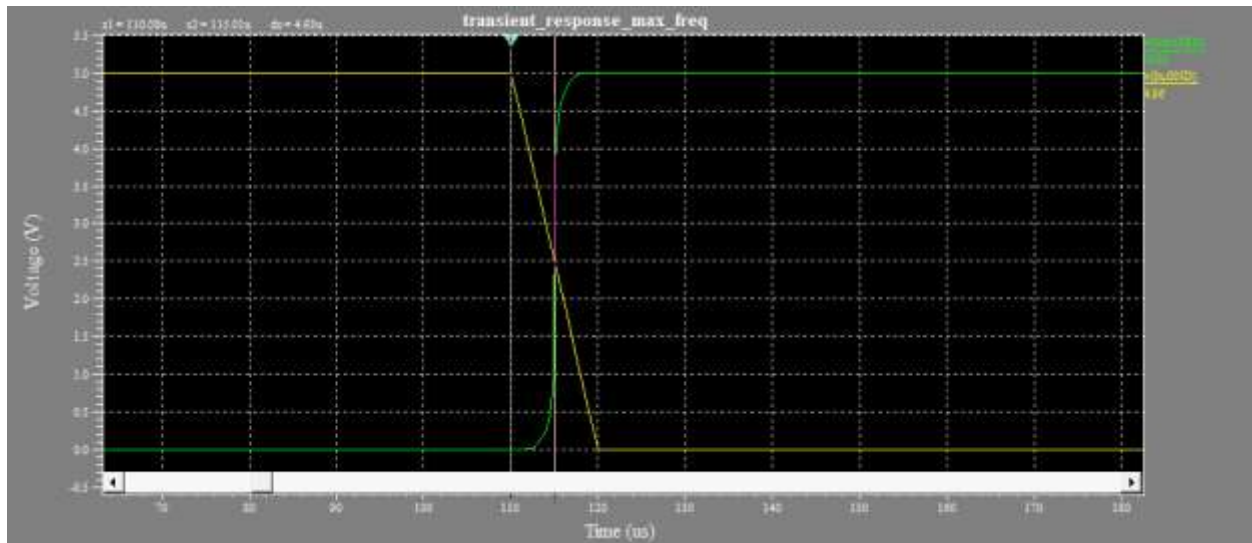
OUTPUT:



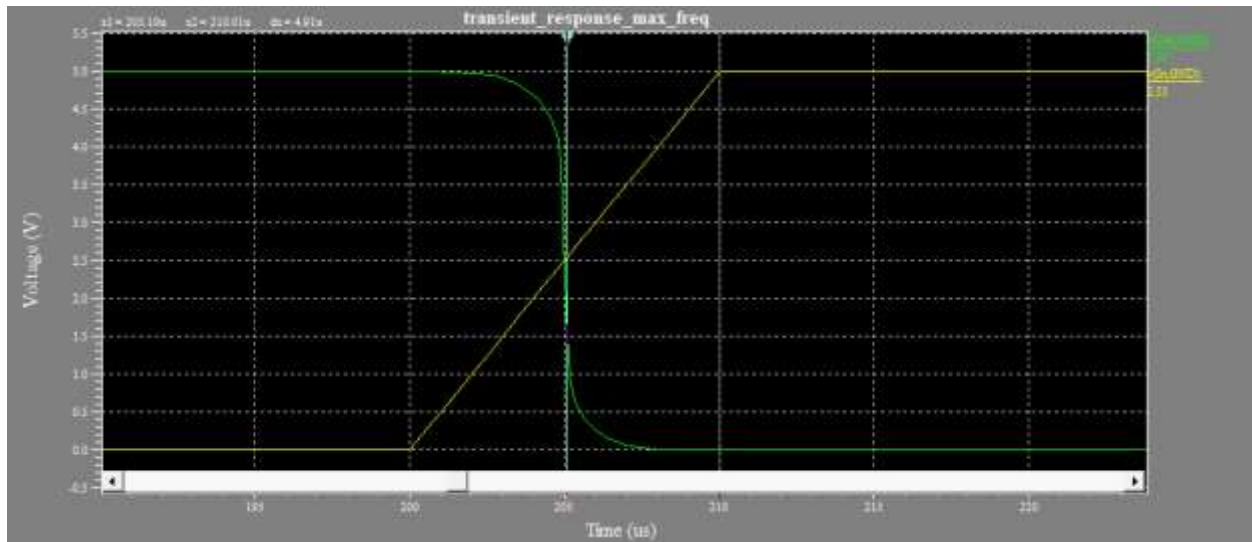


GETTING  $\tau_{PHL}$  AND  $\tau_{PLH}$ :

$\tau_{PHL} \approx 4.93\mu s$



$\tau_{PLH} \approx 4.91\mu s$

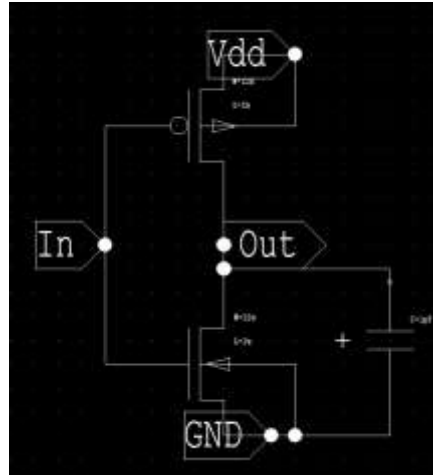


Then,  $\tau_{PHL} \approx \tau_{PLH}$





### 3- WITH A CAPACITOR OF 1pF ADDED

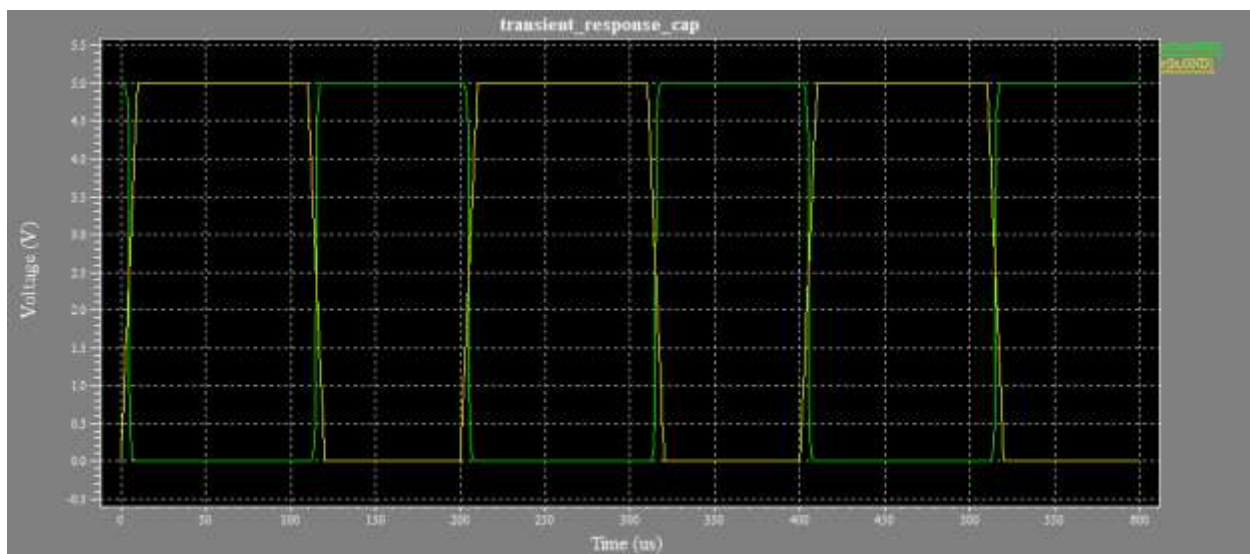


```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 17:01:39
.include "D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab2\ml5_20.md"

* Waveform probing commands
.probe
.options probefilename="inverter_sch_cap.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\Simulation\inverter_sch_cap.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
C1 Out GND 1pF
M1 Out In GND NMOS L=2u W=10.7u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=34.5u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
VPulse In GND PULSE (0 5 0 0 0 100u 200u)
VSupply Vdd GND 5
.tran/op 10u 600u method=50f
.print tran v(In,GND) v(Out,GND)
```

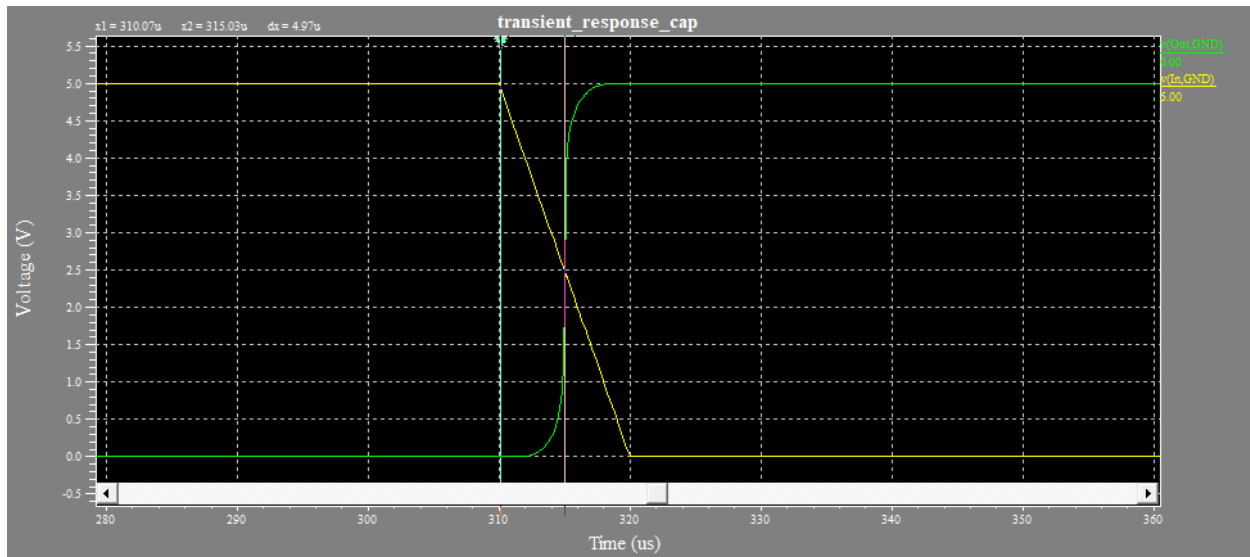
OUTPUT:





GETTING  $\tau_{PHL}$  AND  $\tau_{PLH}$ :

$\tau_{PHL} \approx 4.97\mu s$



$\tau_{PLH} \approx 4.95\mu s$

