Alexandria University
Faculty of Engineering
Electrical and Electronics Engineering Department
Fall semester, 2021/2022

جامعة الإسكندرية
كلية الهندسة
قسم الهندسة الكهربية
الفصل الدراسى الأول, 2022/2021

DIGITAL IC LAB

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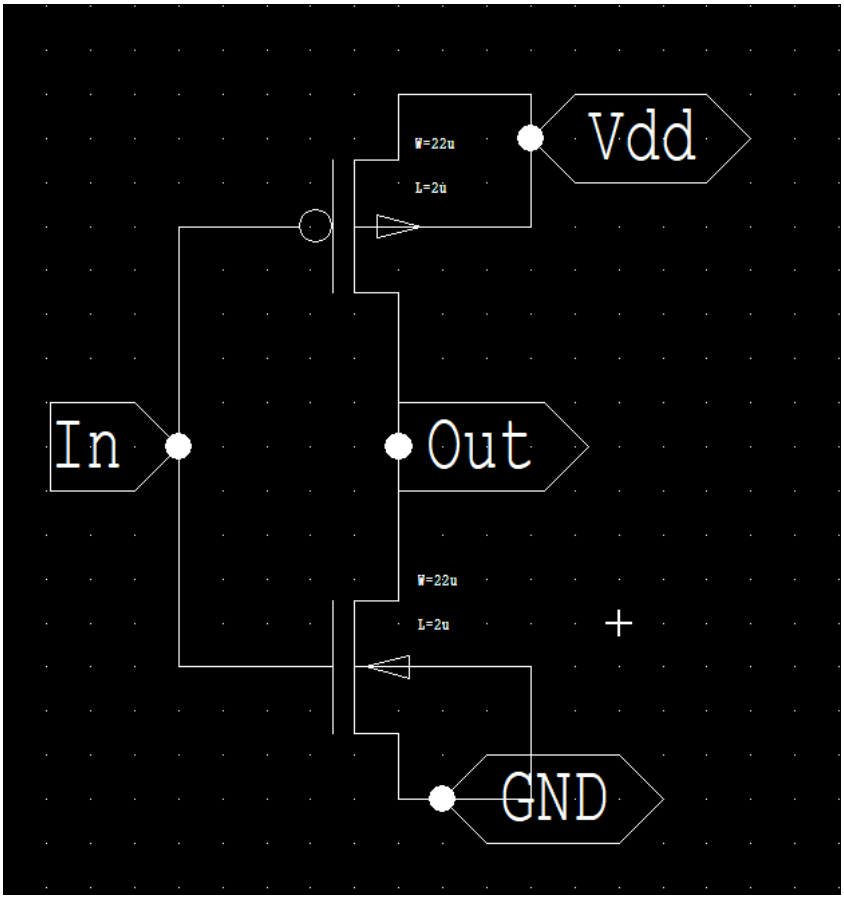
ID: 79

Assignment 2: CMOS Inverter Layout and LVS

INVERTER SCHEMATIC:



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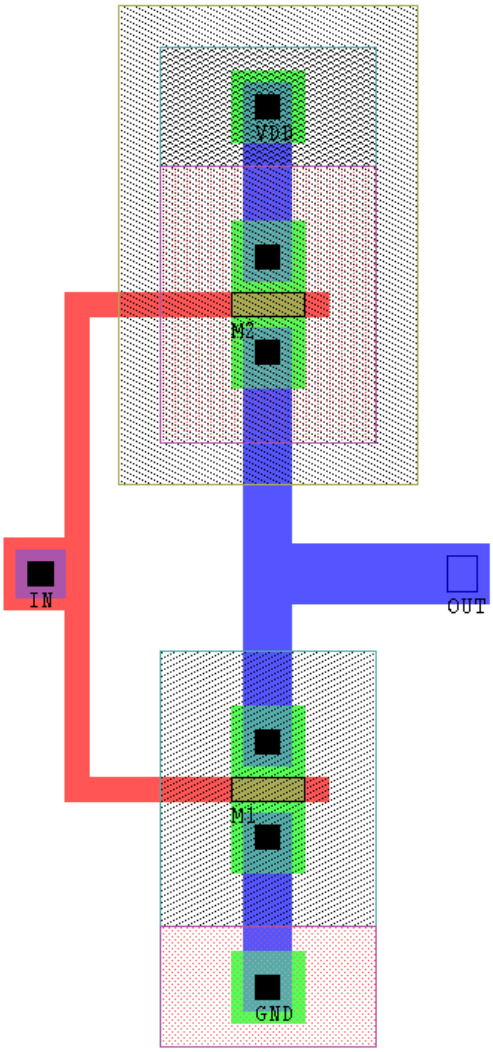
SCHEMATIC NETLIST

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 30, 2021 at 18:56:53
.include ml5_20.md

* Waveform probing commands
.probe
.options probefilename="inverter_sch_lvs.dat"
+ probesdbfile="D:\Materials\college\final year\Final-year-projects\Digital IC\labs\lab1\Simulation\inverter_sch_lvs.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 Out In GND GND NMOS L=2u W=10.7u AD=66p PD=24u AS=66p PS=24u
M2 Out In Vdd Vdd PMOS L=2u W=34.3u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0
```

INVERTER LAYOUT



LAYOUT NETLIST:

```
* Extract Date and Time:  12/30/2021 - 19:17

.include ml5_20.md

* Warning:  Layers with Unassigned AREA Capacitance.
*   <N Diff Resistor>
*   <Poly2 Resistor>
*   <P Diff Resistor>
*   <N Well Resistor>
*   <Poly Resistor>
*   <P Base Resistor>
* Warning:  Layers with Unassigned FRINGE Capacitance.
*   <Pad Comment>
*   <N Diff Resistor>
*   <Poly2 Resistor>
*   <P Diff Resistor>
*   <N Well Resistor>
*   <Poly Resistor>
*   <Poly1-Poly2 Capacitor>
*   <P Base Resistor>
* Warning:  Layers with Zero Resistance.
*   <Pad Comment>
*   <NMOS Capacitor>
*   <PMOS Capacitor>
*   <Poly1-Poly2 Capacitor>

* NODE NAME ALIASES
*       1 = OUT (15,-59)
*       2 = IN (-20,-58.5)
*       3 = VDD (-1,-19.5)
*       4 = GND (-1,-93)


M2 1 2 3 3 PMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u
* M2 DRAIN GATE SOURCE BULK (-3 -36 3 -34)
M1 4 2 1 4 NMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u
* M1 DRAIN GATE SOURCE BULK (-3 -76.5 3 -74.5)

* Total Nodes: 4
* Total Elements: 2
```

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LVS VERIFICATION