

Analog and Digital IC Design Practice
Lab Project Report on
**“NEURAL AMPLIFIER WITH
CAPACITIVE FEEDBACK”**

“Till Post Layout Simulation”

*Project
Using
Cadence Virtuoso
gdk90*
Submitted by
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Introduction:

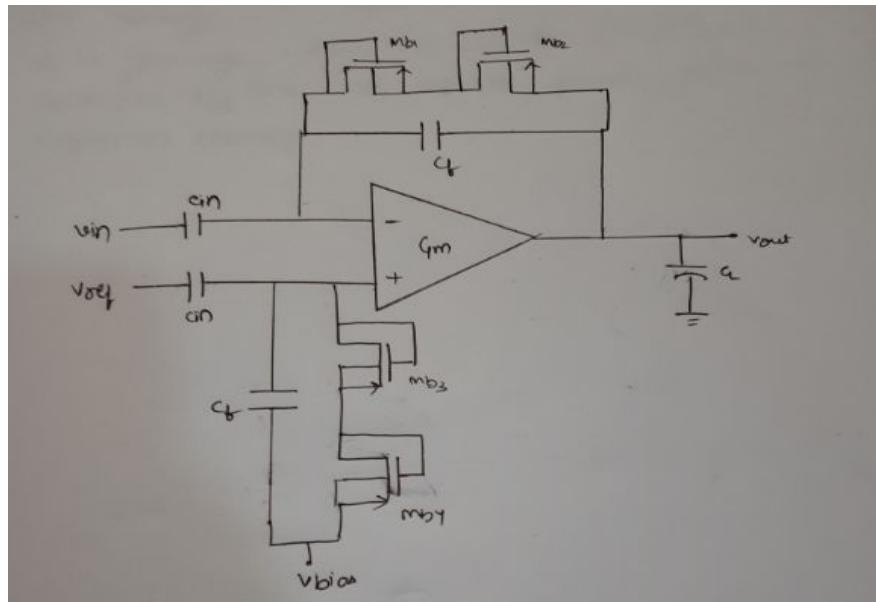
Neural Amplifier IC:

NEURAL AMPLIFIERS are biopotential amplifiers, explicitly intended in order to enhance and condition bioelectric signals that are emerging from the sensory system. The neural signals can be characterized by its frequency content(bandwidth) & its amplitude. Generally they carry amplitudes of little value which may be of order from micro to milli volts hence we require an amplifier which can boost or amplify such signals meanwhile rejecting the noise attached to the signal developed from source which may also be thermal noises.

The neural signals can be transduced from neural tests, for example, recording ECG signals or using the microelectrodes in order to record neural spikes or similar activities. Neural signals should be first pre-amplified by front end amplifiers, these amplifiers must possess high gain & low input referred noise than the subsequent stages in design. The noise from further subsequent stages should be referred back to these electrodes through the gain of such amplifiers. As we know, the gain of common mode signals are too less which rather attenuates the noise signals. After getting an amplified version of neural signals with lowest noise attached to it, it can be fed to post features in order to digitize the signals and process through the processor & to envision the desired waveform on an oscilloscope.

The important features of a Neural amplifier are low power, noise rejection and smaller area. Low power and noise rejection are desired to enhance the precision of the output while a smaller area is in consideration when it is used for portable applications, requiring a miniaturized specialised integrated system with a minimum IC area. Also, the chip area and the power consumption of any neural amplifier are dependent on the design process and application. It is always desirable to have maximized on-chip functionality which is in contrast with IC die area. However, with modern circuits designs, IC fabrication technologies and highly advanced VLSI labs have made many things possible which enables designers to think innovatively which relax such trade-offs(functionality vs area, etc)from practicality point of view.

Capacitive feedback neural amplifier:



Explanation:

The topology shown above is a one with capacitive feedback ,which consists of a gain stage (which is an OTA) where the cut-off frequency is in control by the feedback & the input capacitances namely C_f and C_{in} respectively & MOS bipolar pseudo-resistors Mb_1 - Mb_2 .

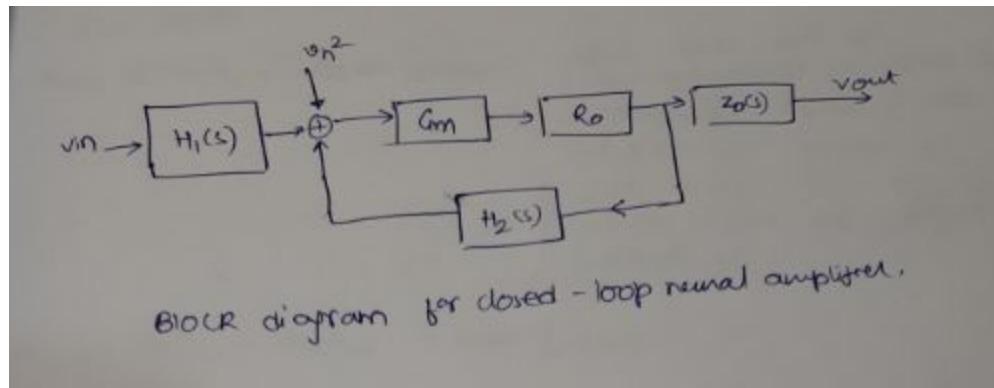
This Mos bipolar pseudo resistor can be made using two diode connected MOS transistors in series. Midband gain_(Av) for the neural amp is in control by ratio of input capacitance to the feedback capacitance, given by :

$$Av=-(\text{Input capacitance}_C_{in}/\text{Feedback capacitance}_C_f).$$

C_{in} is an AC coupling capacitor for rejection of DC offsets given by source and its value is kept large to compensate the effect of parasitic capacitors developed while C_f is acronym for feedback capacitor. This capacitor can be realized by MIM capacitor as it offers low body capacitance, high density & good linearity.

Such an arrangement enhances the performance by eradicating the noise current by gate-oxide leakages by input transistors and also it doesn't ruin the bandwidth offered by the neural amplifier with capacitive feedback.

Block Diagram representation of neural amplifier with capacitive feedback:



(wrote on notes, and took picture to show)

$H_1(S)$: It is the T.F. of input source of neural signals to the input of gain stage operational transconductance & its equation is as follows
 $H_1(s) = C_{in}/(C_{in} + C_f + C_p)$.

$GmRo$: It is the T.F. of the OTA gain stage and it signifies the net specifications achieved by the capacitive feedback Neural amp. Gm is net trans-conductance while R_o is net output resistance offered by operational transconductance gain stage .

$Z_o(s)$: It represents the T.F. of output- impedance and it is shown as $Z_o = sR_pC_L/(1+sR_pC_L)$, C_L is the load capacitance & R_p is the resistor offered by a Pseudo resistors.

$H_2(S)$: It is the T.F. for the feedback path as shown above block diagram as is given by $H_2(s) = C_f/(C_{in} + C_f + C_p)$, C_p is parasitic gate capacitance due to MOS bipolar pseudo resistor.

The overall transfer/system function equation is given as

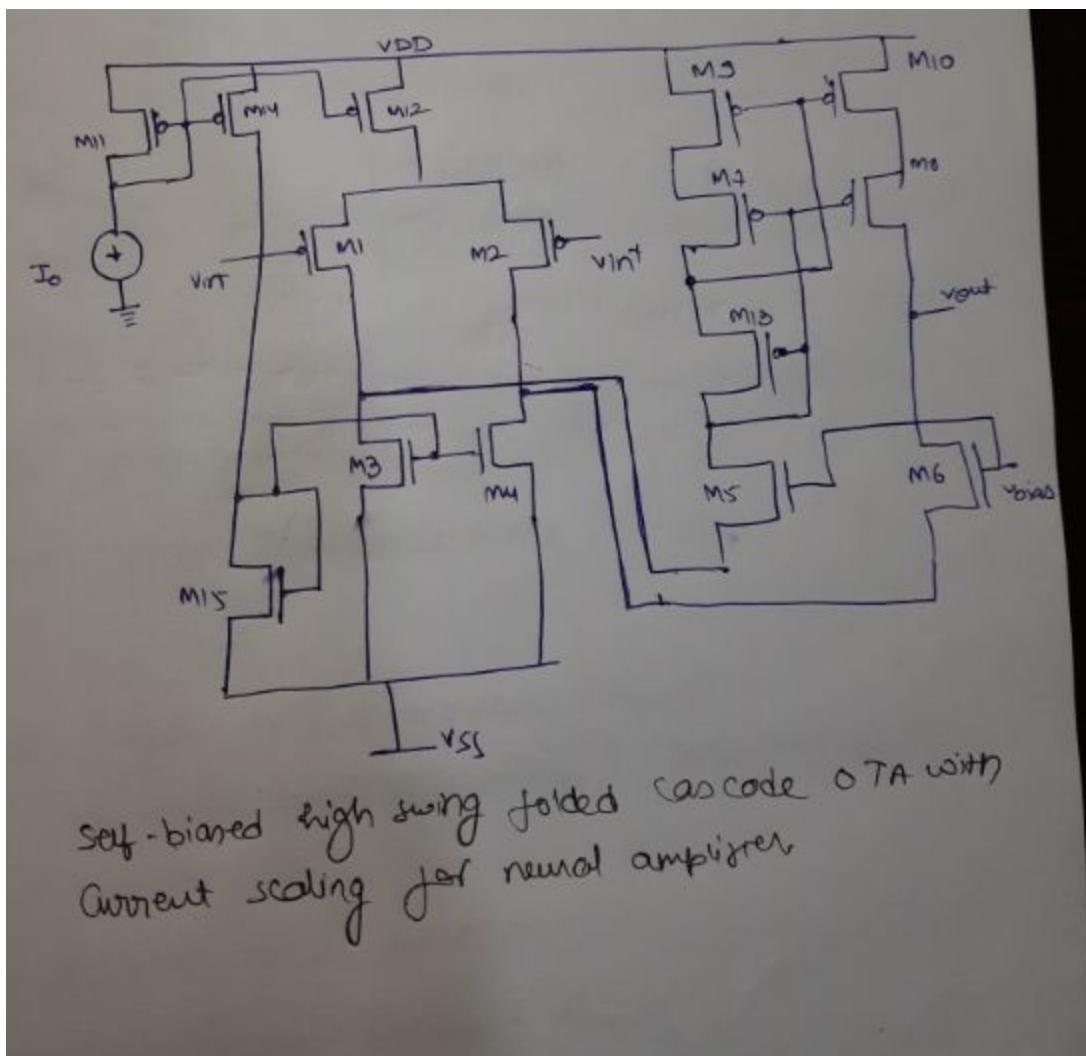
$$H(s) = V_{out}/V_{in} = -(Z_o(s) * H_1(s)/H_2(s)) = -(C_{in}/C_f) * (sR_pC_L/(1+sR_pC_L)).$$

Therefore, midband gain of the neural amp with capacitive feedback is given as $-C_{in}/C_f$.

Also, Input referred noise for this OTA is equated to Input referred noise of net capacitive feedback neural amplifier as given by $\underline{V_{n2,amp}} = \underline{V_{n2}} ((C_{in} + C_f + C_p)/C_{in})^2$

OTA:

Designing the gain stage as a capacitive feedback based neural amplifier, a different version of the known folded cascode operational transconductance amplifier has been used as shown in the schematic. The major benefit of using this folded-cascode-OTA(which offers high swing and self biased and with-current-scaling) is major improvement in noise rejection, reduced supply margins & overcoming output swing limitation.



(Schematic of OTA, drawn on notes & took picture to show)

PEN-PAPER BASIC ANALYSIS:

Sizing & other design parameters for OTA:-

$V_{DD} = 1.8V, V_{SS} = -1.8V$
 $I_D = 56mA$

$w_{L1} \leftarrow w_2/L_2 = 100\mu m / 0.18\mu m,$ since loop can't be
 size of mosfet in gmos-30
 technology, hence I used
 4 transistors instead of
 with sizing 30μm, 30μm, 30μm
 4 low each with length
 0.18μm.

$w_3/L_3 = w_4/L_4 = w_5/L_5 = 8\mu m / 0.18\mu m$

$w_5/L_5 = w_6/L_6 = 0.42\mu m / 0.18\mu m$

$w_7/L_7 = w_8/L_8 = 4\mu m / 0.18\mu m$

$w_9/L_9 = w_{10}/L_{10} = 1\mu m / 0.18\mu m$

$w_{13}/L_{13} = 10\mu m / 0.18\mu m$

$w_{11}/L_{11} = w_{12}/L_{12} = w_{14}/L_{14} = 1\mu m / 0.18\mu m$

Small signal Analysis for OTA:-

↳ small signal Transconductance = $G_{mOTA} = 8m_1$,

↳ small signal output resistance (Z_{out}) =
 $R_{ota} = g_{m1} R_{ds} \left((202) / (206) \parallel (2m_{10} r_{d10} \cdot 202) \right).$

↳ low frequency gain for OTA:-

$A_{v,OTA} = G_{m,OTA} \times R_{o,OTA}$
 $= 8m_1 2m_8 R_{ds} \left((202) / (206) \parallel (2m_{10} r_{d10} \cdot 202) \right)$

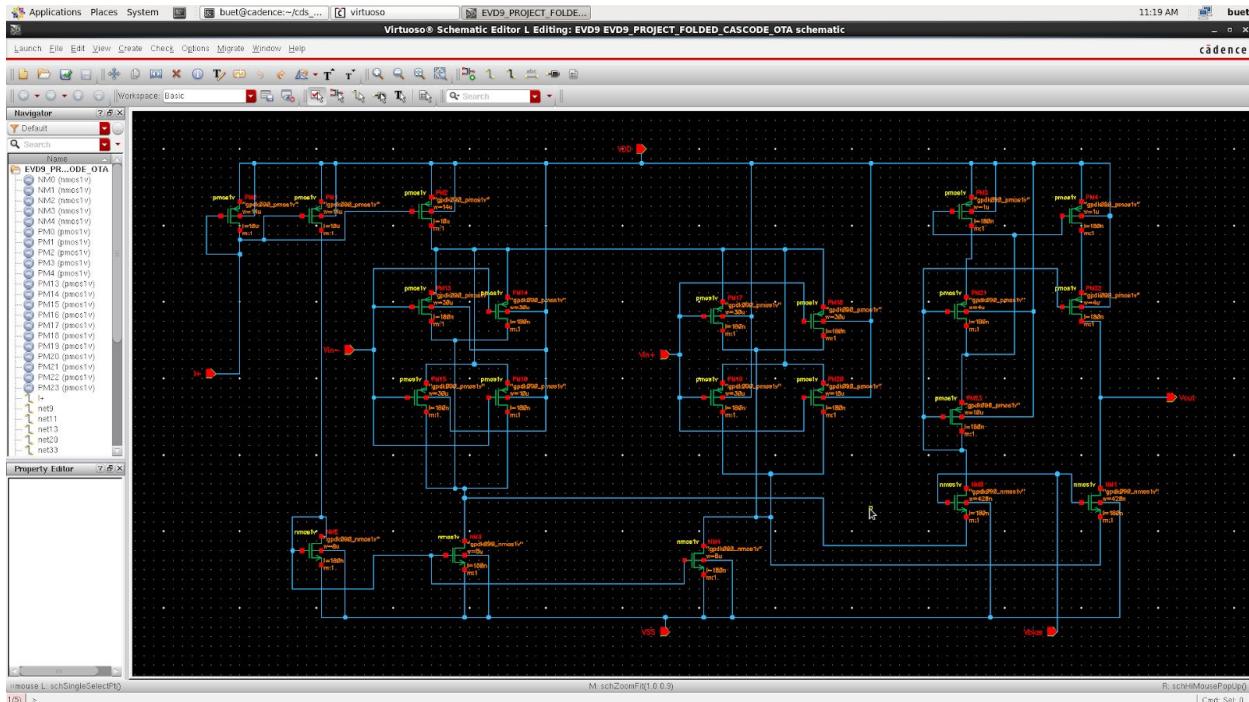
Noise Analysis:-

$V_{n,thermal}^2 = \frac{8KT}{2m^2} \left(\frac{2m_1}{3} + \frac{2m_9}{3} + \frac{2m_{13}}{3} \right)$

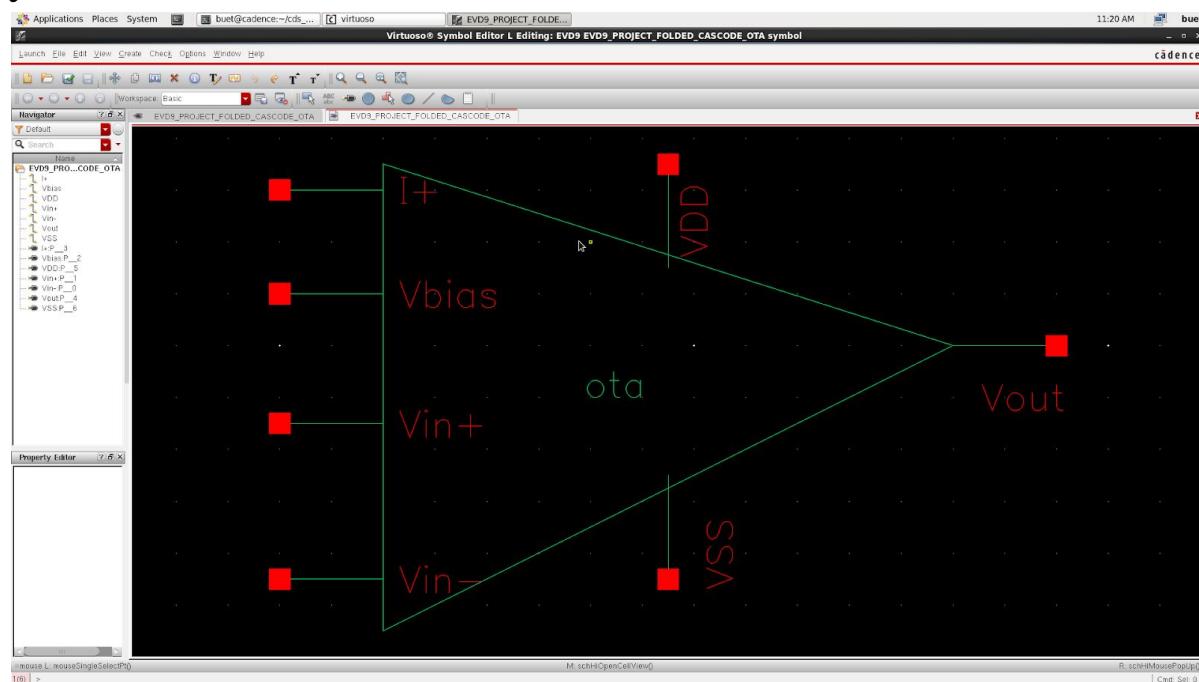
$V_{n,jitter}^2 = \frac{K_{fp}}{4pR_{ds}^2 W_{Lif}} \left[1 + \frac{2K_{fn}}{K_{fp}} \left(\frac{L_1}{L_6} \right)^2 + \left(\frac{L_1}{U_1} \right)^2 + \left(\frac{L_1}{U_3} \right)^2 \right]$

$V_{n,OTA}^2 = V_{n,jitter}^2 + V_{n,thermal}^2$

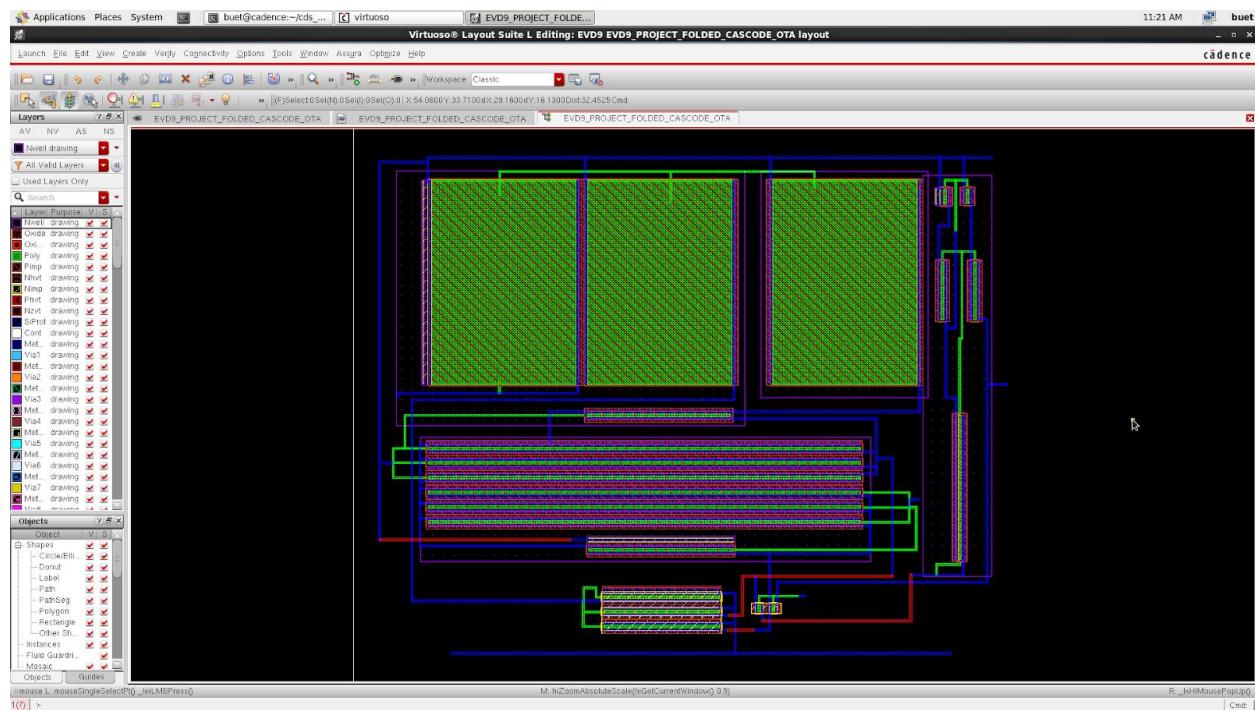
Schematic of folded cascode operational transconductance (offers high swing and self biased and with-current-scaling) for Neural Amp. :



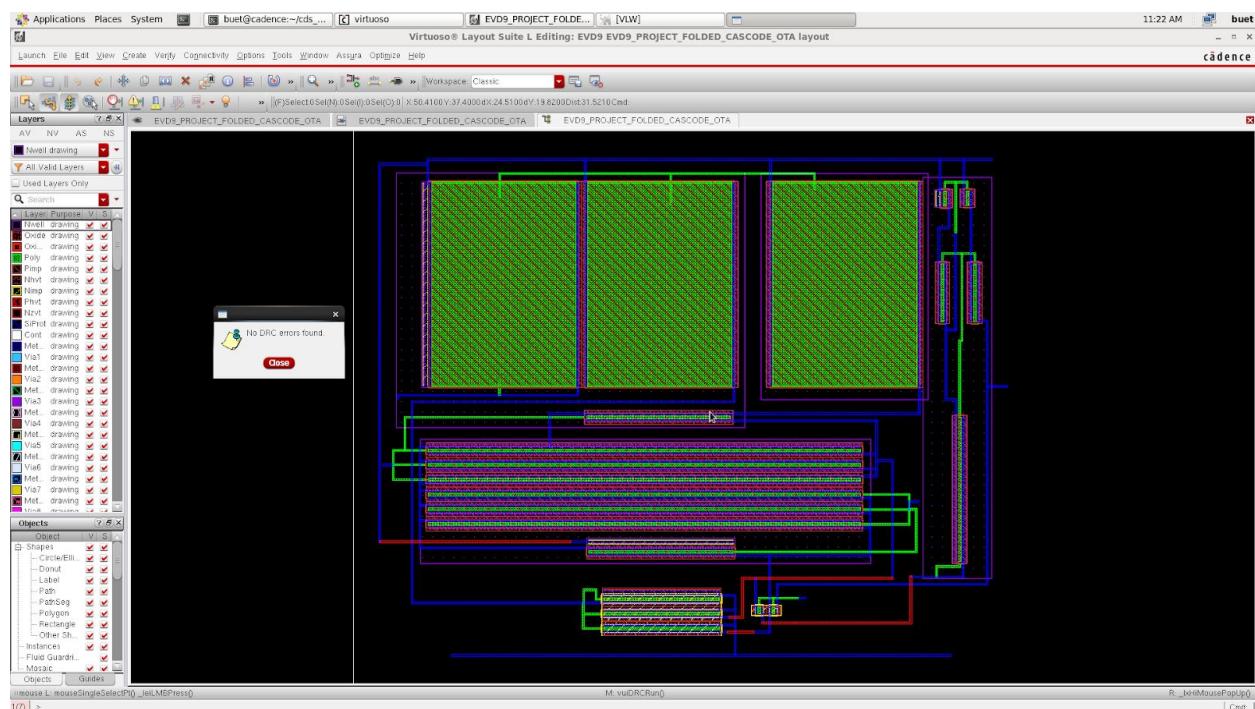
Symbol for OTA:



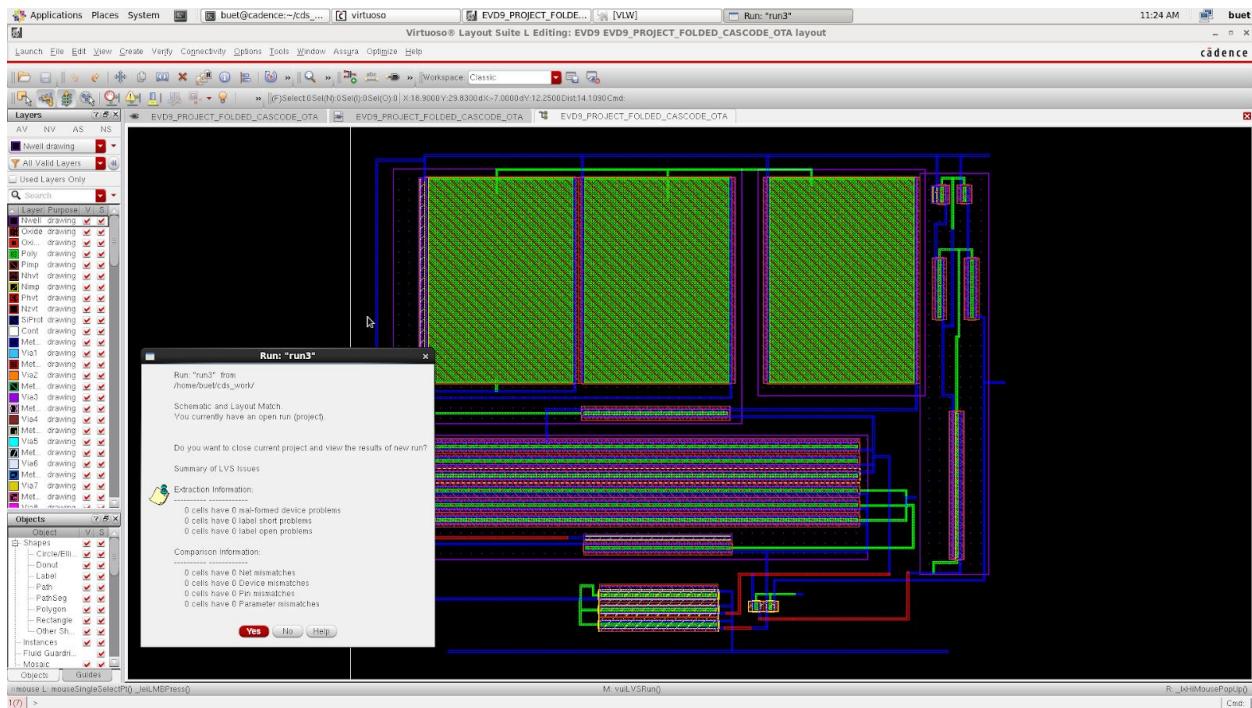
Layout of OTA:



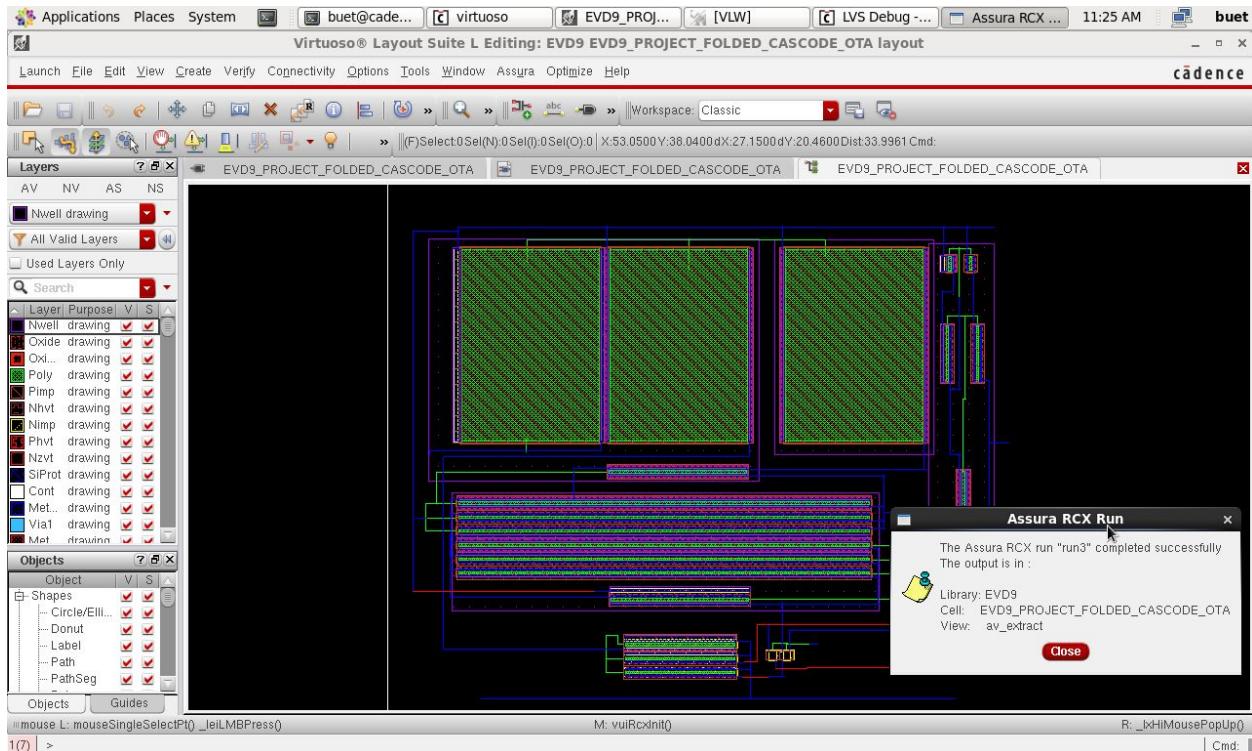
No DRC Error of OTA:



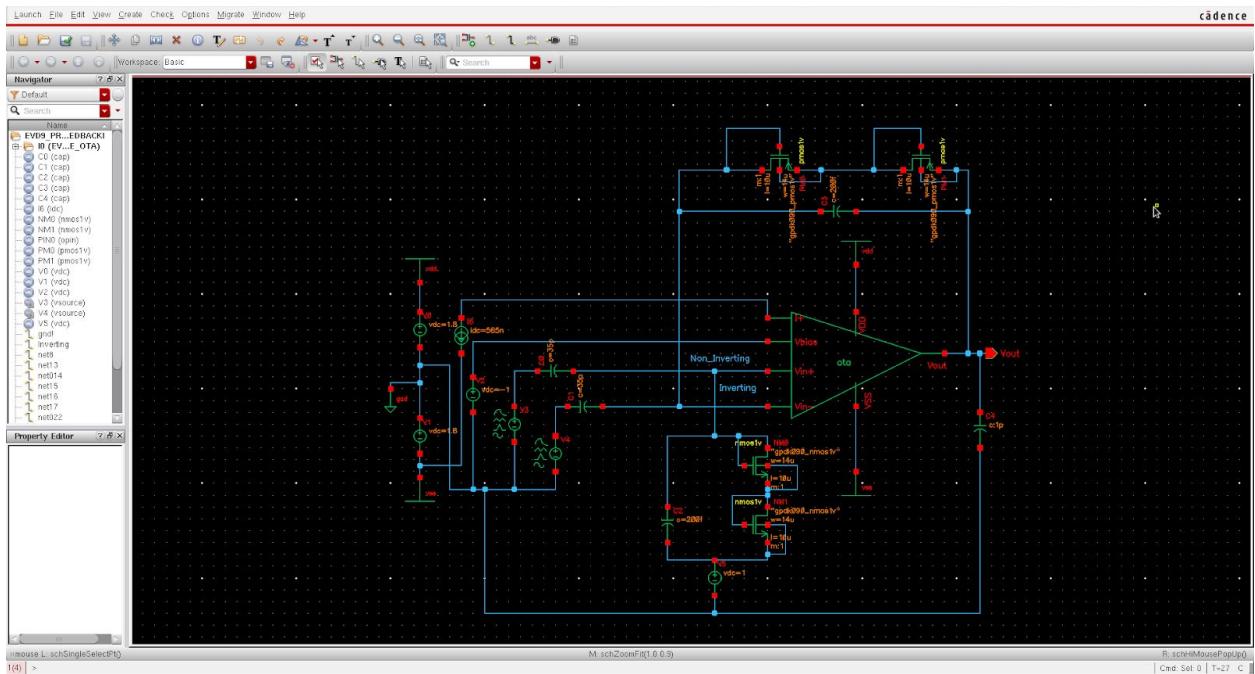
No LVS Error of OTA:



RCX Extraction/ AV Extraction:



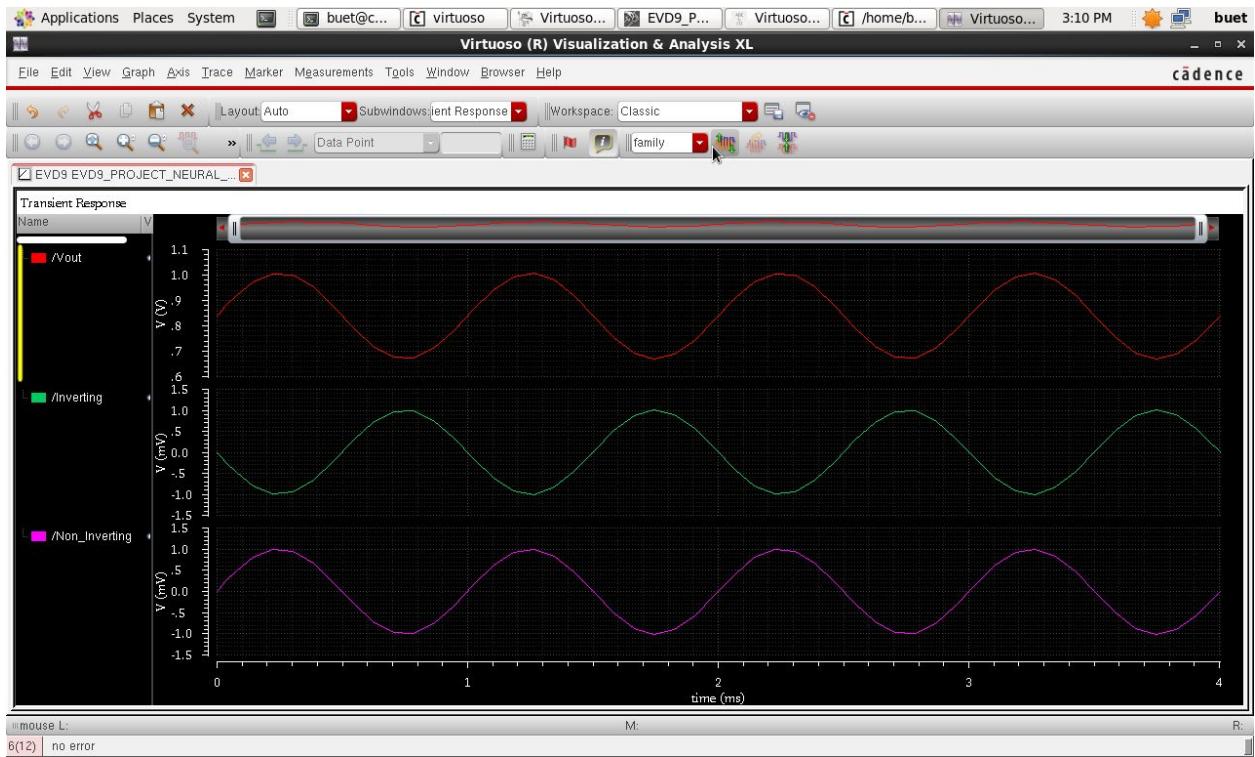
Schematic(Test-Bench) for capacitive based neural amplifier:



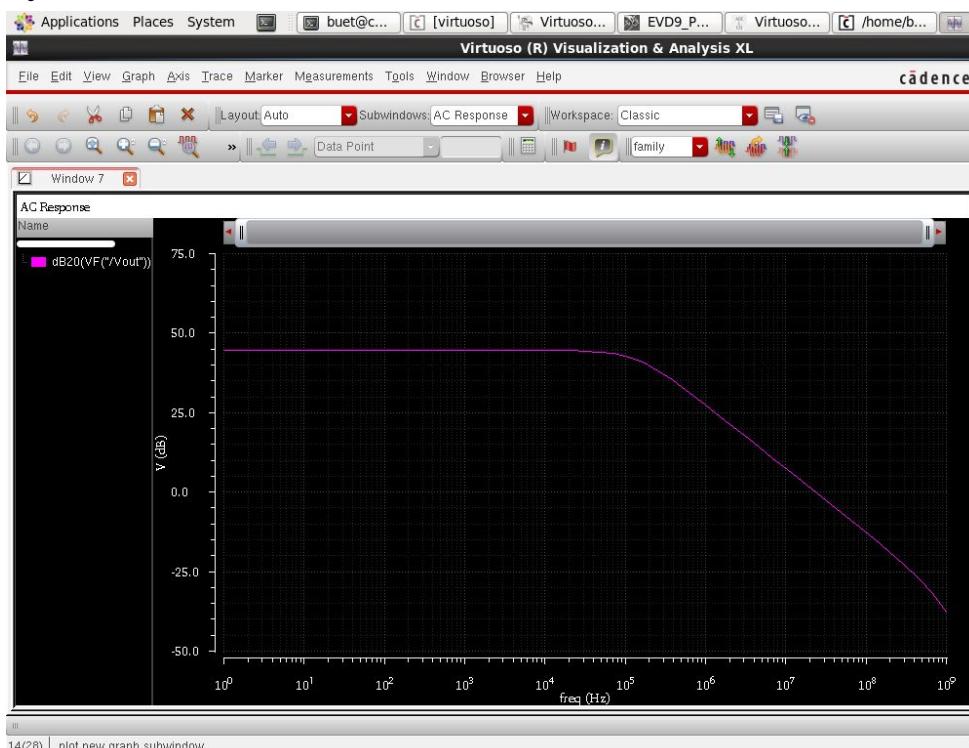
Pre-Layout simulation:

Note:

1. At the non-inverting terminal, we apply Vref and at the inverting side we should apply the Vin or input neural signal.
2. For simulation purposes, I gave input as sine and square inputs to obtain the gain and viewable transient analysis. We can give any small signal as Vin but it should be in a differential signal with respect to Vref otherwise the gain of common mode signal is very very small.
3. We also have Mos bipolar pseudo resistor, which I added **externally** in the testbench. Sizing of the pseudo resistor was achieved using a hit and trial method.
4. Generally, neural signals may not be in a properly defined known waveform like sine or square. It may look like a noise of max. Milli volt as amplitude. Hence gain and CMRR of Neural Amplifier is an important parameter. Noise is treated as common mode signals and because of this design, noise will be rejected and neural signal will be amplified only.

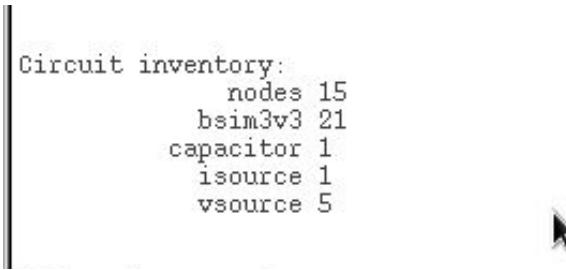


Ac -Analysis:



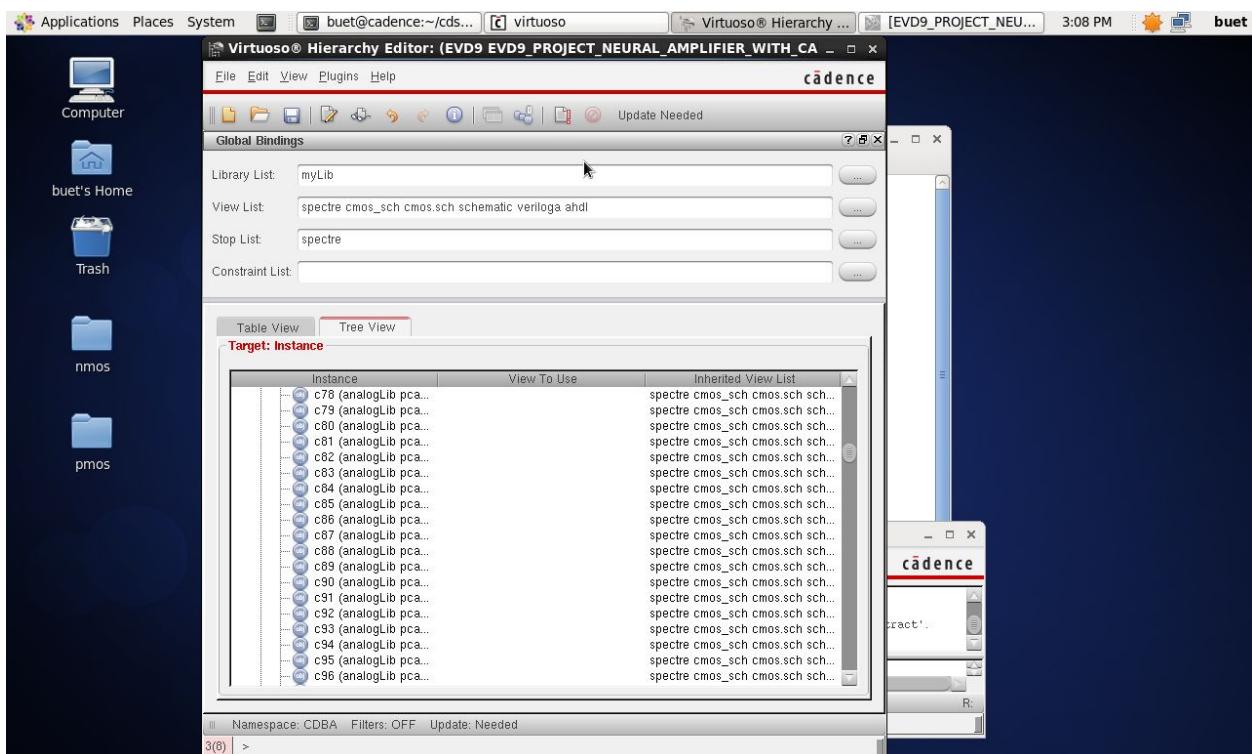
Gain for differential signal is 45dB(Pre-layout).

Pre-layout Circuit-Inventory:



```
Circuit inventory:
    nodes 15
    bsim3v3 21
    capacitor 1
    isource 1
    vsource 5
```

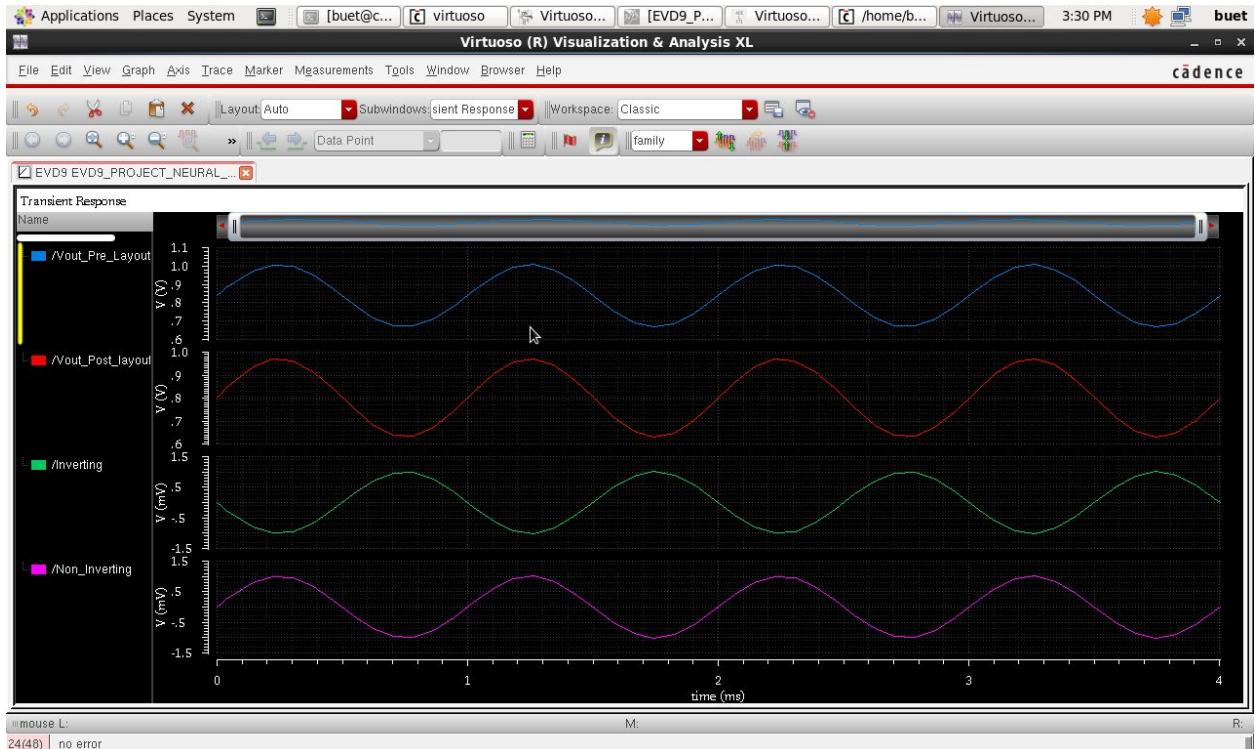
Config:



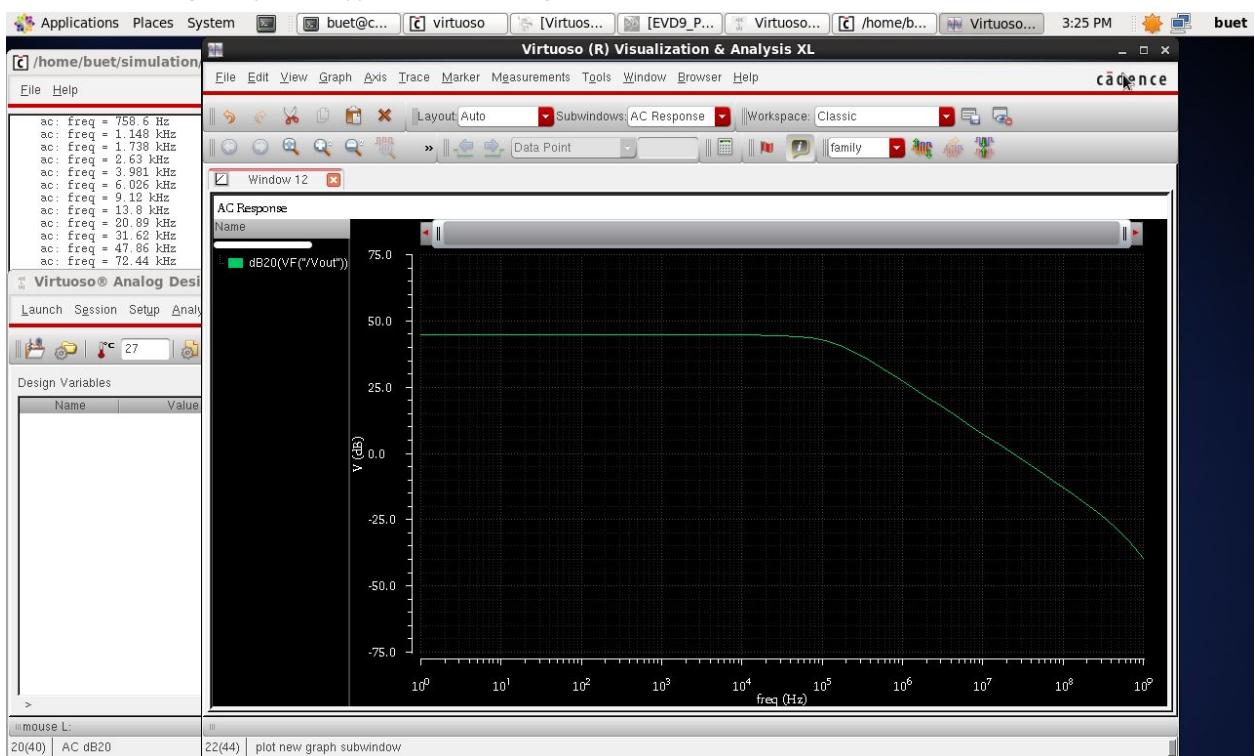
When it is kept in av-extracted view, many intrinsic capacitors and resistors come into picture. Av-extracted to schematic view can be changed in the table view and vice-versa. Av-extracted view is used for post-layout simulation.

Post-layout simulation for capacitive feedback neural amplifier:

I. Transient Analysis for Differential signalling :

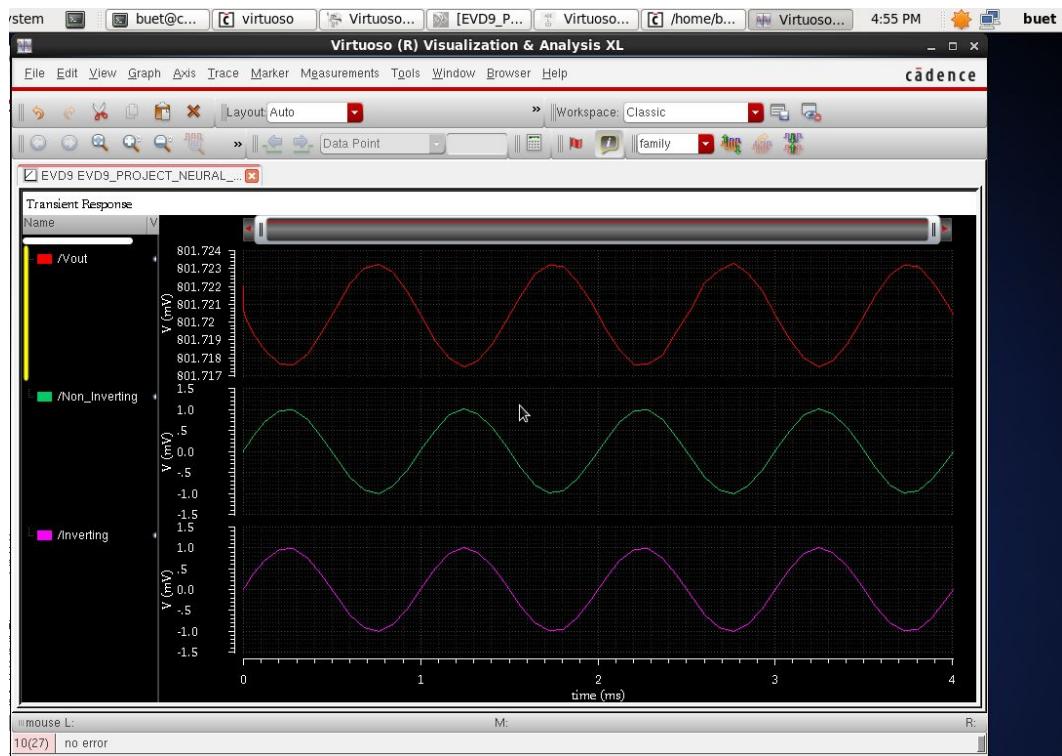


II. AC Analysis for differential signal:

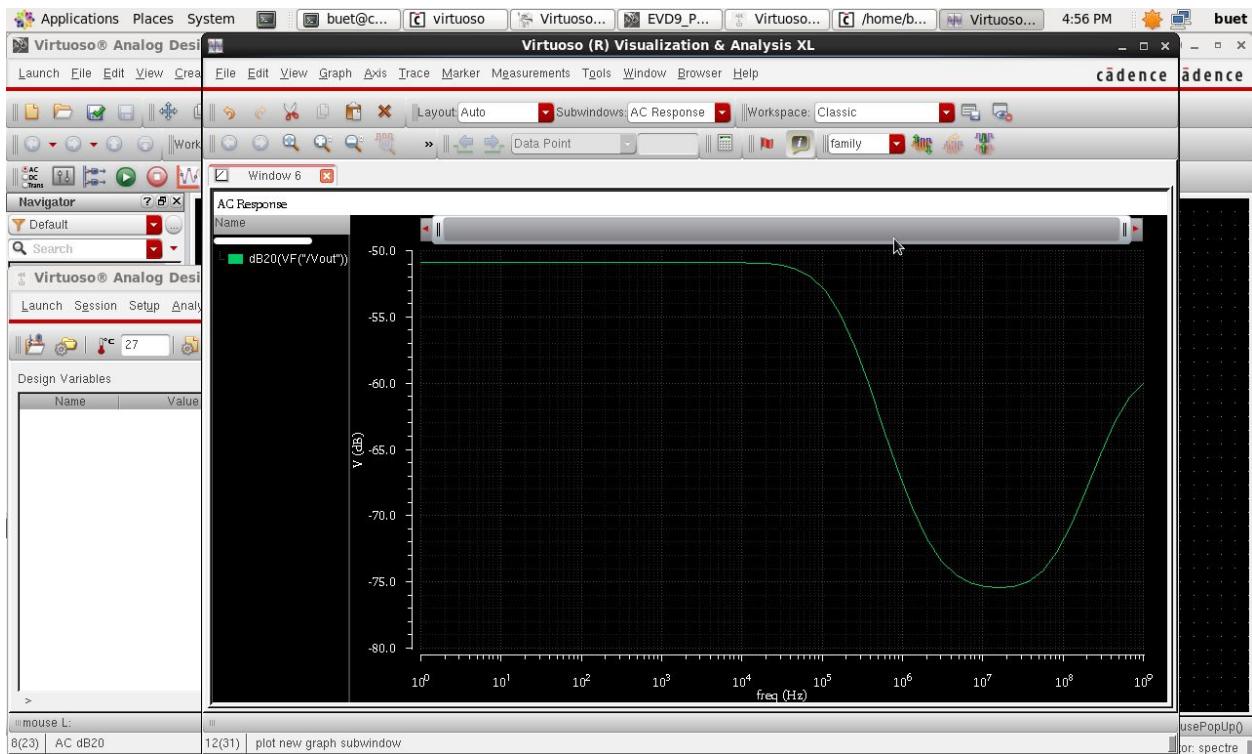


Gain for differential signal is 45dB(Post-layout).

III. Transient Analysis for Common mode signalling:

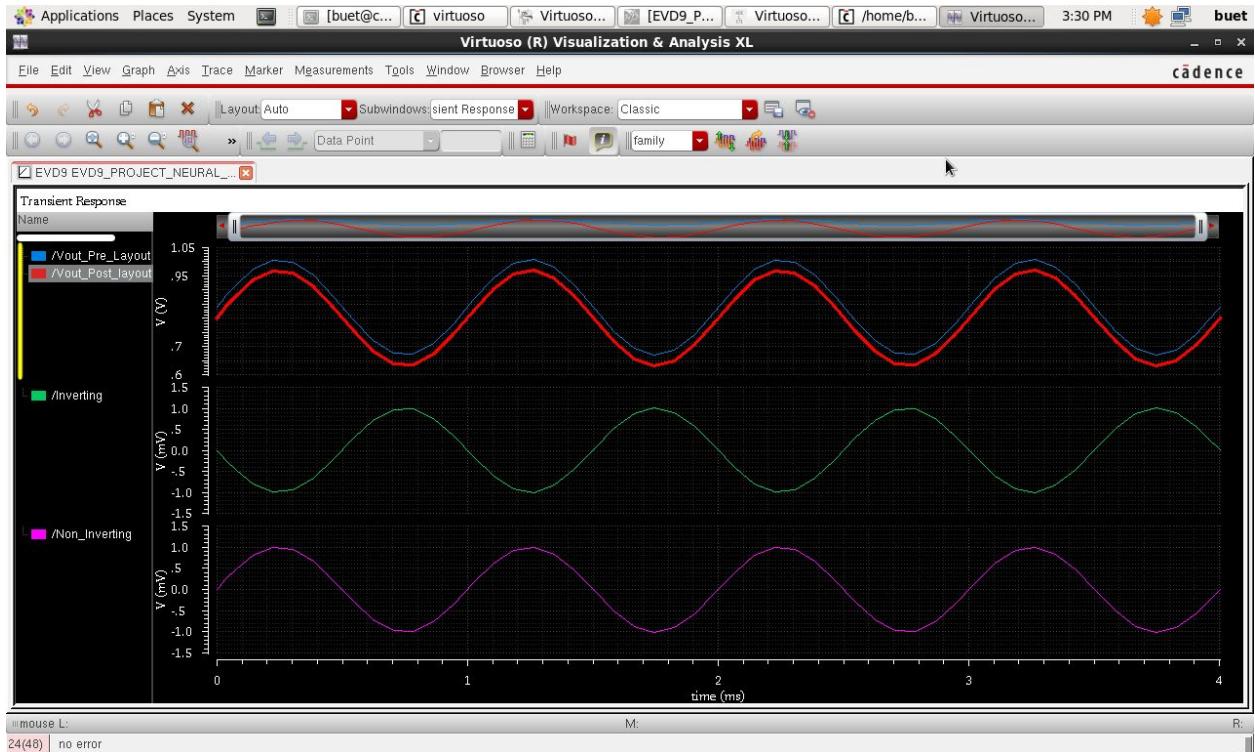


IV. AC Analysis for common mode signal:



Gain for Common mode signal is -50dB(Post-layout).

Comparison of Pre-Layout and Post-Layout Output:

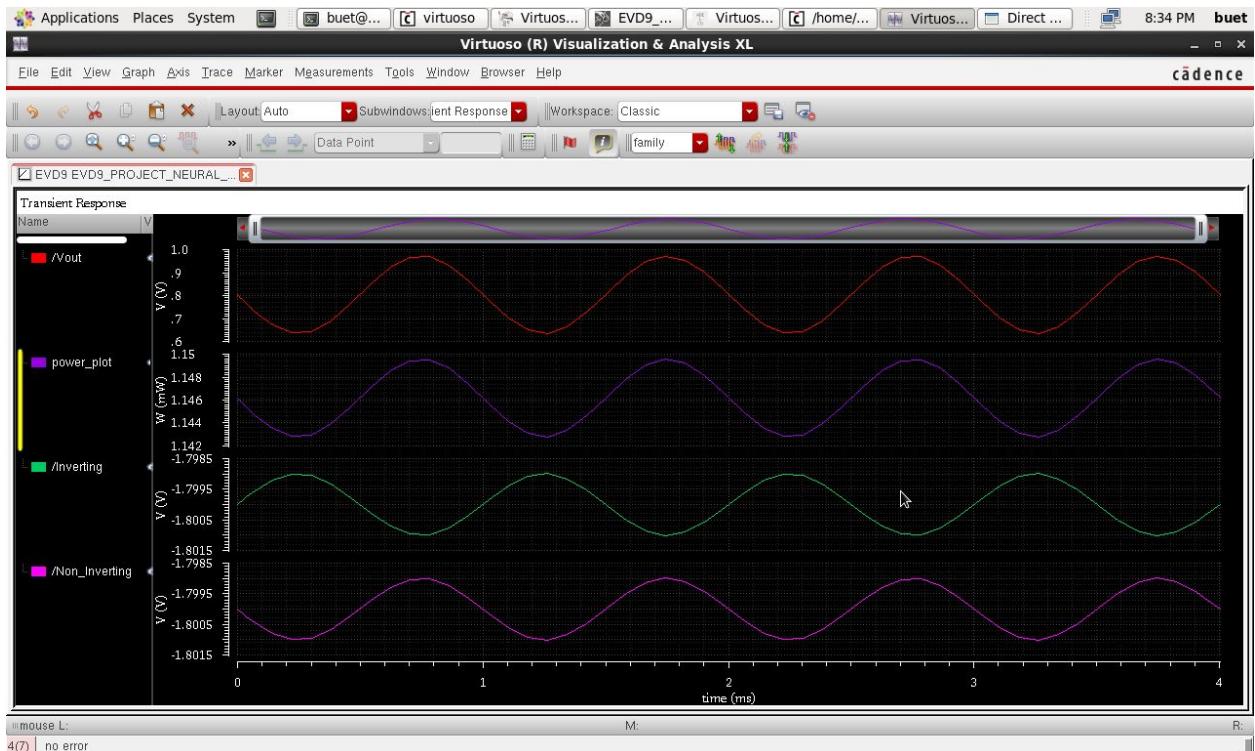


There is a dip in voltage at output while transient analysis because of resistors and capacitors developed during av-extraction.

Post-layout Circuit-Inventory:

```
Circuit inventory:  
    nodes 259  
    bsim3v3 21  
    capacitor 110  
    isource 1  
    resistor 351  
    vsource 5
```

Power Plot:



The 2nd plot shows the power plot after the post layout simulation.

CMRR:

Since $\text{CMRR} = (\text{Adm}/\text{Acm})$ or

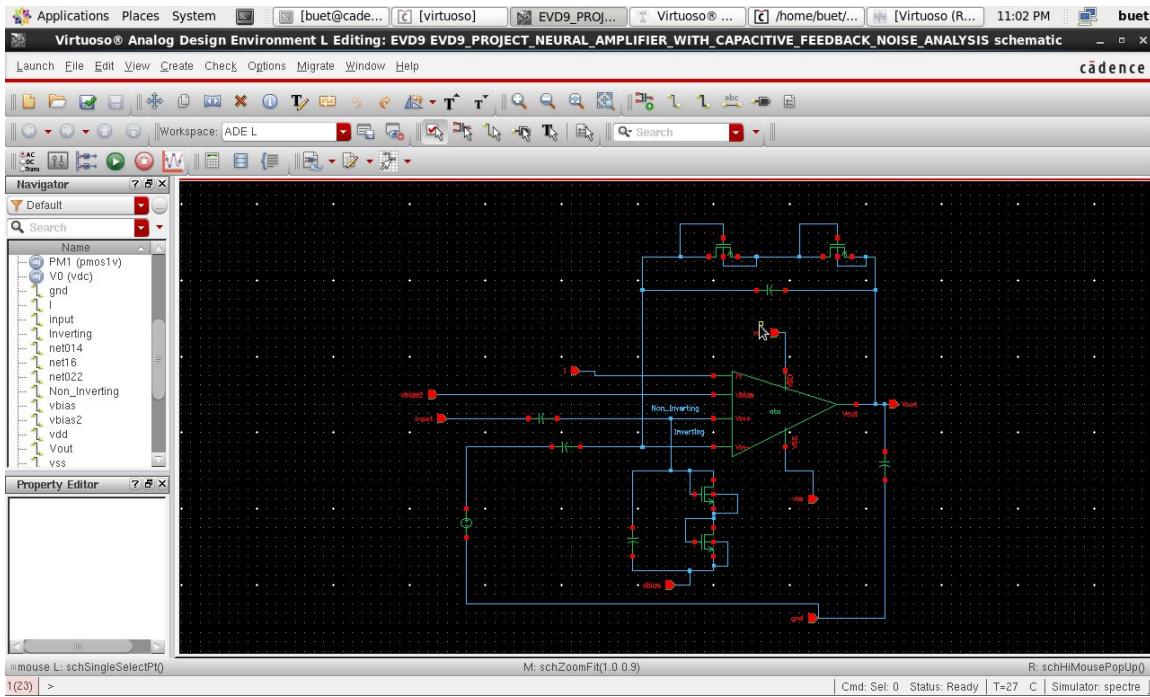
$$\text{CMRR(dB)} = 20 \cdot \log(\text{CMRR}) = 20 \cdot \log(\text{Adm}/\text{Acm}) = \text{Adm(dB)} - \text{Acm(dB)} = 45 \text{dB} - (-50 \text{dB}) = 95 \text{dB}.$$

Pole Location:

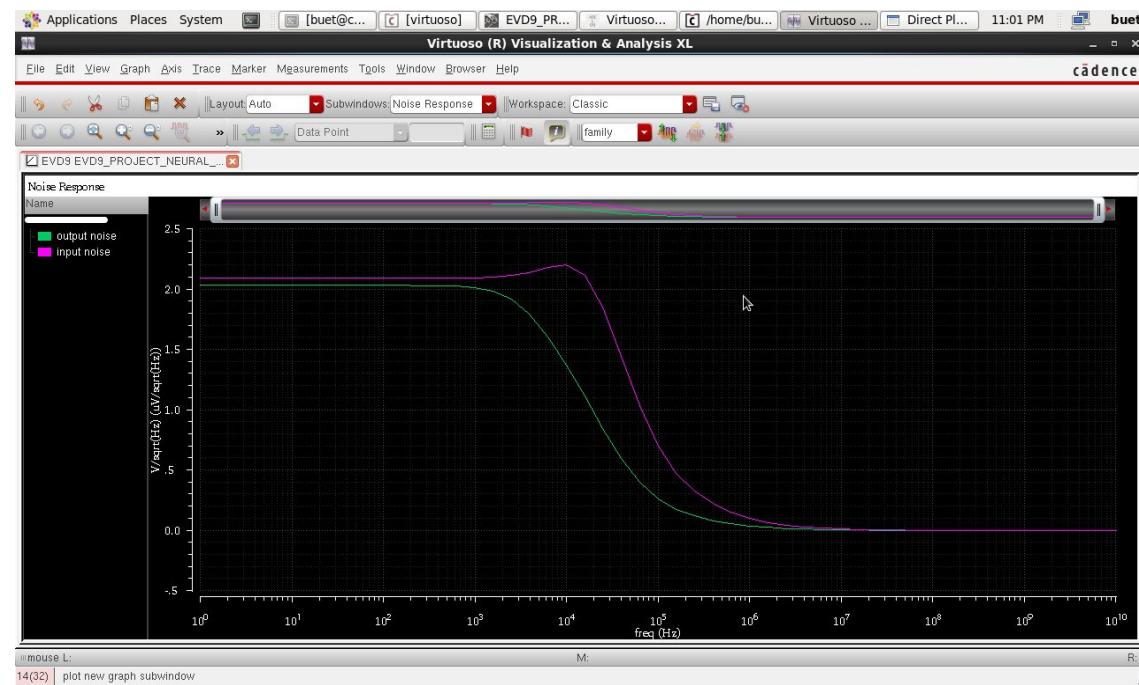
In AC-response of Differential signalling , the gain reduces to 0 at **20MHz**, realising the location of pole for this neural amplifier with capacitive feedback.

Noise Analysis: For noise-analysis, I created a separate schematic with noise input applied at Inverting & Non-inverting terminal separately to find the input-referred noise and output-referred noise in each case.

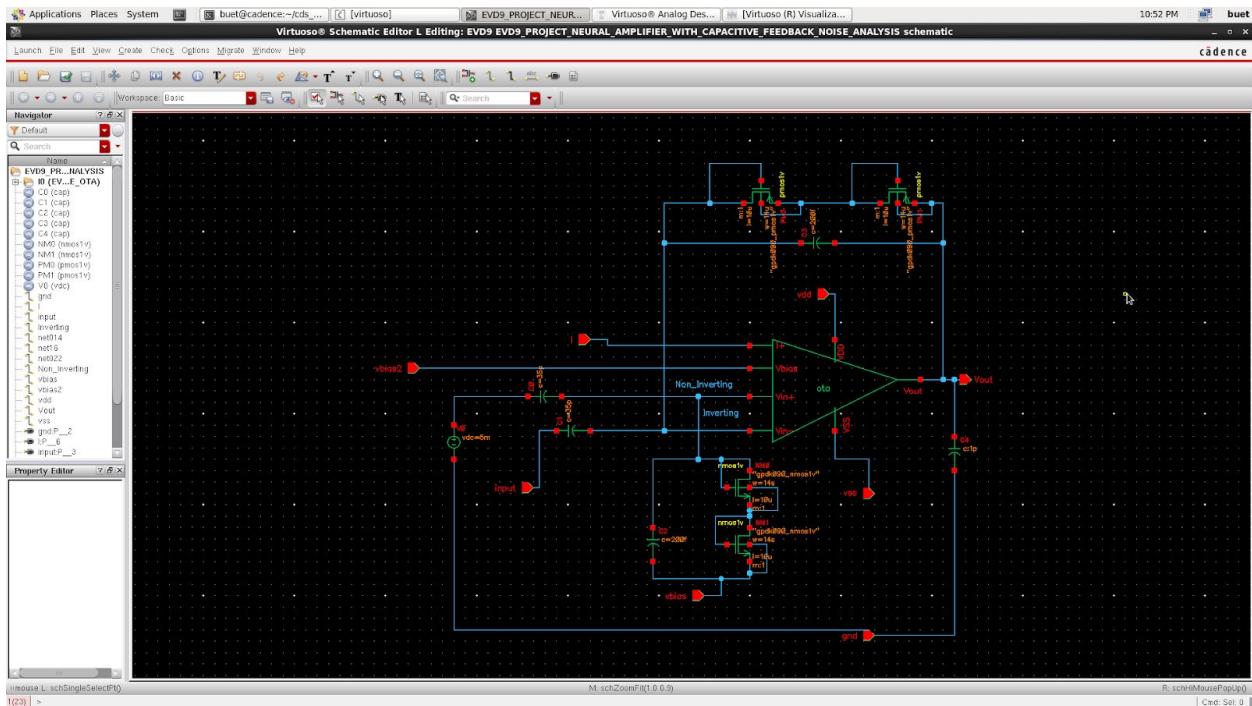
I. Schematic for the case when noise-input is applied to Inverting terminal:



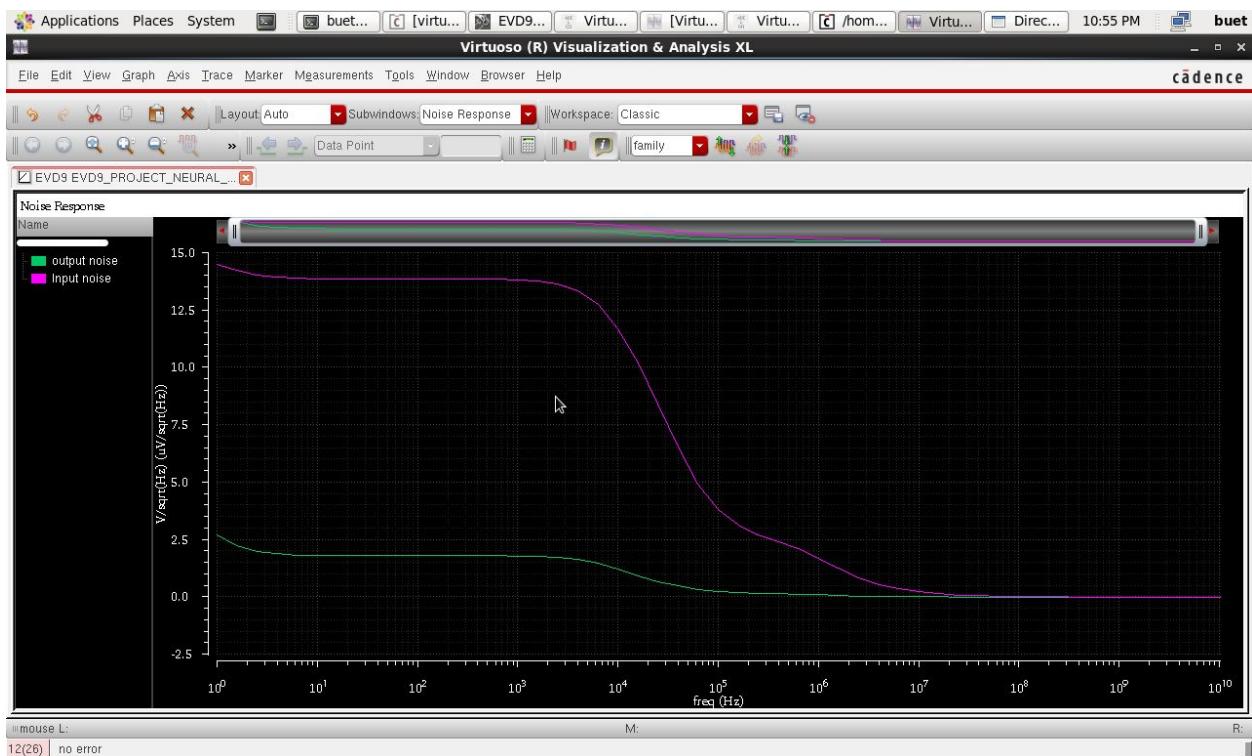
Plot:



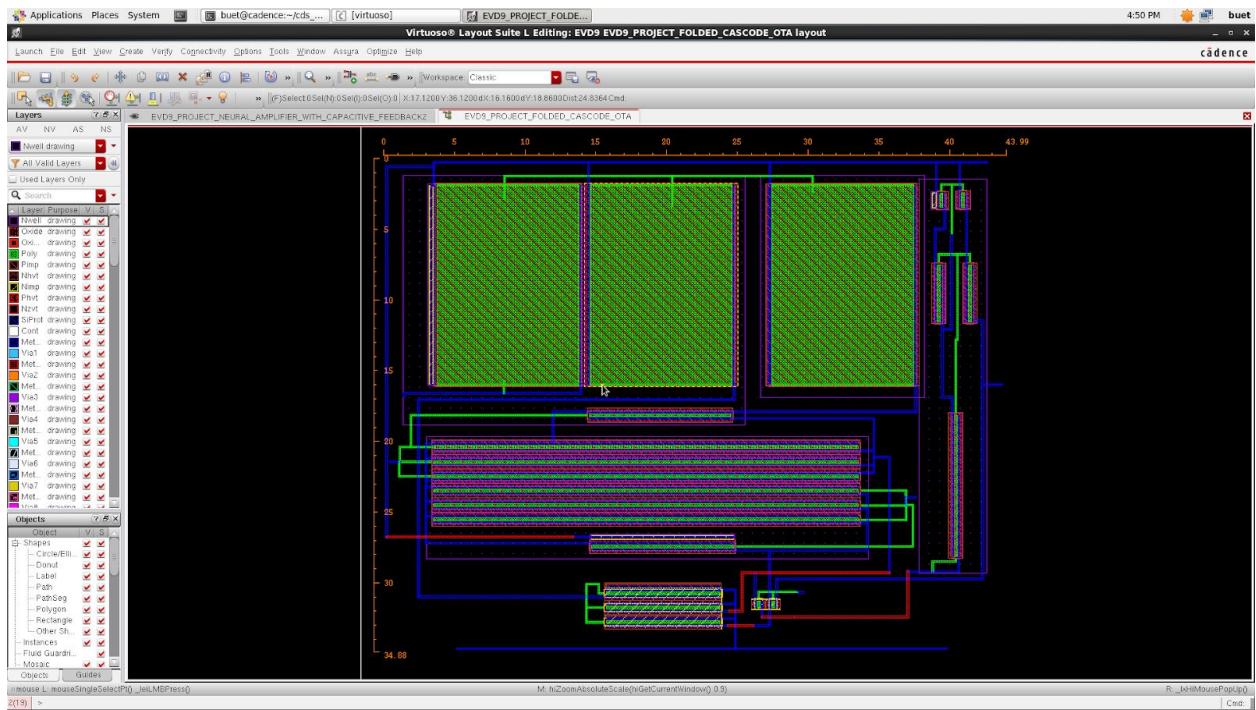
II. Schematic, when input as noise is applied to the Non-Inverting terminal:



Plot:

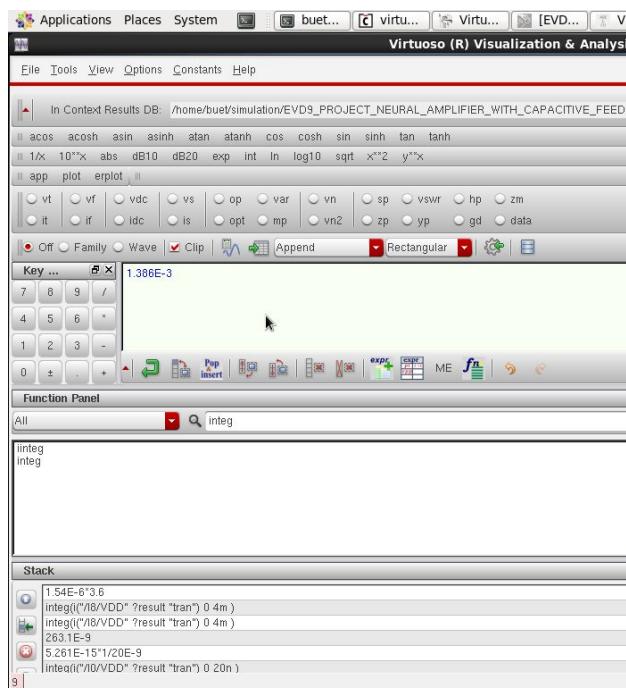


Area of the Operational transconductance amplifier-IC :



$$\text{Area} = \text{length} * \text{breadth} = 42.99 * 34.88 \mu\text{m}^2 = 1499.49 \mu\text{m}^2 = 1500 \mu\text{m}^2$$

Power Analysis:



Power dissipated is 1.38 mW.

Result:

Designed a Neural Amplifier with capacitive feedback, which gives the CMRR of 95dB, rejects the common mode signals by giving very less gain to it but enhances the gain of differential signals, also it provides good rejection to noise. It was designed using cadence-virtuoso gpdk-90.

Obtained simulation values:

Term	Value
CMRR	95dB
Diff. mode gain	45dB
Common-mode gain	-50dB
Input referred noise, from Inverting-terminal	2uV/sqrt(Hz)
Power dissipation	1.38mW
Area	1500um ²

Conclusion:

Neural Amplifier amplifies the low amplitude neural spikes while collecting the neural signals through specific recording systems. Neural amplifiers should be capable of rejecting low noise developed by the background of the recorder. Also, the constant need of having more recording sites and to avoid heating has given rise to think of miniaturised IC and low power requirements. Capacitive feedback topology is such an amplifier that fulfills both and is noise efficient as well. It uses a folded cascode operational trans-conductance(offers high swing, self bias and with current-scaling) which gives optimum performance with trade-off between noise & power. Simulation results obtained for shown above capacitive feedback *Neural Amplifier* shows an effective CMRR and significant gain for differential signalling.

References:

“Design of high gain, high bandwidth neural amplifier IC considering noise-power trade-off” by N. M. Laskar, K. Guha, S. Nath, S. Chanda, K. L. Baishnab, P. K. Paul, K. S. Rao published in Springer