POWER CONSUMPTION ANALYSIS IN STATIC CMOS GATES

Presentation by:
Dhruthi - EVD17I012
Ranjan -EVD17I009

Department of ECE
Indian Institute of Information Technology Design and Manufacturing
Kancheepuram, Tamil Nadu, 600-127

ABSTRACT:

This paper addresses the power consumption in CMOS logic gates through a study that considers the transistor network arrangement and the advance of the technology node. The relationship between charge/discharge and short-circuit dynamic power components are investigated through electrical simulations(SPICE). The static power dissipation is also analyzed. Experimental results demonstrate that dynamic power still remains the main source of consumption in standard cell designs, although the short-circuit component seems to decrease at the advancing of CMOS fabrication processes. The static power, on the other hand, keeps growing at each new technology node, becoming even more a critical challenge in VLSI design.

INTRODUCTION:

Submicrometer and nanometer technologies have brought power consumption to a special role. Some of the related problems are the heating in high-performance systems and the battery lifetime in portable applications. Due to this fact, research and engineering efforts have been made to maintain power consumption under acceptable levels over the last few decades.

There are two main ways to build power efficient CMOS circuits:

1. *THE TECHNOLOGY : includes the research on new materials, the modification of supply and threshold voltages, and the doping levels*
2. *THE DESIGN CHOICES: includes algorithms, data encoding style, the use of pipeline, parallelism, clock gating and other low power techniques.*

When different alternatives of technology nodes are not available, it is important to choose wisely the algorithms and the architecture to be used in the circuit because it is in this phase of the design flow that the most significant power savings can be achieved.

This work presents the evaluation of the impact of both topology and technology choices on power consumption of CMOS logic gates used in standard cell libraries.

PRELIMINARIES:

Power consumption in digital VLSI circuits can be basically divided into two different categories: dynamic and static power components.

1. Dynamic power occurs always when the gate output node presents a signal transitioning. It can be still separated into two types: the charge/discharge of circuit capacitances and the short-circuit caused by a finite slope of the input transition, allowing both networks to be conducting simultaneously.

1.a. The **charge/discharge** component depends on the speed of the circuit, the supply voltage and the value of the node capacitances. It can be represented as follows:

$$P_{switching}=\alpha C_{node} f V^2_{DD} \qquad (1)$$

The summation of $P_{switching}$ over all the nodes estimates the total charge/discharge power consumption of the circuit.

1.b. The **short-circuit** occurs when all devices go into saturation region, highly dependent on rise time of input. This component is less intuitive to be modeled because it depends on both the technology and the design parameters.

It depends on the threshold and supply voltages, the drive strength of the gate, the frequency of operation, the input slope, and the output load connected to the gate.

Veendrick was one of the first authors to address this issue . A closed form for a symmetric inverter with the assumption of zero load capacitance at the output was derived, although the short-circuit value is strongly dependent on the output capacitance (C_L). The Vendrick's expression to short-circuit power dissipation is the following:

$$P_{SC}=12.(V_{DD}-2V_T)3.\square.f \qquad (2)$$

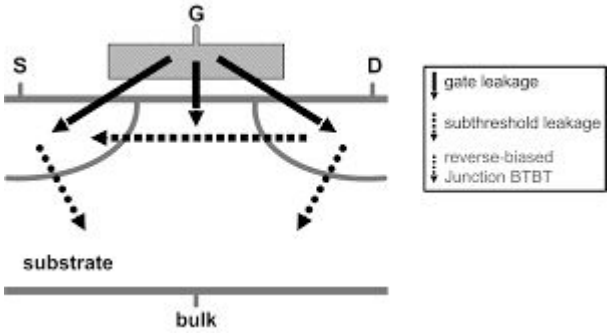
2. Static power occurs mainly due to the currents that exist when the circuit is not switching or it is in steady state. It is composed of all the undesired currents in the circuit due to the device's non-idealities i.e.

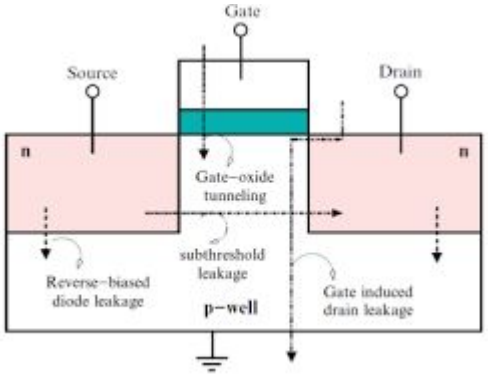
2.a Subthreshold current (I_{sub}), seen in the weak inversion operation region, which happens due to the proximity of the threshold and the V_{DD}. It is the main source of static dissipation in digital VLSI circuits and it can be modeled as follows:

$$I_{sub} = I_{off} \cdot 10^{\frac{V_{GS} + n(V_{DS} - V_{DD}) - V_{SB} k_y}{S}} \qquad (3)$$

2.b Tunneling gate oxide current, is important in technologies with the gate oxide thinner than 20 Angstroms. It occurs due to imperfections or defects in the oxide and it is important only when the logic gate has several transistors.

2.c Reverse biased junction current, Reversed biased junction currents occur due to all the reversed biased p-n junctions present in the transistors.





All these currents are due to geometry or fabrication issues. In general, in circuit design, only the subthreshold current and the gate tunneling current are taken into account on the calculation of the static power consumption.

DISCUSSION-1

INFLUENCE OF GATE TOPOLOGY ON POWER CONSUMPTION:

This section describes the effects of the circuit topology on the power dissipation of a single logic gate. A 0.35 μm commercial technology is used for modeling the transistors. First of all, the importance of the two components of the dynamic power is analyzed regarding the size of a CMOS inverter gate, as well as the input slope and the output load. Table below shows the dynamic power energy per cycle (i.e., a high-to-low and a low-to-high transitions) for a minimum sized inverter, keeping the ratio Wp/Wn = 2 in order to have a symmetric gate. The inverter is loaded by four equally sized inverters, i.e., the fanout of four (fo4) rule, and the input has a typical slope for this technology, obtained through the ring oscillator experiment.

	Energy(fJ)
Charge/Discharge	100
short-circuit	20

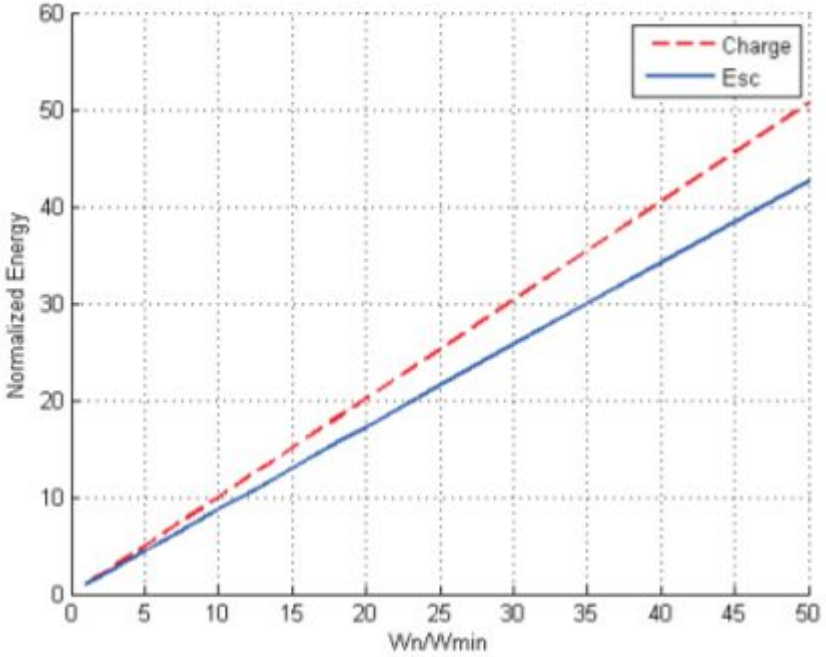
Table:Dynamic power consumption of a minimum sized inverter

The total dynamic power is calculated through the current supplied by V_{DD} over the entire cycle. When the output transitions from '0' to '1', part of the current is used to charge the capacitances, while part is wasted through the PMOS transistor as heat and through the NMOS transistor due to the short-circuit between the power lines. When the output goes from '1' to '0', the charge stored in the capacitances is discharged by the NMOS transistor while V_{DD} supplies a small amount of current due to the short-circuit.

The charge/discharge component represents actually the main source of the dynamic power dissipation.

➔ *Impact of gate sizing on power consumption*:

The size of the CMOS inverter is varied from the minimum transistor width until 50 times this value for the used technology. The inverter is loaded by the fo4 rule.



Dynamic power consumption vs inverter sizing.

It can be seen that both, the short-circuit and the charge/discharge energy components increase with the increase of the transistor width. Roughly, this can be explained as follows: the charge/discharge component is only proportional to the output capacitance. As long as the fo4 rule is used, the gate capacitance seen by the inverter output grows linearly with transistor size, as shown in equation:

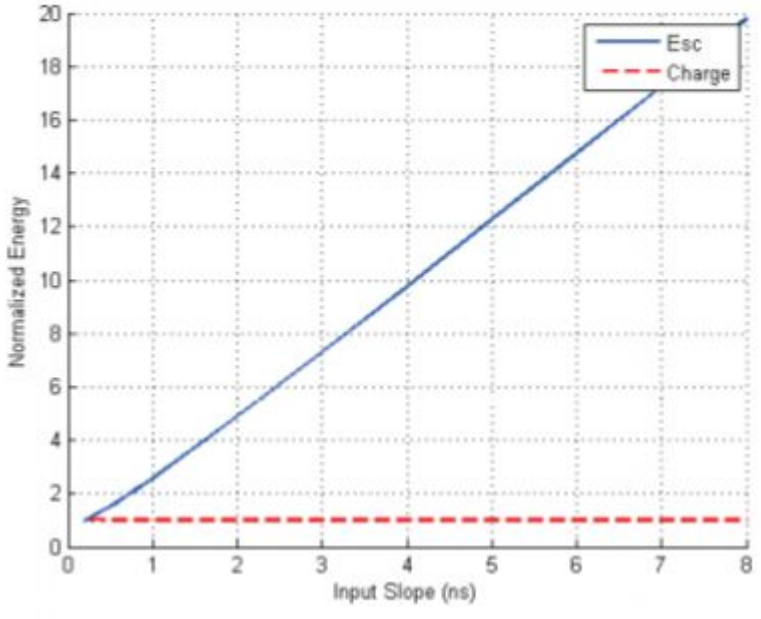
$$C_{gate}=(\varepsilon ox/tox)xWxL \qquad (4)$$

where C_{gate} is the gate capacitance, ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness, W and L are the width and length of the transistors.

It can be also seen that the short-circuit component also increases, but at a slower pace than its counterpart. As it will be explained, the short-circuit energy is inversely proportional to the output capacitance $C_{L.}$

➔ *Impact of the input slope on the dynamic power consumption*:

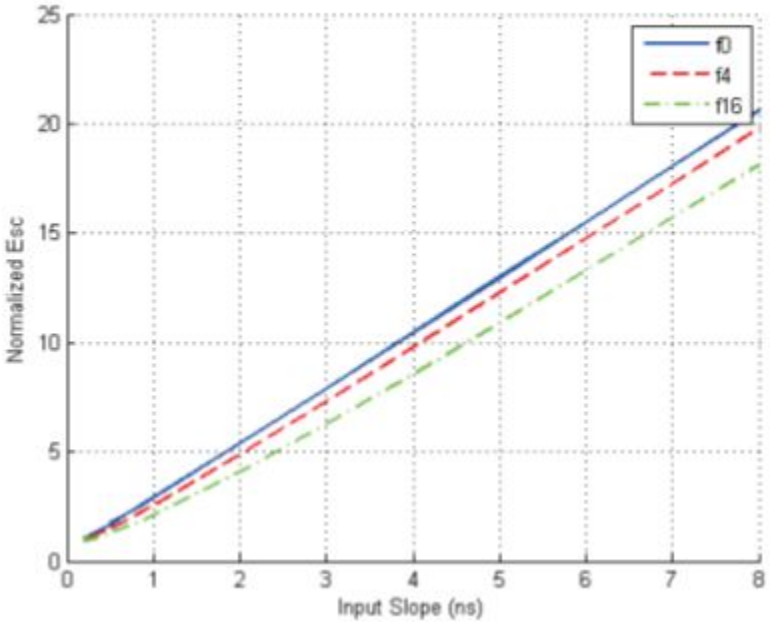
Using the minimum sized inverter loaded by the f04 rule, the transition time of Vin is varied from 200 ps until 8 ns.



Influence of input slope in the dynamic power consumption.

As depicted in Fig, the charge/discharge component (dashed line) does not change, as expected by equation (1). The short-circuit (continuous line), in turn, grows linearly with the input slope. Intuitively, it happens because the slower the input slope, the more time both networks will be ON simultaneously. When it becomes too slow, the dynamic power consumption can be dominated by the short-circuit.

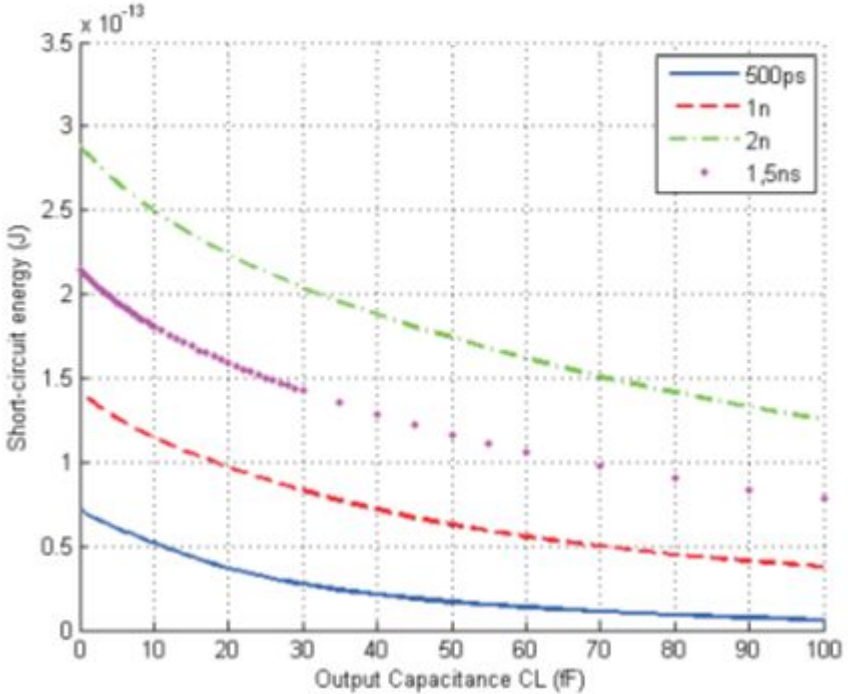
➔ ***Influence of the output capacitance on the short-circuit power dissipation of a minimum sized inverter under various input slopes*:**



As can be seen, the short-circuit augments as the output capacitance diminishes. This dependence happens because the transistor causing the short circuit begins in the linear region of operation, so its current depends on the V_{DS} of the network. If C_L is big, a large amount of charge has to be removed from the output to change the V_{DS} of the transistor, making the slope of the input faster than the output. Keeping the V_{DS} small will allow just a little amount of current to flow between the power rails. If C_L is diminished, V_{DS} will augment faster, allowing more current to be wasted between the power lines, making the output slope faster than the input. As a general rule for circuit design, it is a good guideline to try the balance between the input and output slopes at each stage. Making so, the short-circuit will remain only a fraction of the total dynamic power consumption.

Influence of output capacitance on the short-circuit power dissipation.

➔ ***The short-circuit energy as a function of CL for some arbitrary input slope***:



Short-circuit energy Vs output capacitance.

As expected, the longer the input slope, the greater the short circuit energy. For any given value of C_L, the 2 ns input slope will always have the greater power consumption. Also, the greater the output capacitance, the lesser the short-circuit energy.

DISCUSSION-2

After the CMOS inverter, NAND and NOR gates are analyzed. They present a similar behavior, caused by the stacked transistors (Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the "stacking effect" or "self reverse bias") in the pull-down and pull-up networks, respectively. It was discussed that the charge/discharge component only depends on the capacitance seen by the gate. As mentioned, the short-circuit depends on various parameters, including the position of the input transitioning.

Table below shows the normalized short-circuit for a minimum sized NOR2 gate by the logical effort method.

Input	Short- circuit- energy
A	2.25
B	1.00

The input connected to the power rail presents more than twice the short circuit of the input connected to the output node. It happens mainly due to the body effect, which can be modeled as an increase in the threshold voltage of the transistor when there is a different potential between the bulk and the source terminals. As long as transistors closer to the power rails do not suffer with this effect, it is natural that their short-circuit dissipation remains greater than the other stacked transistors because the time when both networks will be ON is greater than the other transistors in the network. The body effect can be modeled by the following equation:

$$V_T=V_{TO}+\gamma((\Phi S+VSB)^{(1/2)}-\Phi S^{(1/2)}) \qquad (5)$$

where V_{TO} is the threshold voltage when $V_{SB}=0$. γ is the body effect coefficient and ΦS is the surface potential. When there are stacked transistors in the network, they form a voltage divider, making the body effect stronger on the transistors connected on the output.

Regarding the static power consumption, Table below shows the subthreshold current for the studied gates. The size of the gates wa determined by the logical effort method using the minimum sized inverter as a reference.

Cell	Input Vector	I_{static}(pA)
INV	0	6.73
	1	7.45
2-Input NOR	00	13.5
	01	12.8
	10	7.93
	11	5.93
2-Input NAND	00	5.79
	01	7.00
	10	11.77
	11	14.91

To compare the static and dynamic power two approaches may be used.

1). To integrate the current over the period of interest and calculate the energy due to the undesired currents. For instance, switching the inverter with a frequency of 50 MHz will result in less than a hundred ato joules of energy dissipation over one cycle.

2). To compare the magnitude of the switching and static currents can also give a comparison between the two components. For this technology, the dynamic currents can reach hundreds of micro Ampères per micron of channel width. Both methods show that, for this technology, the static power consumption may be neglected in most cases.

It is observed, for the NAND and NOR gates, that when more than one transistor is OFF in the stack, the static power consumption decreases by about 30%. It is known as the stack effect, which is also due to the body effect in the transistor. Besides the body effect on the transistor connected to the output, the voltage on the intermediate node of the stack causes a negative V_{GS} and diminishes the V_{DS} of the transistor connected to the output. According to the equation (3) the subthreshold current decreases. In smaller technology nodes this effect is stronger. For instance, in a 32 nm technology the difference in the subthreshold current between a single transistor and two stacked transistors is almost 30 times, and one can take advantage of this effect to decrease the static power consumption. Although the stack effect is a very effective way of decreasing static currents, there is a tradeoff between this power component, circuit area and switching speed.

Discussion 3

Power dissipation through technology scaling:

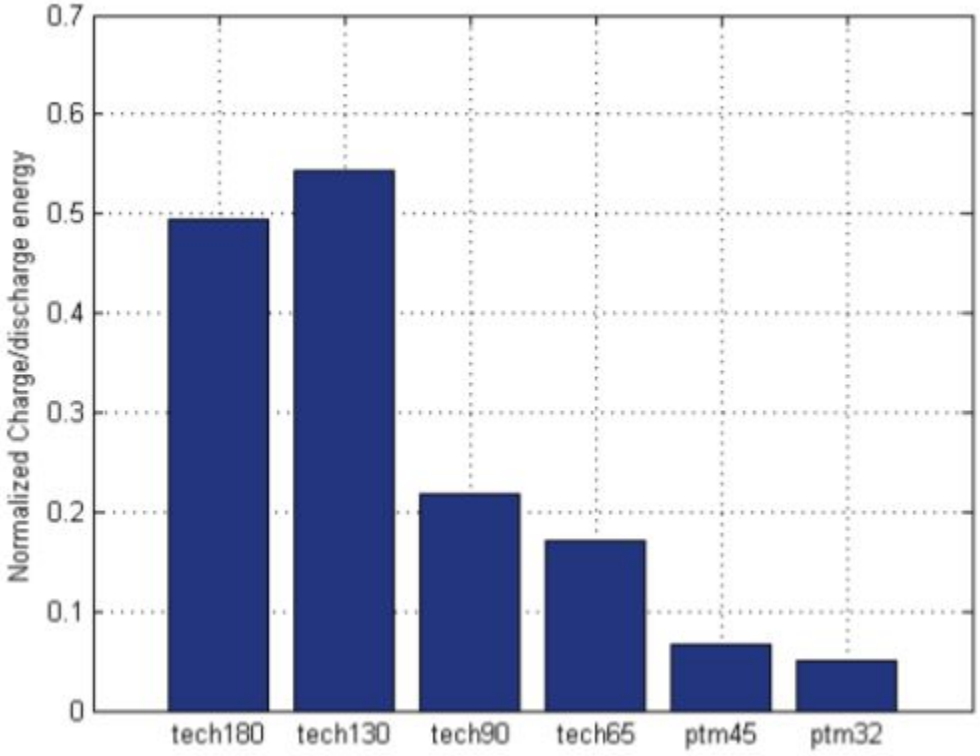
In this section, the effects of technology scaling on power dissipation are analyzed through the study of the inverter logic gate. The relation between the dynamic and static power consumption, as well as a comparison between the two components of the dynamic dissipation are presented. Using as reference the 0.35 μm technology analyzed in the previous section, power consumption is analyzed in 180, 130, 90 and 65 nm commercial technologies, besides 45 and 32 nm PTM technologies.

Table below presents the main parameters of the analyzed technologies.

Tech Node	V_{DD}	V_{Tn}	V_{Tp}	V_T/V_{DD}	L_{min}	W_{min}	t_{ox}
tech350	3.3	0.60	0.52	0.17	350	600	7.2
tech180	1.8	0.55	0.54	0.30	180	300	4.1
tech130	1.8	0.42	0.37	0.22	120	160	2.7
tech90	1.7	0.49	0.40	0.26	80	120	2.3
tech65	1.7	0.63	0.58	0.35	65	120	2.5
ptm45	1.0	0.44	0.42	0.4	50	90	1.8
ptm32	1.0	0.44	0.47	0.4	32	60	1.3

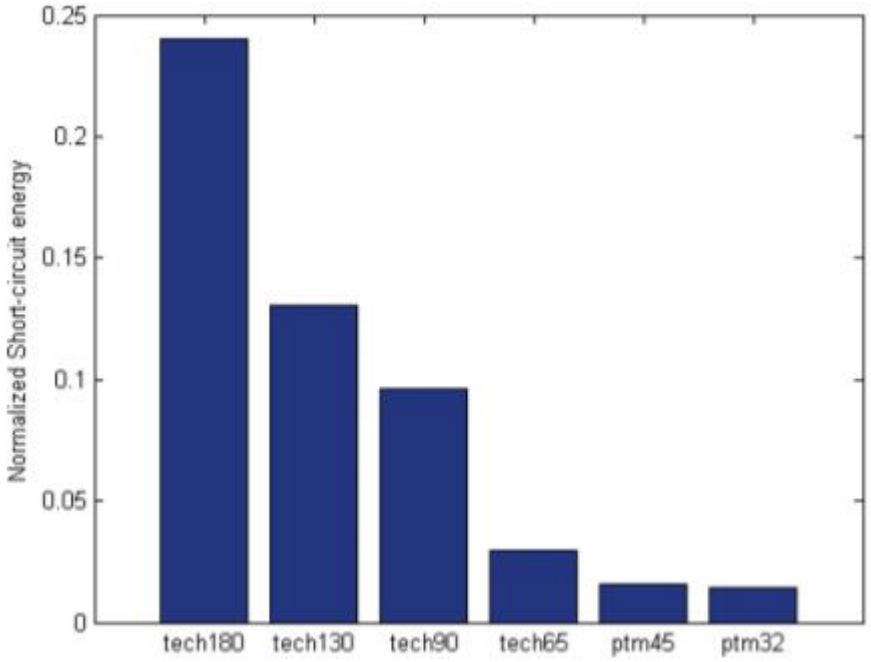
Dynamic power due to scaling:

1. **Charge/discharge component** of dynamic power consumption in the inverter logic gate through the technologies.



Shows the dynamic power consumption of a single, minimum sized inverter under a typical input slope and loaded by the f04 rule. The results are normalized in relation to the 0.35 µm technology. It can be seen that the dynamic power consumption decreases with scaling. It happens because, besides the reduction of voltage supplies, the capacitance that has to be charged decreases with smaller transistors. This result is part of the effort to maintain the power density inside a chip constant over technology scaling. Although for a single gate the dynamic power consumption decreases, the growing number of transistors in a single package makes the power density remain approximately constant.

2. Short-circuit component of a dynamic power consumption in the inverter logic gate through the technologies.



It depicts the tendency for the short-circuit component. It can be seen that this component decreases faster than the charge/discharge component. It happens mainly because of the ratio between VDD and VT. This relationship can be seen in Table IV. If it was about 0.2 in early technologies, it turns around 0.4 in modern nanometer processes. This trend happens mainly to keep leakage currents under acceptable levels, so threshold voltages cannot be decreased as fast as the power supply. VDD is decreased as fast as possible to control the total power dissipation because of its huge impact both on dynamic and static power dissipation. To keep the performance, VT must be reduced as well, but as it is known, leakage currents have an exponential dependence on this parameter. It creates a tradeoff between increasing the device's performance and maintaining undesired currents under control.

If this tendency continues in new technology nodes, the short-circuit power tends to become negligible as long as the input slopes and output capacitances remain under typical circuit conditions. It happens because if $VDD < VTn + |VTp|$ one of the networks will always be off. This condition will be reached if $VT/VDD > 0.5$.

Static power due to Scaling:

The static power consumption, in contrast, becomes a problem as transistor sizes decrease.

Tech	0.35	180	130	90	65	45	32
J_{sub}(nA/μm)	0.0087	118.5	6.1	16.9	0.6	79.6	173.9
J_{gate}(nA/μm)	0	0	0	0	0	4.4	4

STATIC CURRENT DENSITY FROM A 0.35 μM TO A 32 NM TECHNOLOGY NODES

Shows the static currents for minimum sized inverters for each of the studied technologies. As can be seen, the static current density rises from a few pA/μm in the 0.35 μm technology to more than a hundred nA/μm in the 32 nm PTM technology. As predicted, this component becomes a major problem in recent technology nodes. Subthreshold currents grow nearly exponentially, while gate currents begin to appear in nanometer devices, below 90 nm technology nodes. To alleviate the problem of gate current, high-K(dielectric constant) materials began to be introduced in modern CMOS processes. Besides, it is well known that in recent technology nodes the static power dissipation is no longer a negligible part of the total power budget. In fact, this is a major challenge for the future of CMOS integrated circuits.

FINAL ANALYSIS AND CONCLUSION:

The two components of power dissipation, dynamic and static, were analyzed.

The dynamic consumption still is the dominant component in power dissipation, mainly due to the charge/discharge of circuit capacitances. The short-circuit component only becomes a problem when the gate is submitted to large input slopes and/or small output loads. In such cases, the short-circuit may become the main part of the dynamic consumption. This is not a common situation in CMOS digital circuits. Besides, the trend found in recent technology nodes of reducing power supply faster than the threshold voltages may indicate that this component will lose importance in future technologies since in the case that $V_{DD} < V_{Tn} + |V_{Tp}|$ the short-circuit no longer exists.

The static power consumption, in contrast, keeps growing with each new technology node. Although transistors have always been imperfect switches, the constant increase in the number of transistors in a single package along with the severity of these imperfections in submicrometer devices makes this component of dissipation no longer negligible. Both, the subthreshold and gate currents increase exponentially with transistor scaling although gate currents seem to be under control due to the insertion of high-k materials on the gate oxide, and other parasitic currents are becoming more important due to the new effects presented by the different fabrication methods. Effort will have to be made to overcome these problems, both in design techniques like power efficient architectures and technology issues like the introduction of new materials to control these undesired currents.

REFERENCES:

1. This whole presentation work is adopted from : https://www.sci-hub.tw/10.1109/SBCCI.2013.6644863
Already done and concluded by Alberto Wiltgen Jr., Kim A. Escobar, André I. Reis , Renato P. Ribas Institute of Informatics, Federal University of Rio Grande do Sul – UFRGS, Porto Alegre, Brazil {awjunior, kaescobar, andreis, rpribas}@inf.ufrgs.br. They are acknowledge by Research partially supported by Brazilian funding agencies CAPES, CNPq and FAPERGS, under grant 11/2053-9 (Pronem).

2. A. P. Chandrakasan, S. Sheng and R. W. Brodersen, “Low power CMOS digital design”. IEEE J. Solid State Circuits, Vol. 27, pp. 473- 484, Apr. 1992.

3. Predictive technology model

4. J. M. Rabaey, A. P. Chandrakasan, B. Nikolic, “Digital Integrated circuits: a design perspective”. Upper Saddle River, N. K.: Pearson education, 2003.

5. P. F. Butzen, L. S. da Rosa Jr., E. J. D. Chapetta Filho, A. I. Reis and R. P. Ribas, “Standby Power Consumption Estimation by Interacting Leakage Current Mechanisms in Nanoscale CMOS Digital Circuits”. Microelectronics Journal, V. 4, pp. 247-255, 2010.

6. N. H. E. Weste and D. M. Harris, “CMOS VLSI Design: A circuits and systems perspective”. Addison-Wesley, 2011.

Thank You

For your support