SPI PROTOCOL

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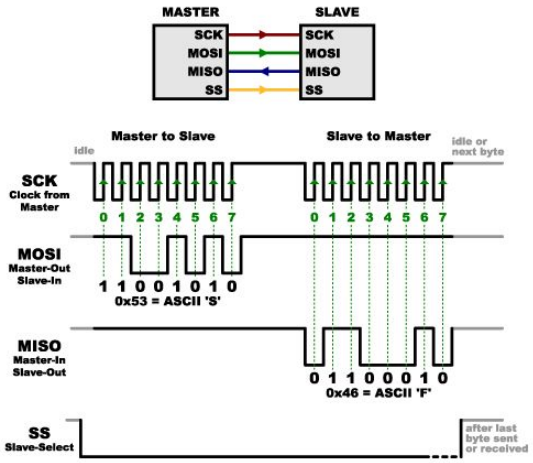
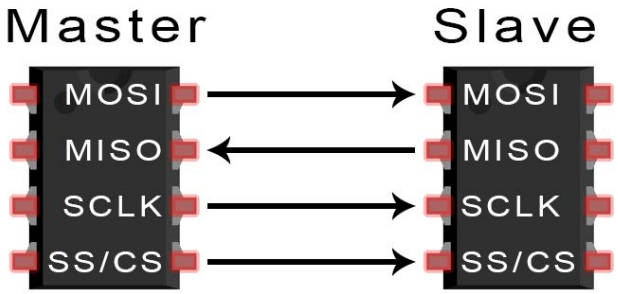
I intend to work on to demonstrate the SPI protocol with 8-bit data transfer with chip or slave select for 1-Master and 1-slaves system using system verilog.

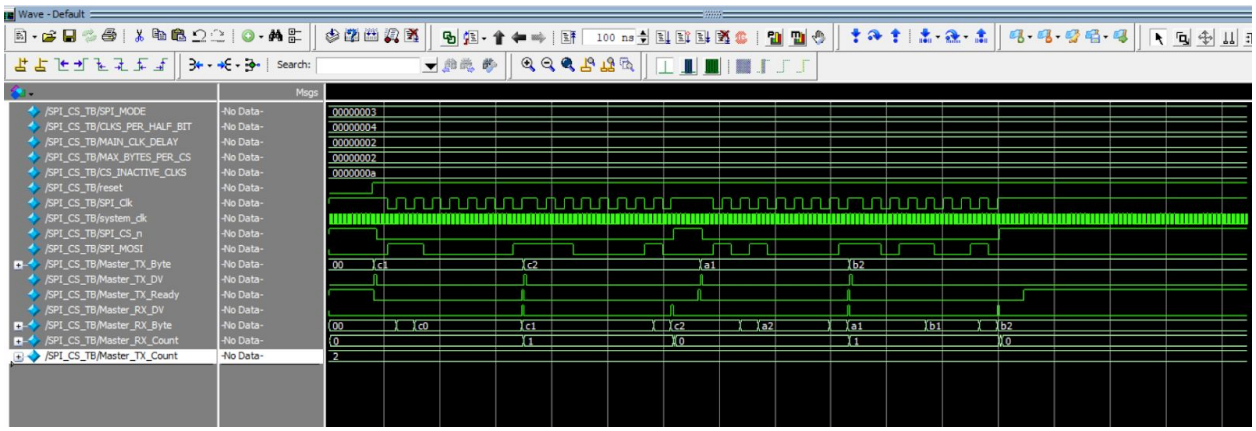
Basic description:I have implemented the SPI protocol ***with chip select or slave select*** for this week , it means it has one slave only and master has access to control over the data transfer to slave but at the same time slave can also send 8-bit data to master, hence it is full duplex communication. I also tried to implement the CPHA & CPOL and the output for MODE =1 & 3 is coming fine but for 0 & 2 last bit is missing in serial communication due to precision at timing waveform, even though the code is running fine for 2-Modes which makes it complete for data transfer as only 1 mode out of 4 should be present in hardware and 2 are working for me , hence it is achieved.





Results: Demonstrated the SPI protocol using System Verilog as HDL and simulated it for various cases to verify it and found the output correctly with chip select this time which enables the slaves to send multiple byte data to master .

Screenshots:



This is output when MOSI & MISO are shorted(above)

```
VSIM 20> run -all
# Sent out 0xc1, Received 0xc1
# Sent out 0xc2, Received 0xc2
# Sent out 0xa1, Received 0xa1
# Sent out 0xb2, Received 0xb2
# ** Note: $finish    : C:/Users/ranjan yadav/OneDrive/Desktop/DSTTD LAB/SPI PROTOCOL/SPI_CHIP_SELECT/SPI_CS_TB.sv(83)
#    Time: 1646 ns  Iteration: 1  Instance: /SPI_CS_TB
# 1
# Break in Module SPI_CS_TB at C:/Users/ranjan yadav/OneDrive/Desktop/DSTTD LAB/SPI PROTOCOL/SPI_CHIP_SELECT/SPI_CS_TB.sv line 83

VSIM 21>
```

Remarks(if any): Finished the SPI Protocol.