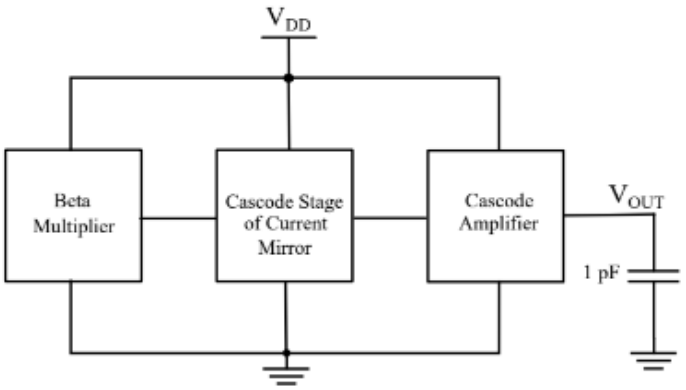
EE301 - Analog Circuits Course Project

Design of Beta Multiplier, Cascode Current Mirror and Cascode Amplifier for the given specifications for

180 nm (Schematic and Layout) and 22nm(Schematic only)



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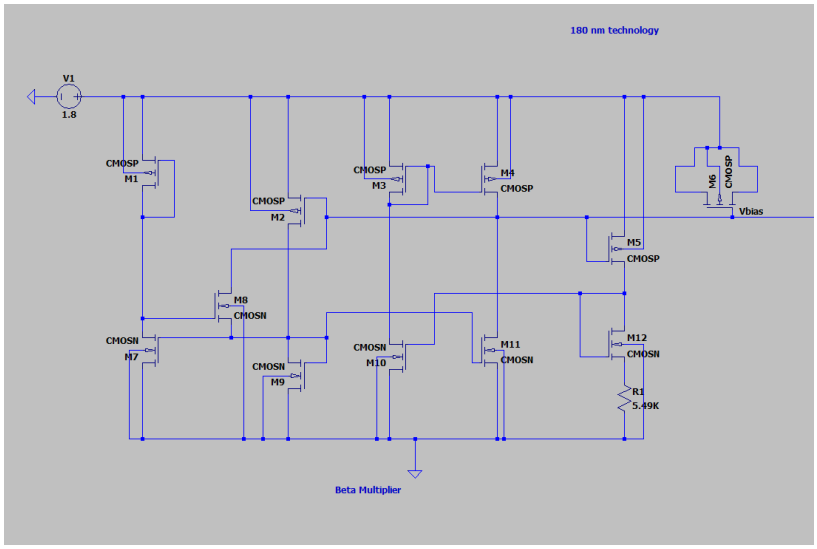
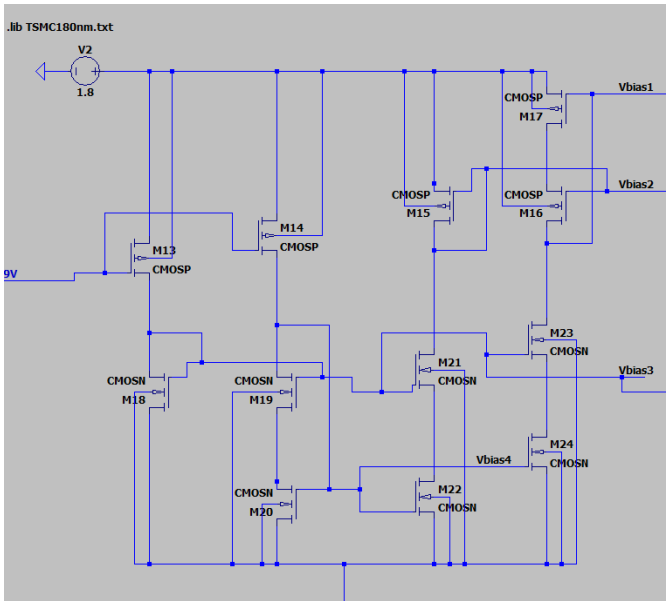
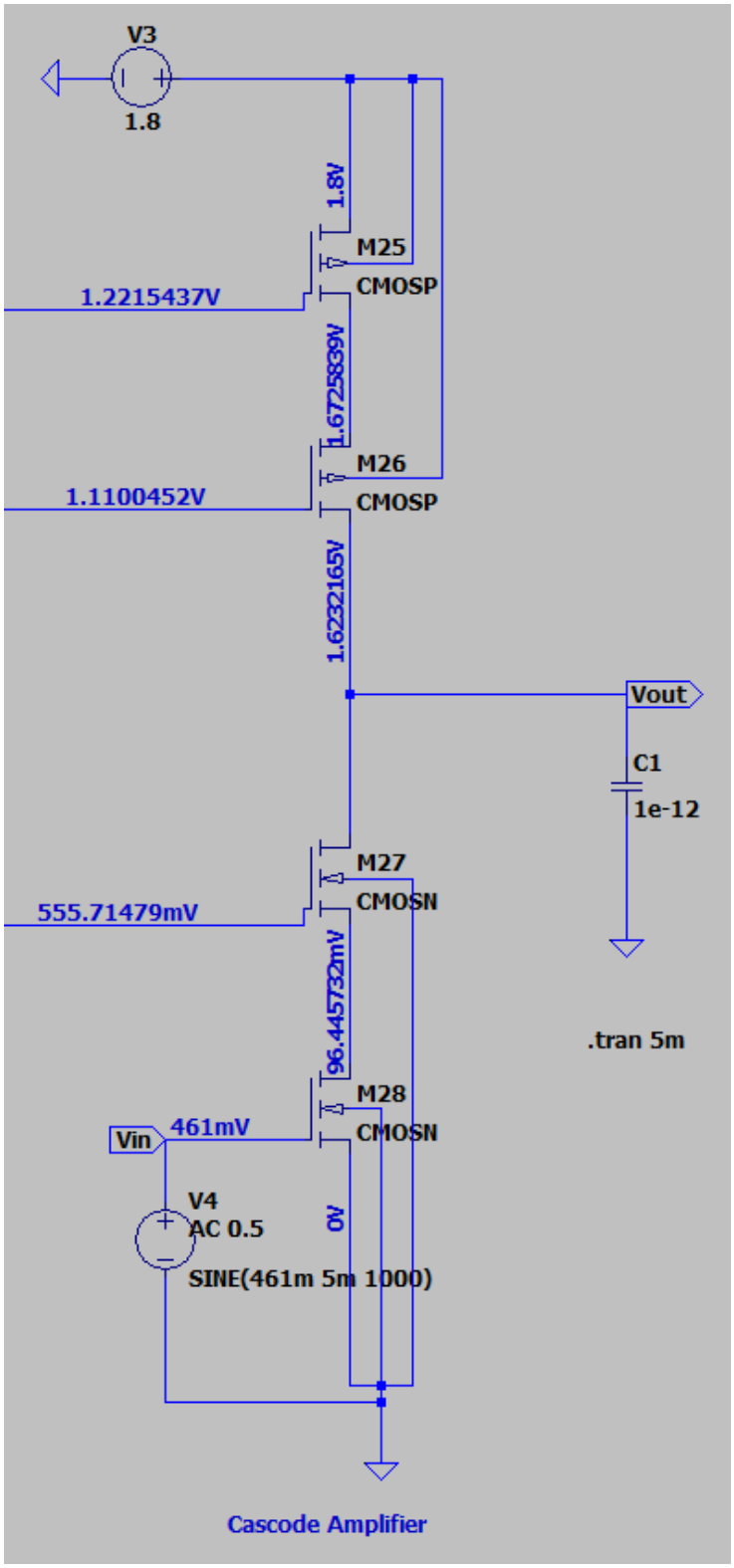
Submitted by : Ranjeet Singh - 2021EEB1203

180 nm Schematic :






V3
1.8
1.8V
M25
CMOSP
1.2215437V
1.6725839V
M26
1.1100452V
CMOSP
1.6232165V
Vout
C1
1e-12
M27
CMOSN
555.71479mV
96.445732mV
.tran 5m
M28
Vin
461mV
CMOSN
V4
AC 0.5
0V
SINE(461m 5m 1000)
Cascode Amplifier

Calculations :

We get the values of bias voltages as

Vbias1 = 1.221V , Vbias2 = 1.11 V ,Vbias 3 = 555.7mV

Assumed the input bias voltage as 462mV.

For a gain of 20V/V , we assume the cutoff frequency to be 500KHz. We use this to calculate output impedance of the circuit.

The process parameters are as follows ,

$$\mu_n C_{ox} = 350.8\mu V/A^2, V_{tn} = 366.2mV$$

$$\mu_p C_{ox} = 71.2\mu V/A^2, |V_{tp}| = 390.6mV$$

$$R_{out} = 1/2\pi f C_L \qquad A_v = G_m R_{out}$$

$$G_m = g_m = \mu_n C_{ox}(W/L)(V_{gs} - V_{tn})$$

$$\text{For M1 NMOS, we get } \frac{W}{L} \text{ as : } 1.87$$

We get the current as :

$$I_d = 3.010\mu A$$

$$\text{Saturation condition on M1 : } V_d \geq V_g - V_{tn}$$

$$V_d \geq 95.8mV$$

$$\text{For M4 ,equating the current , we get}$$

$$I_d = 3.010\mu A = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_{p1}(V_{sg} - V_{tp})^2$$

We get the W/L ratio as ,

$$(\frac{W}{L})_{M4} = 2.342$$

Saturation condition on M4 ,

$$(V_d)_{M4} \leq 1.61V$$

Now applying saturation conditions on M3 ,

Using the upper bound of current equation,

$$3.010\mu A \leq \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_{M3}(1.61 - 1.11 - 0.39)^2$$

$$\text{We get} : (\frac{W}{L})_{M3} \geq 6.98$$

$$\text{Saturation condition on M3} : (V_d)_{M3} \leq 1.5V$$

For M2,
The condition of saturation gives

$$(V_d)_{M2} \geq 189.5mV$$

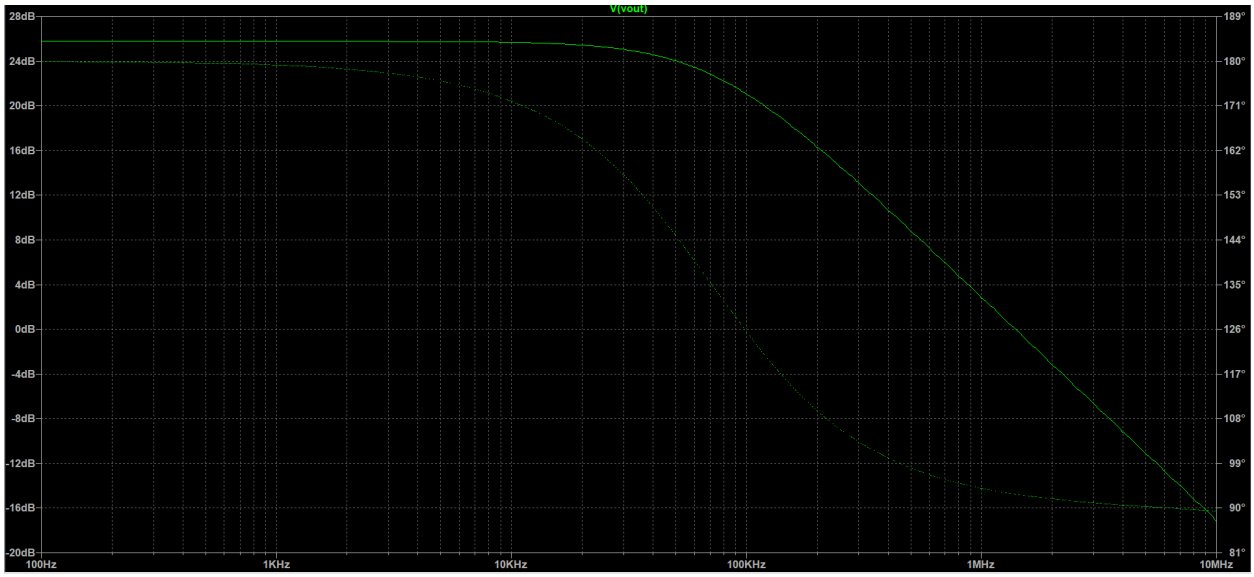
We use the upper bound condition on M2,and equate it with the current

$$(\frac{W}{L})_{M2} \geq 1.95$$

From the simulation values , shown in the following figure, we will obtain the value of the current and get the power consumed by the circuit.We observe that all the transistors are in saturation. We use the bounds calculated to get the desired values,

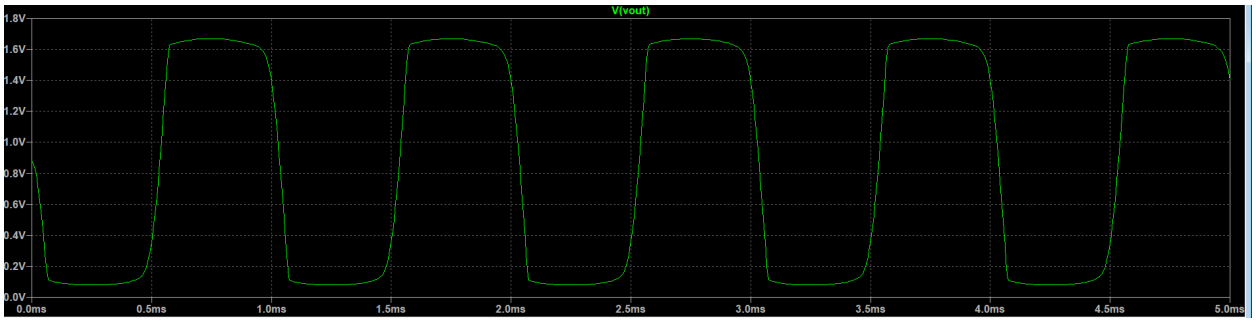
Doing the transient analysis, we get the following output :

Frequency Response



We observe the gain in 25.78 dB and the unity gain bandwidth is 1.37MHz.

2. Vout

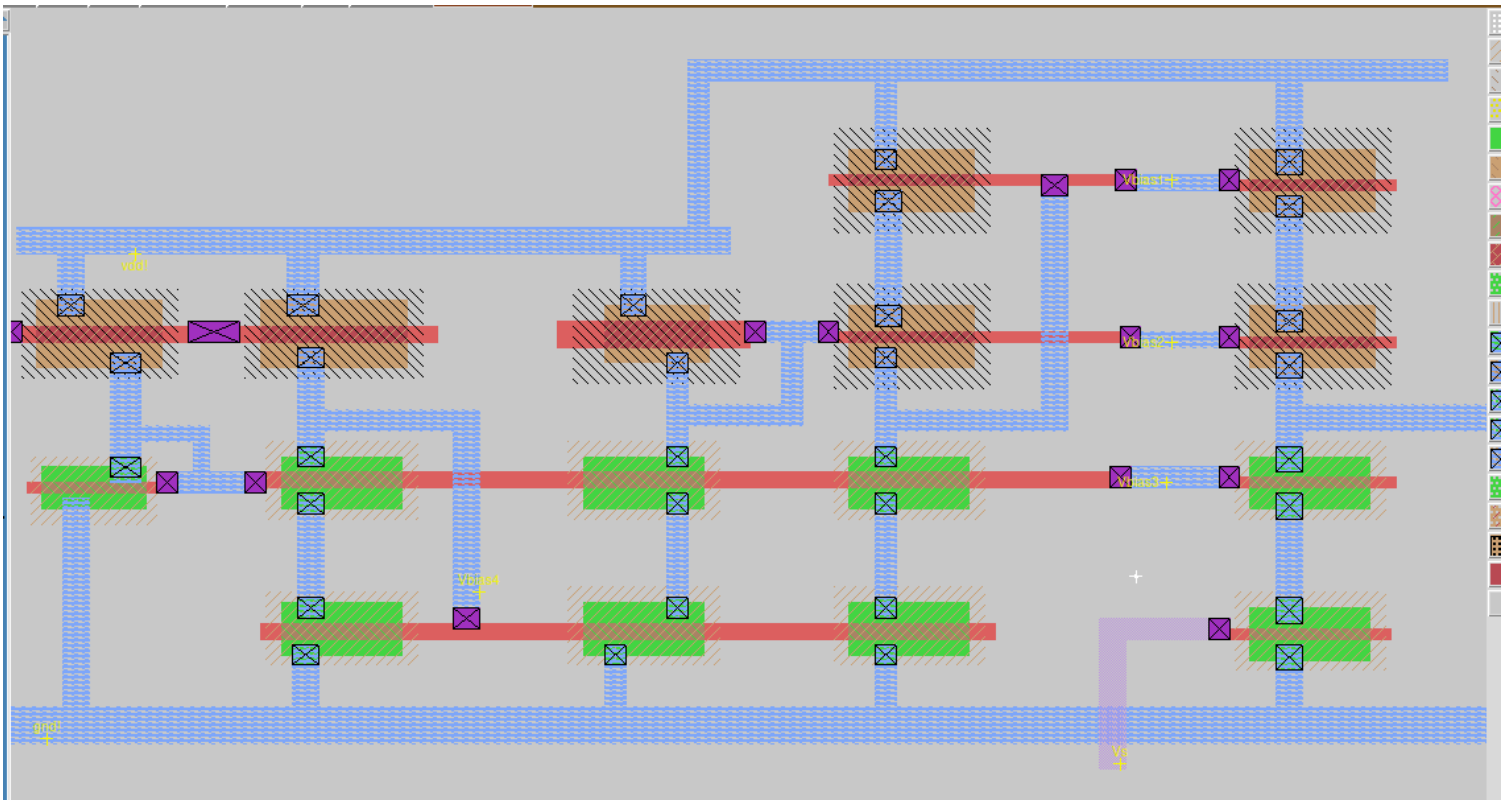


The following W/L values were used in the circuit above:

MOSFET	W/L
M1	1480n/360n
M2	1920n/360n
M3	1620n/360n
M4	460n/360n

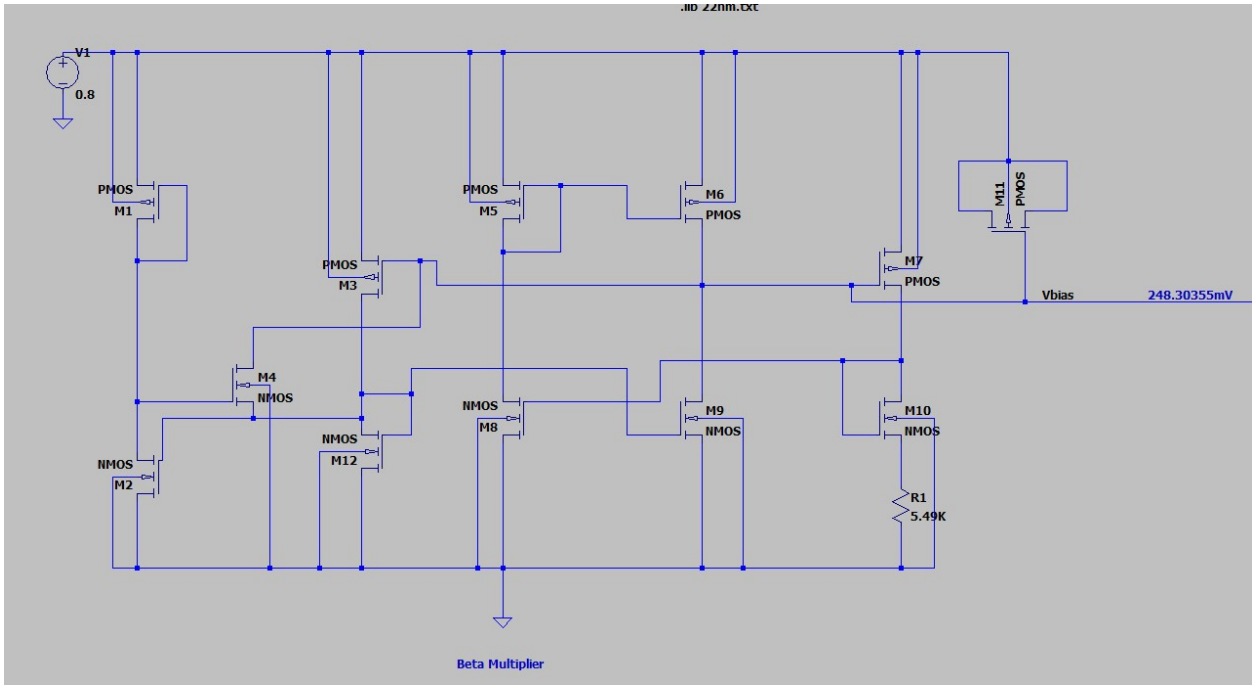
Power Dissipated = 5.418uW which is less than 5mW

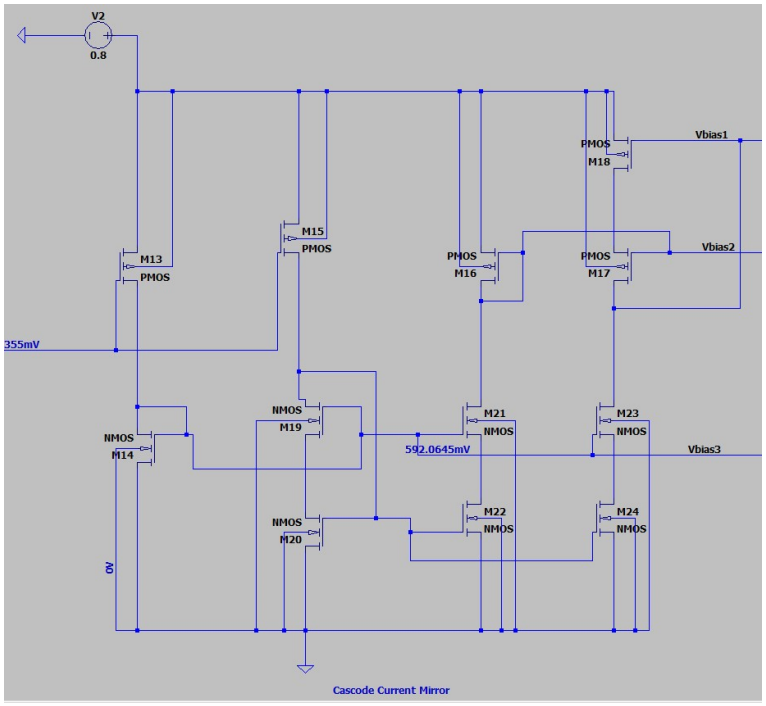
Magic Layout:

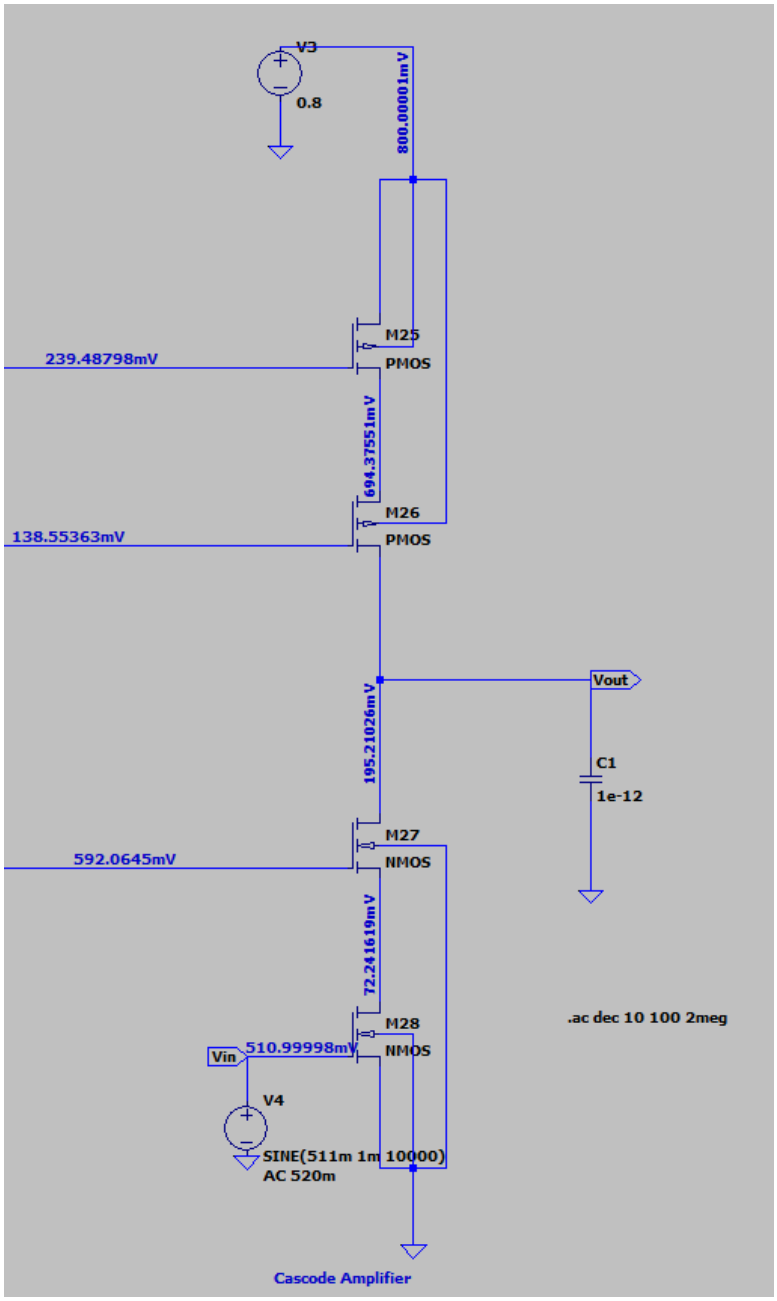


Layout of both the current mirror and cascode amplifiers with the labels.

22nm :


.lib 22nm.txt
V1
0.8
PMOS
M1
PMOS
M5
M6
PMOS
M11
PMOS
PMOS
M3
M7
PMOS
Vbias
248.30355mV
M4
NMOS
NMOS
M8
M9
NMOS
M10
NMOS
NMOS
M2
NMOS
M12
R1
5.49K
Beta Multiplier


V2
0.8
Vbias1
PMOS
M18
M15
PMOS
M13
PMOS
PMOS
M16
PMOS
M17
Vbias2
355mV
NMOS
M19
M21
NMOS
M23
NMOS
NMOS
M14
592.0645mV
Vbias3
M22
NMOS
M24
NMOS
NMOS
M20
0V
Cascode Current Mirror



Given specifications from the txt file of 22nm ,we get the following parameters :

$$V_{tn} = 503mV \qquad \mu_n C_{ox} = 120\mu V/A^2$$

$$V_{tp} = 460mV, \mu_p C_{ox} = 60\mu V/A^2$$

The bias voltages are :

Vbiasp = 248.3 mV , Vbias1 = 239.48mV , Vbias2 = 138.55mV , Vbias3 = 592.06mV
The bias voltage at the input is given to be 511mV

Assuming the cutoff frequency of 250 kHz, the output impedance of the circuit is

$$R_{out} = 1/2\pi f C_L$$

Considering the last NMOS as M1 and the MOSFETS above as M2,M3,M4 respectively,

The gain of the amplifier is given by :

$$A_v = G_m R_{out}$$

Here Gm is the transconductance of the M1 NMOS, we get the value of W/L ratio as :

$$G_m = g_m = \mu_n C_{ox}(W/L)(V_{gs} - V_{tn})$$

$$\text{We get } g_m \text{ as the following :} g_m = 0.0314mS$$

Applying condition of saturation on the M1 NMOS ,
From the Simulation , we have

$$V_{ds} = 72.24mV$$

$$V_{gs} - Vtn \leq V_{ds}$$

$$g_m/(\mu_n C_{ox} W/L) \leq V_{ds} \qquad 36.3 \leq W/L$$

Using W/L for M1 as 21/2, the value of current obtained is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{tn})^2$$

$$I_D = 5.27\mu A$$

Equating the current for M4 PMOS,

$$I_D = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L}_p)(V_{sg} - |V_{tp}|)^2$$

$$\text{We get } (\frac{W}{L})_p = 17.37$$

Now applying conditions of saturation on all the Transistors , we get

Condition of saturation on M4 :

$$V_{sg} - |V_{tp}| \leq V_{sd}$$

$$V_d \leq 699.48mV$$

Applying $(\frac{W}{L})_p$ as $26/2$, we get $(V_d)_{M4}$ as 694.3mV

Condition of saturation on M3 :

$$\text{Given : } (V_{sg})_{M3} = (V_d)_{M4} - V_{bias2}$$

$$(V_d)_{M3} \leq V_{tp} + V_{bias2}$$

$$(V_d)_{M3} \leq 598.55mV$$

Using the current equation on M3, we get the bound on the W/L ratio of this MOSFET,

$$5.27\mu A \leq \frac{1}{2}60\mu A/V^2(\frac{W}{L})_{M3}(699.48 - 138.55 - 460mV)^2$$

Hence for M3 , we have

$$\frac{W}{L} \geq 10.707$$

Using this value as 27/2 , we get a large voltage drop across M2 NMOS,
Using the current condition , we get the W/L raito by assuming the voltage at source as 72.24mV

Hence the W/L ratio for M2 is :

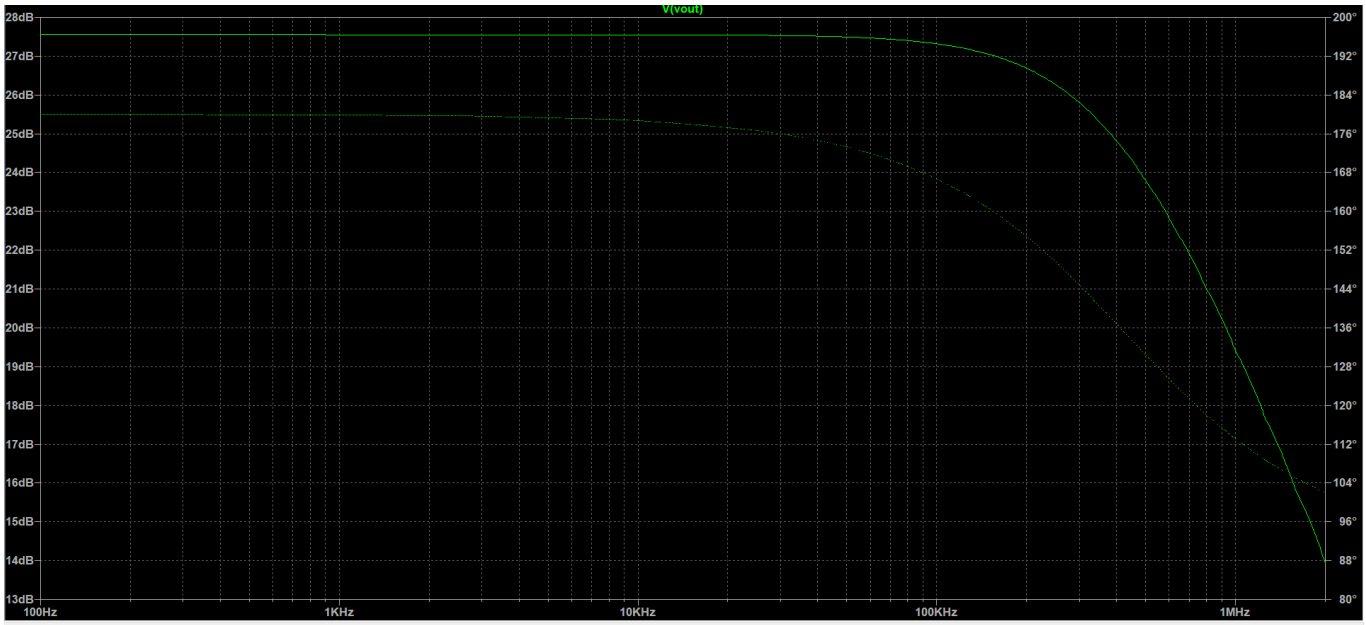
$$V_{bias3} = 592.06mV \qquad (V_s)_{M2} = 72.24mV$$

$$(\frac{W}{L})_{M2} \simeq 31$$

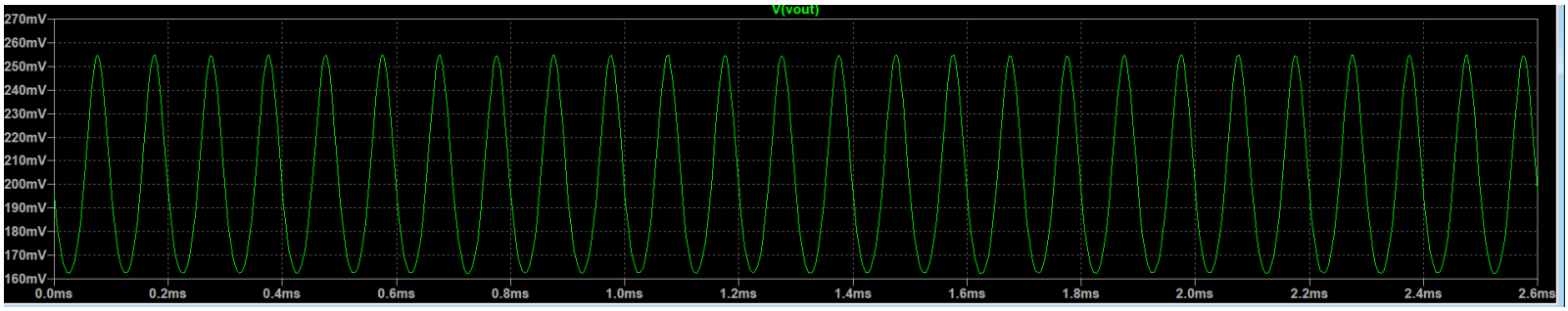
We get the following waveforms, using the obtained values of W/L and use hit and trial to reach the desired value of the gain.

MOSFET	W/L ratio
M1	21/2
M2	21/2
M3	27/2
M4	26/2

Frequency Response:



Vout :



We observe Av = 27.547dB , Unity Gain Bandwidth = 10 MHz

Power Dissipated = 4.216uW

Therefore, our 22nm circuit meets the circuit specifications requirements.

Conclusion :

1. The gain of the amplifier in the case of 180 nm is 25.78 dB and in case of 22nm is 27.547dB.
2. The unity gain bandwidth is 1.37MHz for 180nm and 10MHz for 22nm.
3. We observe that the power dissipation is also less than 5mW in both the cases.