

EECS 270A – Advanced Analog IC Design - 1

Fall 2021

Final Project

University of California, Irvine

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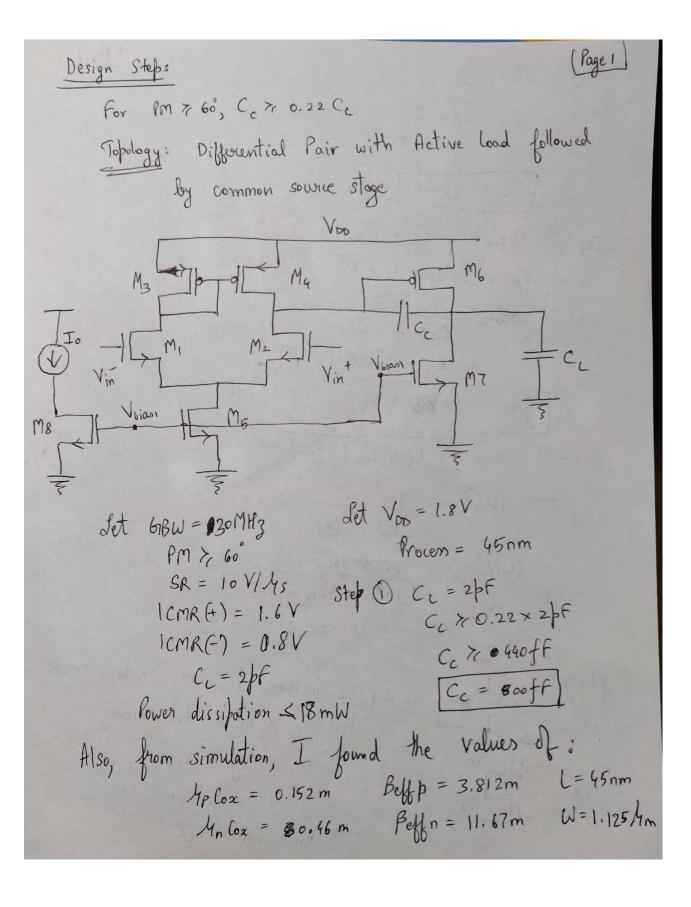
Design problem:

Design an amplifier (with more than one stage) that satisfies the listed requirements:

- (Gain-bandwidth product) GBW > 210e9
- $Rin > 500 k\Omega$
- Rout $< 150 \Omega$
- DC Power Consumption < 18 mW
- Output Voltage Swing > 2.4 Vpp
- Vdd < 3.6

Design approach:

The amplifier was designed on paper and then simulated on Cadence. The details of the design are as shown below:



Step (2)
$$SR = J_5$$
 C_c
 $I_5 = SR \times C_c$
 $I_5 = 20V \times 800 \text{ f}$
 $J_5 = 20VA$

Step (3) Design of M , $2M_2$
 $g_{mi} = G18W \times C_c \times 2\pi$
 $= 20 \times 10^6 \times 800 \text{ f} \times 2\pi$
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 $= 20 \times 10^6 \times 800 \text{ f} \times 2\pi$
 $= 20 \times 10^6 \times 10^6 \times 10^6 \times 2\pi$
 $= 20 \times 10^6 \times 10$

$$V_{in}(max) = V_{di} + V_{ti} - 0$$

$$V_{di} = V_{bo} - V_{sg3}$$

$$V_{di} = V_{bo} - \sqrt{\frac{2 T_{o}}{\beta_{P}}} + |V_{tx}|$$

$$= V_{gs} = \sqrt{\frac{2 T_{s}}{\beta_{P}}} + |V_{tx}|$$

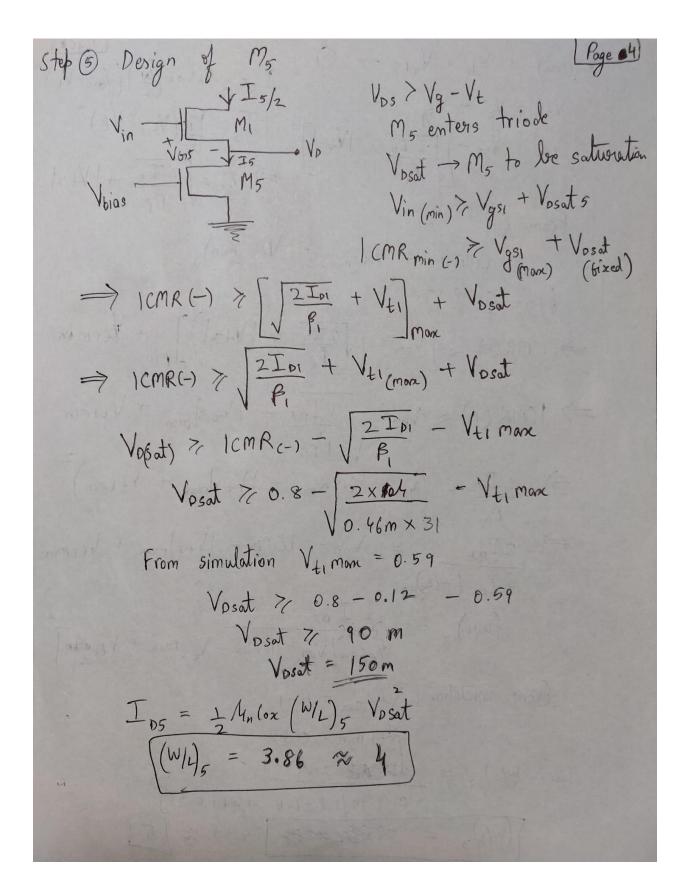
$$= V_{gs} = \sqrt{\frac{2 T_{s}}{\beta_{P}}} + |V_{tx}|$$
From 0,
$$|CMR(+)| \leq |V_{oi}(min)| + |V_{ti}(min)|$$
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$$|CMR(+)| \leq |V_{oi}(min)| + |V_{ti}(min)|$$

$$= V_{gs} = \sqrt{\frac{2 T_{s}}{\beta_{P}}} + |V_{tx}|$$

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$$= V_{ti}(min)$$



Step 6 Design of M6 For PM of 60°, gm6 > 10gm, gm6 7 10 × 160 4 9m6 ≥ 1600 le VD53 = VDS4 = VDS6 Dass = Vast = Vast $\frac{(W/L)_6}{(W/L)_4} = \frac{I_6}{I_4} \Rightarrow \frac{(W/L)_6}{(W/L)_4} = \frac{g_{m6}}{g_{m4}}$ gm4 = J2Ip. 4p Cox (W/L)4 gm4 = \ \ 2014 x 0.152 m x 4 gm4 = 110.27/4A/V (WL) 6 = gm6 (WL)4 $= \frac{1600 \times 5}{110.27}$ = 58.03 (w/L) 6 % 59

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Step (7) Design of
$$M_7$$

$$\overline{I}_6 = \frac{(\omega/L)_6}{(\omega/L)_4}$$

$$= \frac{(\omega/L)_6}{(\omega/L)_4} \times \overline{I}_4$$

$$= \frac{59}{4} \times 10 \text{ A}$$

$$= \frac{147.5 \text{ A}}{12.5 \text{ A}}$$

$$\overline{I}_7 = \frac{(\omega/L)_7}{(\omega/L)_5}$$

$$(\omega/L)_7 = \overline{I}_7 \cdot (\omega/L)_5$$

$$(\omega/L)_7 = \overline{I}_7 \cdot (\omega/L)_5$$

$$= \frac{150}{45} \times 4$$

$$(\omega/L)_{1,2} = 4 \rightarrow \frac{180}{45}$$

$$(\omega/L)_{2,3} = 4 \rightarrow \frac{180}{45}$$

$$(\omega/L)_{3,4} = 5 \rightarrow \frac{225}{45}$$

$$(\omega/L)_{1,2} = 30 \rightarrow \frac{1350}{45}$$

PC Power consumption:

PIV X I

= 1.8 × ((1504) + (204))

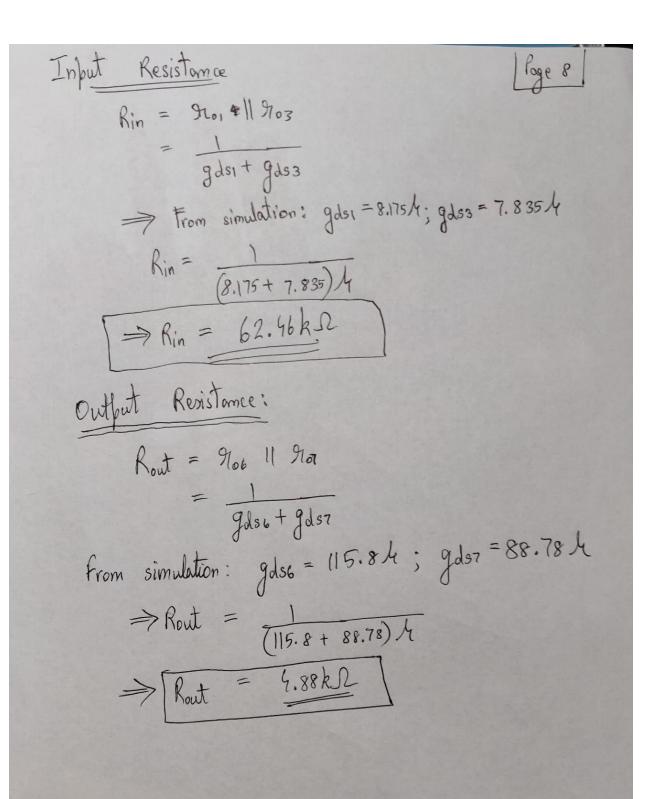
= 1.8 × (17047)

= 0.3 m W

Output voltage Swing:

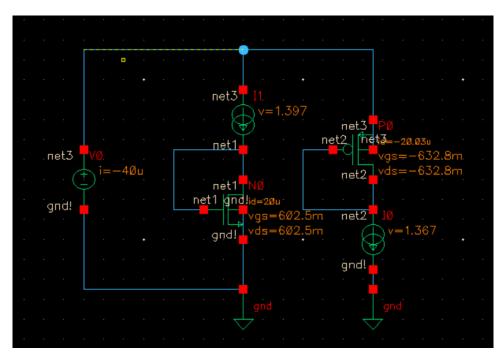
Vout(max) =
$$V_{DD}$$
 - $V_{DSOT}(6)$

= 1.8 - $V_$

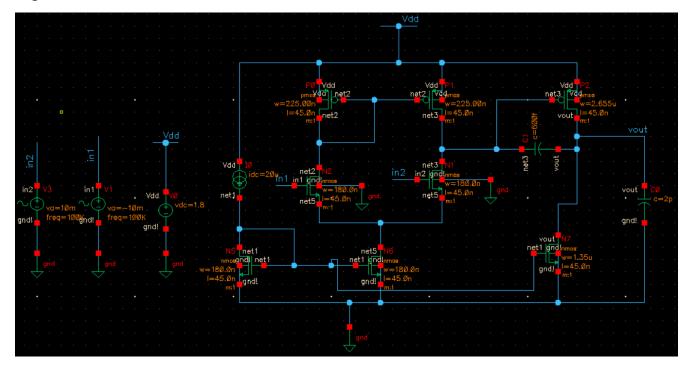


Simulation results:

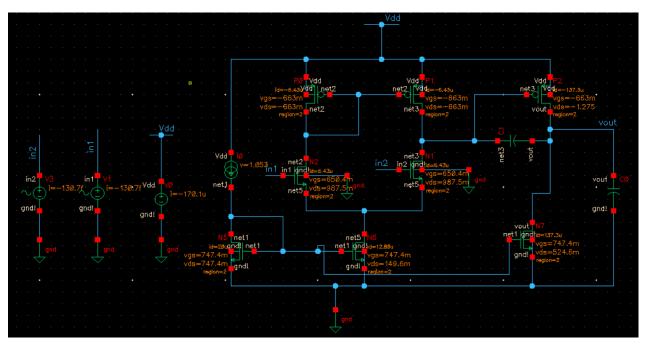
The circuit used to calculate the beta effective is as follows:



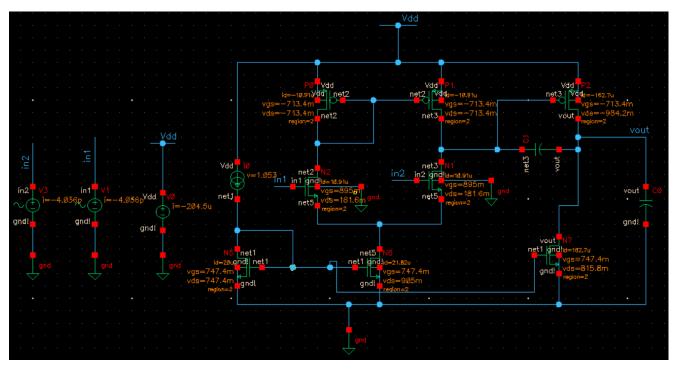
The amplifier circuit schematic is as shown: The dimensions of the transistors are depicted in the schematic.



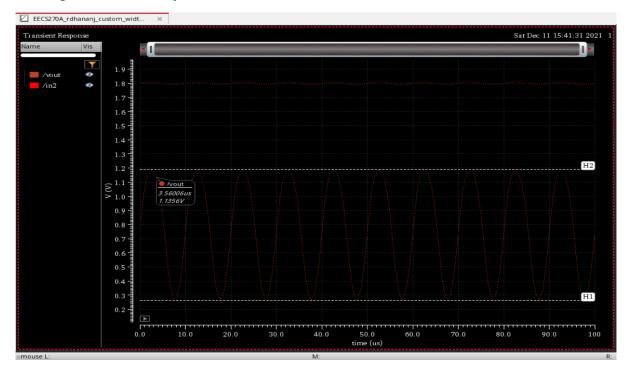
The DC analysis by setting ICMR = $\underline{\mathbf{0.8V}}$ is as follows: All transistors are in region 2(saturation)



The DC analysis by setting ICMR = $\underline{1.6V}$ is as follows: All transistors are in region 2(saturation)



Running transient analysis:



Input amplitude vin (p to p) - 10 mV

Input amplitude vip (p to p) - -10mV

Input frequency – 100kHz

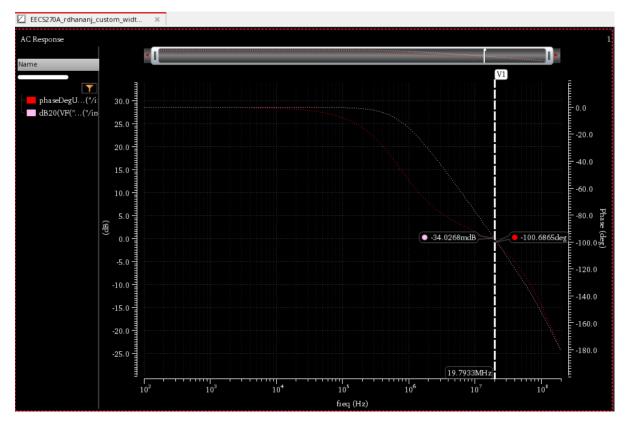
Start time -0

Stop time – 100us

 $Common\ mode\ voltage-1.6V$

Output amplitude (p to p) -0.92V

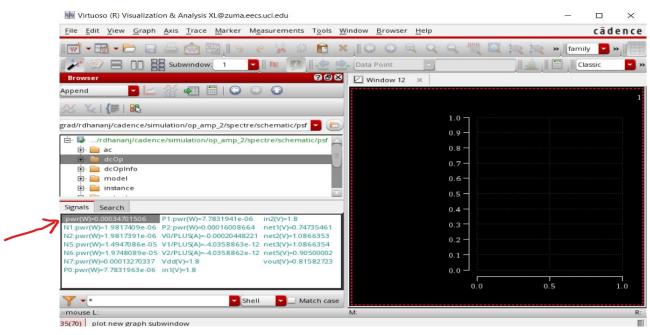
Running AC analysis and plotting the AC gain and phase:



It is observed that the GBW is 19.79MHz. Gain is about 27dB.

The phase margin is obtained as 180 - 100 = 80 degrees

Simulation to find the power dissipation:



From the simulation, we see that the power dissipation is 0.00034701506W which is approximately $\underline{0.35mW}$

Summary:

Simulation results observed:

- 1. Gain Bandwidth Product 19.79MHz
- 2. Phase Margin **80 degrees**
- 3. Gain **27dB**
- 4. Power dissipation $\underline{0.35mW}$
- 5. Vdd used **1.8V**
- 6. Rin **62.46k ohm**
- 7. Rout **4.88k ohm**