

Ranjith Tamil Selvan

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<https://www.linkedin.com/in/ranjith-tamil-selvan/>
<https://github.com/ranjithtamil/cplusplus>

EDUCATION

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- Texas A&M University**, College Station, TX May 2020
- Master of Science in Computer Engineering (CEEN) (GPA: 3.8 / 4.0)
(Courses – Algorithms, Operating Systems, Distributed Systems & Cloud Computing, Secure Computer Systems, Software Engineering)
- College of Engineering Guindy**, Chennai, India April 2015
- Bachelor of Engineering in Electronics and Communication (GPA: 3.5 / 4.0)
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- ## SKILLS

Programming Languages: C, C++, Python
Languages: English (Native), Tamil (Proficient), Hindi, Malayalam, Arabic (Limited)

EXPERIENCE

Fujitsu Network Communications

- Software Engineer III, Richardson, TX* September 2020- Present
- Develop software features for the Layer3 protocols team working on dhcp, ospf
 - Bring-up of switch-emulator for easier and faster prototyping

Arista Networks

- Software Development Intern, Austin, TX* May 2019- August 2019
- Implemented a leader-election algorithm for high availability of Arista's extensible operating system (EOS) switches in C++/Python
 - Fixed software bugs in hardware abstraction modules and infrastructure modules

Nokia

- Technical Lead, Platform Team Core-1 Protocols, Chennai, India* May 2018- August 2018
- Developed software for platform and infrastructure teams for Nokia's network switch (7302/7330 products)
 - Customized HAL source code between network OS and network processor sdk (Broadcom sdk)
 - Implemented feature requirements for infrastructure modules such as card management & redundancy

Senior Software Engineer

May 2016- April 2018

- Spearheaded code-porting of edge router network stack running on different platforms onto Nokia's platform – involved customizing hardware dependent platform source-code on different architecture, CPU and network processor
- Performed initial source layout analysis, creating development environments for the team – cross-compiling for target, building common system libraries and OS libraries
- Migrated existing third-party toolchain (Greenhill's) to open-source GCC, resulting in enhanced compile time (by 70%), reduced image size (reduced by 50%)
- Developed, improved and integrated a new systemwide tracing instrumentation framework process for timestamping, stack-tracing, dumping useful platform details and packet tracing to improve developer live debugging and prototyping

Graduate Engineering Trainee

June 2015- April 2016

- Customized board support package (BSP) for a new quad core PPC based Freescale SoC (T2080) hardware
- Specialized in use of on-chip JTAG debuggers (GHS Multi, CodeWarrior, Lauterbach trace) for board-bring up, customized VxWorks source in areas of initialization, memory management, interrupt controller, process scheduler and bringing up kernel shell
- Collaborated with managers, technical architects and software testers to fix bugs and provide solutions by analysis of post-mortem logs obtained from system-crash scenarios from field (and) scaling tests