

Electric and Electronic Components in Motor Vehicles
48 V On-Board Power Supply
Requirements and Tests

VDA 320

This VDA Recommendation covers electric and electronic components in motor vehicles for the development of a 48 volt power supply.

This Recommendation was elaborated in the VDA's Working Group electronics, project group "48 Volt Power Supply".

If modifications are required to individual sections of the test in an individual case, they should be agreed separately between the vehicle manufacturer and the supplier.

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Continued on pages 2 to 54

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Contents

	Page
1 References	8
Non-destructive testing - Visual testing - General principles	8
2 Terms and definitions	9
2.1 Terms and abbreviations	9
2.2 Terminal markings	9
2.3 Temperatures	9
2.4 Times	9
2.5 Voltages and currents.....	10
2.6 Modes of operation	12
2.7 Functional statuses.....	13
3 General requirements	14
3.1 Assumptions regarding components with 48 V connection	14
3.2 Requirements for components with 48 V connection.....	14
3.3 Standard tolerances	15
3.4 Standard values.....	15
3.5 Sampling rate and measured value resolution.....	15
3.6 Description of interfaces	15
3.7 Restrictions on performing the tests	15
3.8 Test voltages	16
3.9 Test procedure	16
3.10 Parameter check	17
3.11 Continuous parameter monitoring with drift analysis	18
3.12 Physical analysis	18
4 Electrical requirements and tests.....	19
4.1 E48-01a Long-term Overvoltage	19
4.2 E48-01b Overvoltage with Components that Return Electrical Energy.....	20
4.3 E48-02 Transient Overvoltage.....	22
4.4 E48-03 Transient Event in Lower Limited Operation Range.....	23
4.5 E48-04 Recuperation.....	24
4.6 E48-05 Superimposed Alternating Voltage.....	25
4.7 E48-06 Slow Decrease and Increase of the Supply Voltage	27
4.8 E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage	30
4.9 E48-08 Reset Behaviour.....	32
4.10 E48-09 Brief Interruptions.....	34
4.11 E48-10 Starting Pulses.....	36
4.12 E48-11 Ground Loss in 48 V Power Supply	38
4.13 E48-12 Ground Offset	41
4.14 E48-13 Internal Dielectric Strength.....	42

4.15 E48-14 Standby Current.....	43
4.16 E48-15 Operation in Unlimited Operation Range	44
4.17 E48-16 Operation in Upper Limited Operation Range	45
4.18 E48-17 Operation in Lower Limited Operation Range	46
4.19 E48-18 Overvoltage Range	48
4.20 E48-19 Undervoltage Range	49
4.21 E48-20a Fault Current, Part 1.....	51
4.22 E48-20b Fault Current, Part 2.....	52
4.23 E48-21 Short Circuit in Signal Line and Load Circuit.....	53

List of figures

	Page
Figure 1: Definitions of the voltage ranges.....	10
Figure 2: Component with two voltage supplies.....	16
Figure 3: Test pulse for E48-01a Long-term Overvoltage.....	19
Figure 4: Test pulse for E48-01b Overvoltage with Components that Return Electrical Energy	21
Figure 5: Test pulse for E48-02 Transient Overvoltage	22
Figure 6: Test pulse for E48-03 Transient Event in Lower Limited Operation Range	23
Figure 7: Test pulse for E48-04 Recuperation	24
Figure 8: Test pulse for E48-05 Superimposed Alternating Voltage	26
Figure 9: Test pulse for E48-06a Slow Decrease and Increase of the Supply Voltage	27
Figure 10: Test pulse for E48-06b for Operation with Storage, Part 1	28
Figure 11: Test pulse E48-06c for Operation with Storage, Part 2	29
Figure 12: Test pulse for E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage	31
Figure 13: Test pulse for E48-08 Reset Behaviour	33
Figure 14: Test pulses for E48-09 Brief Interruptions	35
Figure 15: Basic circuit for E48-09 Brief Interruptions.....	35
Figure 16: Test pulse: E48-10 Starting Pulses.....	36
Figure 17: Basic circuit diagram for E48-11 Ground Loss in 48 V Power Supply	39
Figure 18: Basic circuit diagram for E48-12 Ground Offset (U_{B48})	41
Figure 19: Basic circuit diagram for E48-13 Internal Dielectric Strength.....	42
Figure 20: Test pulse for E48-15 Operation in Unlimited Operation Range.....	44
Figure 21: Test pulse for E48-16 Operation in Upper Limited Operation Range	45
Figure 22: Test pulse for E48-17 Operation in Lower Limited Operation Range	47
Figure 23: Test pulse for E48-18 Overvoltage Range.....	48
Figure 24: Test pulse for E48-19 Undervoltage Range.....	50

Figure 25: Basic circuit diagram for E48-20a Fault Current, Part 1	51
Figure 26: Basic circuit diagram for E48-20b Fault Current, Part 2	52
Figure 27: Basic circuit diagram for E48-21 Short Circuit in Signal Line and Load Circuit	54

List of tables

	Page
Table 1: References.....	8
Table 2: Abbreviations	9
Table 3: Abbreviations for temperatures	9
Table 4: Abbreviations for times.....	9
Table 5: Abbreviations for voltages and currents.....	11
Table 6: Definitions of standard tolerances	15
Table 7: Definitions of standard values	15
Table 8: Testing parameters for E48-01a Long-term Overvoltage.....	19
Table 9: Test parameters for E48-01b with Components that Return Electrical Energy, Part 1	20
Table 10: Test parameters for E48-01b Overvoltage with Components that Return Electrical Energy, Part 2.....	21
Table 11: Test parameters for E48-02 Transient Overvoltage	22
Table 12: Test parameters for E48-03 Transient Event in Lower Limited Operation Range.....	23
Table 13: Test parameters for E48-04 Recuperation.....	24
Table 14: Test parameters for E48-05 Superimposed Alternating Voltage, Part 1 ...	25
Table 15: Test parameters for E48-05 Superimposed Alternating Voltage, Part 2 ...	26
Table 16: Test parameters for E48-06a Slow Decrease and Increase of the Supply Voltage	27
Table 17: Test parameters for E48-06b for Operation with Storage, Part 1.....	28
Table 18: Test parameters for E48-06c for Operation with Storage, Part 2.....	29
Table 19: Test parameters for E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage	30
Table 20: Test parameters for E48-08 Reset Behaviour.....	32
Table 21: Test parameters for E48-09 Brief Interruptions.....	34
Table 22: Test parameters for E48-10 Starting Pulses	36
Table 23: Test parameters for E48-11 Ground Loss in 48 V Power Supply	39
Table 24: Test parameters for E48-12 Ground Offset.....	41
Table 25: Test parameters for E48-13 Internal Dielectric Strength.....	42
Table 26: Test parameters for E48-14 Standby Current.....	43
Table 27: Test parameters for E48-15 Operation in Unlimited Operation Range	44

Table 28: Test parameters for E48-16 Operation in Upper Limited Operation Range	45
Table 29: Test parameters for E48-17 Operation in Lower Limited Operation Range	46
Table 30: Test parameters for E48-18 Overvoltage Range	48
Table 31: Test parameters for E48-19 Undervoltage Range	49
Table 32: Test parameters for E48-20a Fault Current, Part 1.....	51
Table 33: Test parameters for E48-20b Fault Current, Part 2.....	52
Table 34: Test parameters for E48-21 Short Circuit in Signal Line and Load Circuit	53

Area of application

This document defines requirements, test conditions and tests performed on electric, electronic and mechatronic components and systems for use in motor vehicles with a 48 V on-board power supply. Unless otherwise indicated, the tests described here are not electric service life tests.

Any additional or differing requirements, test conditions and tests are defined in the relevant component specifications.

The tests described here do not serve to qualify either components or the production process.

1 References

The documents cited below (Table 1) are required for application of this document. Whenever the publications are cited with dates, only the version referred to applies. When the publications are cited without dates, the last version of the document applies (including all amendments).

Table 1: References

ANSI/UL94	Standard for Safety Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
DIN 72552-2	Terminal markings for vehicles - Part 2: Codes
DIN 72552-4	Terminal markings for vehicles - Part 4: Summary
DIN EN 13018	Non-destructive testing - Visual testing - General principles
DIN EN ISO/IEC 17025	General requirements for the competence of testing and calibration laboratories

2 Terms and definitions

The following terms and definitions apply for application of this document.

2.1 Terms and abbreviations

Table 2: Abbreviations

Abbreviation	Meaning
A, B, C, D in diagrams	Functional status A, B, C, D
DUT	Device Under Test (specimen)
GND	Ground for 12/24 V electrical system (terminal 31)
GND48	Ground for 48 V electrical system (terminal 41)
n.c.	Not connected
PTB	The Physikalisch-Technische Bundesanstalt, Germany's national metrology institute
RMS	Root mean square
Store	Energy store (e.g. battery)
TB	Subsystem (part of vehicle power supply system)

2.2 Terminal markings

Terminal 40 is the positive lead for the 48 V supply.

Terminal 41 is the ground connection for the 48 V supply.

The terminal markings are defined in the German standards DIN 72552-2 and DIN 72552-4.

2.3 Temperatures

Table 3: Abbreviations for temperatures

Abbreviation	Meaning
T_{\min}	Minimum operating temperature
T_{RT}	Room temperature
T_{\max}	Maximum operating temperature
T_{test}	Test temperature

2.4 Times

Table 4: Abbreviations for times

Abbreviation	Meaning
t_r	Rise time, e.g. that of a voltage
t_f	Fall time e.g. that of a voltage
t_{test}	Test duration

All slope characteristics refer to 10% or 90% values of the voltage.

2.5 Voltages and currents

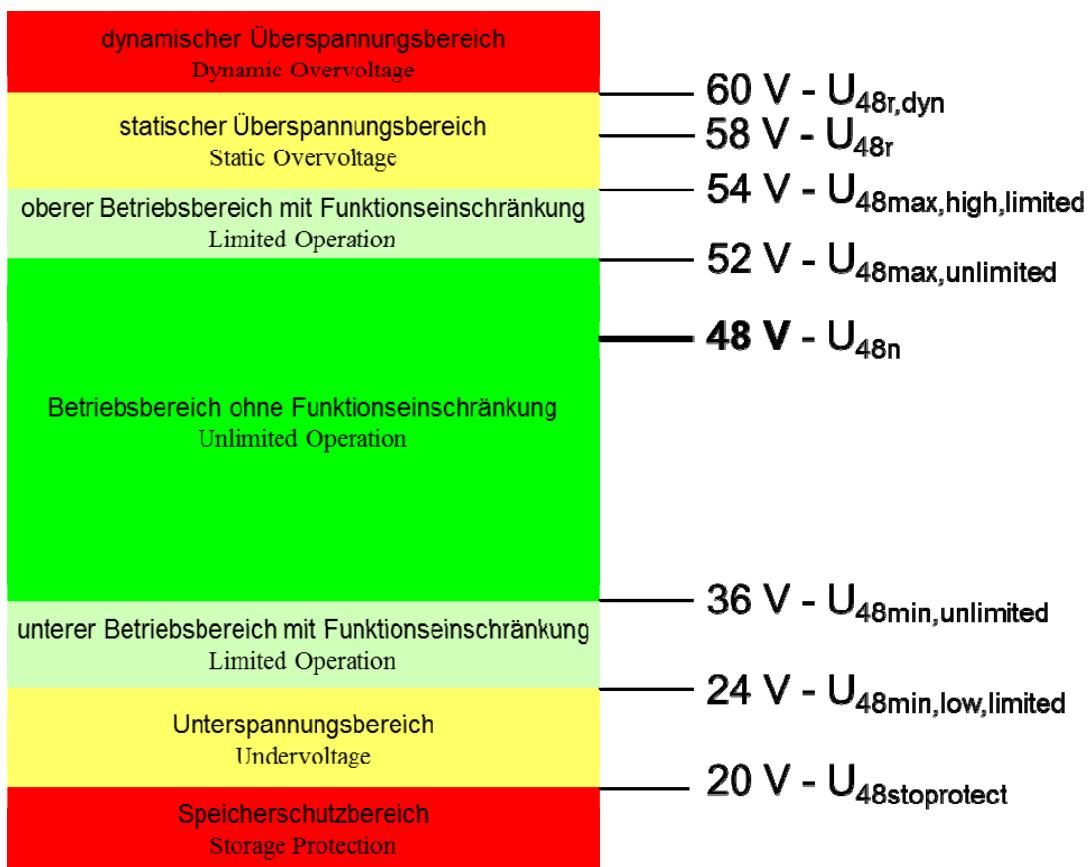


Figure 1: Definitions of the voltage ranges

Dynamic overvoltage

Voltages over $U_{48r,dyn}$.

Static overvoltage

The overvoltage range including all tolerances between $U_{48max,high,limited}$ and U_{48r} .
The range between U_{48r} and $U_{48r,dyn}$ represents the tolerance.

Upper limited operation range

The range between $U_{48max,unlimited}$ and $U_{48max,high,limited}$ is intended for calibrating the storage medium and for the uptake of recovered energy.

Unlimited operation range

The range between $U_{48min,unlimited}$ and $U_{48max,unlimited}$ allows the components to operate without restriction.

Lower limited operation range

The system may operate only temporarily in the range from $U_{48min,low,limited}$ to $U_{48min,unlimited}$. Countermeasures should be taken to bring about a return to the unlimited operation voltage range.

Undervoltage

All voltages below $U_{48\text{min,low,limited}}$ are defined as undervoltages. The storage protection voltage is $U_{48\text{stopprotect}}$.

Storage protection voltage

All voltages below $U_{48\text{stopprotect}}$.

Table 5: Abbreviations for voltages and currents

Abbreviation	Meaning	Value
$U_{48\text{r,dyn}}$	Lower limit of the dynamic overvoltage range	60 V
$U_{48\text{r}}$	Lower limit of the 2 V tolerance for the dynamic overvoltage range	58 V
$U_{48\text{max,high,limited}}$	Maximum voltage of the upper limited operation range	54 V
$U_{48\text{max,unlimited}}$	Maximum voltage of the unlimited operation range	52 V
$U_{48\text{n}}$	Rated voltage for 48 V power supply	48 V
$U_{48\text{min,unlimited}}$	Minimum voltage of the unlimited operation range	36 V
$U_{48\text{min,low,limited}}$	Minimum voltage of the lower limited operation range	24 V
$U_{48\text{stopprotect}}$	Storage protection voltage	20 V
$U_{48\text{pp}}$	Peak-to-peak voltage	
$U_{48\text{rms}}$	RMS value of a voltage	
$U_{48\text{max}}$	Maximum voltage that can occur during a test	
$U_{48\text{min}}$	Minimum voltage that can occur during a test	
$U_{48\text{test}}$	Test voltage for 48 V power supply	
$U_{12\text{test}}$	Test voltage for 12 V power supply	14 V
$U_{24\text{test}}$	Test voltage for 24 V power supply	28 V

2.6 Modes of operation

Throughout their service life the electrical, electronic and mechatronic components and systems work in various modes of operation, which are reproduced in the tests.

2.6.1 Mode of operation I – DUT is not electrically connected

2.6.1.1 Mode of operation I.a

The DUT is not energised; the connecting pins and wiring harness are not connected.

If a coolant circuit is present, it is not filled and the connections are sealed.

2.6.1.2 Mode of operation I.b

The DUT is not energised, but the connecting pins and wiring harness are connected.

If a coolant circuit is present, it is filled and the coolant lines are connected.

2.6.2 Mode of operation II – DUT is electrically connected

2.6.2.1 Mode of operation II.a

The DUT is operated without an operating load.

If a coolant circuit is present it should be filled, and the coolant lines should be connected. The throughput and temperature of the coolant should be adjusted if necessary – as set forth in the component specifications.

2.6.2.2 Mode of operation II.b

The DUT should be operated with the minimum operating load. It must be operated in such a manner that it generates the minimum intrinsic heating (e.g. by reducing a continuous power output or rarely triggering external loads).

If a coolant circuit is present, it should be filled and the coolant lines should be connected. The throughput and temperature of the coolant should be adjusted if necessary – as set forth in the component specifications.

2.6.2.3 Mode of operation II.c

The DUT is operated with the maximum operating load. It must be operated in such a manner that it generates the maximum intrinsic heating (e.g. through realistic maximisation of a continuous power output or by frequently triggering external loads).

If a coolant circuit is present, it should be filled and the coolant lines should be connected. The throughput and temperature of the coolant should be adjusted if necessary – as set forth in the component specifications.

2.7 *Functional statuses*

The functional statuses are indicated in the test descriptions and the relevant figures using the letters A to E.

2.7.1 *Functional status A*

The DUT must perform all the functions.

2.7.2 *Functional status B*

The DUT must perform all the functions while the test parameters are applied; however, one or more functions may lie outside the tolerance indicated for functional status A. The permissible deviations are defined either in the drawing or in the component specifications. After application is terminated, the DUT must return to functional status A automatically.

2.7.3 *Functional status C*

The DUT fails to perform one or more functions while the test parameters are applied. After application is terminated, the DUT returns automatically to functional status A or B (depending on the test). A DUT that acquires undefined functions at any time does not correspond to functional status C.

2.7.4 *Functional status D*

The DUT fails to perform one or more functions while the test parameters are applied. After application is terminated, the DUT returns to functional status A when the terminal is switched off and then on or when the vehicle is restarted. A DUT that acquires undefined functions at any time does not correspond to functional status D.

2.7.5 *Functional status E*

The DUT fails to perform one or more functions while the test parameters are applied; the DUT does not ignite (pursuant to UL 94 v0) and no short circuit occurs between the 48 V system and the 12/24 V system. After application is terminated, the DUT can no longer be used unless it is repaired or replaced.

3 General requirements

3.1 Assumptions regarding components with 48 V connection

- Static direct voltages ≤ 60 V occur with a maximum ripple of 10 % RMS in the on-board supply voltage.
- A single error in the wiring harness must not cause the 48 V supply to short circuit to the 12/24 V system.
- There is a common ground for the 12/24 V system and the 48 V system, which are connected via physically separate grounding bolts/connections.
- All the voltage and current information refers to the component (terminal voltage).
- The polarity of the 48 V supply is prevented from reversing by appropriate measures in the vehicle.
- Jump starting with the 48 V power supply is prevented by appropriate measures applied in the vehicle.

3.2 Requirements for components with 48 V connection

- A single error must not cause a short circuit between the 48 V supply and the 12/24 V supply.
- Components simultaneously supplied at 48 V and 12/24 V, and interfaces based on 12/24 V, need their own ground connections for both supply voltages. These ground connections must be physically separated from one another.
- If a 48 V component loses its ground (terminal 31 and/or terminal 41), this must not disrupt or destroy communication networks or the electrical networks.
- Overcurrent tests should be detailed in the component specifications.
- No component may cause the voltage to enter the dynamic overvoltage range (e.g. through a load dump or resonance peaks).
- If the voltage enters the overvoltage range up to U_{48r} , countermeasures should be taken via the component that is feeding energy back in/causing entry into the overvoltage range, so that the voltage exits the overvoltage range at the lower boundary.
- If the voltage enters the lower limited function range, countermeasures should be taken so that the voltage returns to the unlimited operation range.

3.3 Standard tolerances

Unless otherwise indicated, the tolerances specified in “Table 6: Definitions of standard tolerances” apply.

Envelope tolerances should always be viewed as one-sided only, so the requirement is not relaxed.

Tolerances refer to the required set-point.

Table 6: Definitions of standard tolerances

Abbreviation	Meaning	Tolerance limits
f	Frequency	$\pm 1 \%$
T	Temperature	$\pm 2 \text{ }^\circ\text{C}$
F _{rel}	Relative humidity	$\pm 5 \%$
t	Time	+ 5 % to 0 %
U	Voltage	$\pm 0.5 \%$
I	Current	$\pm 2 \%$

3.4 Standard values

Unless otherwise indicated, the standard values in “Table 7: Definitions of standard values” apply.

Table 7: Definitions of standard values

Abbreviation	Meaning	Value
T _{RT}	Room temperature	$23 \text{ }^\circ\text{C} \pm 5 \text{ }^\circ\text{C}$
F _{rel}	Relative humidity	25 % (+ 5 % to 0 %) to 75 % (- 5 % to 0 %)
T _{test}	Test temperature	T _{RT}
R _i	Internal resistance of the source	$10 \text{ m}\Omega \leq R_i \leq 100 \text{ m}\Omega$

3.5 Sampling rate and measured value resolution

The sampling rate/bandwidth of the measuring system should be adjusted for each test. All measured values must be recorded with all peaks.

The resolution of the measured values should be adjusted for each test. Care should be taken to ensure that any voltage peaks occurring do not cause voltage overflow, and that they do not fail to be measured because the resolution is too low.

3.6 Description of interfaces

Complete descriptions of statuses and electrical properties of all the interfaces must be provided. These descriptions form the basis of the evaluation of the test results and must have the appropriate amount of detail.

3.7 Restrictions on performing the tests

The testing laboratory must be organised and operated in accordance with DIN EN ISO/IEC 17025. All the testing equipment used for making measurements must be calibrated in accordance with DIN EN ISO/IEC 17025 (or as

determined or recommended by the manufacturer), and must be traceable to the PTB or another equivalent national metrology laboratory. The test devices, workshop equipment, set-ups and test procedures used must not influence the behaviour of the DUT (for example the current it draws). They should be documented in the test report together with the accuracies and the calibration expiry date.

3.8 Test voltages

Unless explicitly specified otherwise, the voltage curves indicated refer to the terminal voltages of the DUT and must be measured and documented in the test set-up.

The specified voltages under $U_{48r,dyn}$ should be maintained at the component with an accuracy given in "Table 6: Definitions of standard tolerances" (measured at the connector or terminal of the control unit).

A tolerance range of 0 % to -1 % applies to the $U_{48shprotect}$ threshold.

All 48 V components that are equipped with an interface for 12/24 V supply (see Figure 2), or communication interfaces, must also satisfy the corresponding requirements for the 12 V/24 V supply:

- during the 12/24 V supply system tests, the voltage in the 48 V supply system is U_{48n} , unless required otherwise in the individual tests;
- during the 48 V supply system tests, the voltage in the 12 V supply system is U_{12test} , unless indicated otherwise in the individual tests;
- during the 48 V supply system tests, the voltage in the 24 V supply system is U_{24test} , unless indicated otherwise in the individual tests.

In addition, it must be guaranteed and evidenced as appropriate that no voltage or voltage curve within the limits defined for the 48 V supply causes the destruction or loss of function of the component on the 12/24 V side. This also applies if the test pulse destroys the component to be tested on the 48 V side.

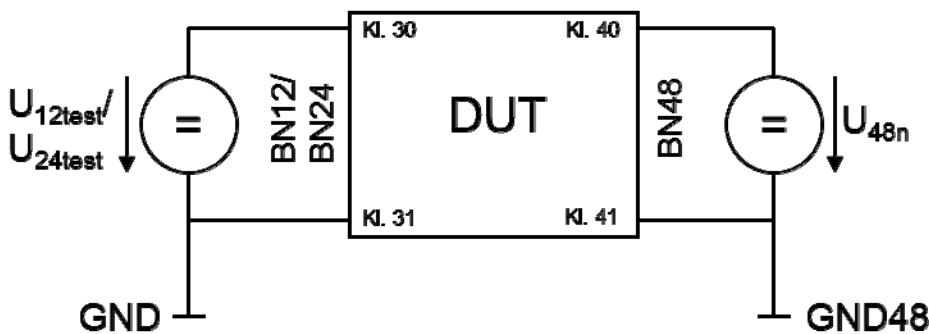


Figure 2: Component with two voltage supplies

3.9 Test procedure

The test procedure should be defined with the client in a testing plan. Each DUT undergoes all the agreed tests systematically. The electrical tests may be carried out in any order. For each test, the permitted error memory entries, functional statuses and severity levels for the component should be agreed with the client and recorded.

Details of the modes of operation, operating loads (e.g. triggering, original sensors, original actuators and replacement circuitry) and the required boundary conditions should be agreed between the client and the contractor and documented. Components that are electrically both a source and a sink must be tested in both modes of operation.

The mode of operation stipulated during the tests should represent the most demanding requirement for the component. Any deviations should be defined in the component specifications.

The functional status stipulated in the tests/parts of tests should be maintained as a minimum. Higher functional statuses (towards A) are permissible. The functional behaviour (including derating, e.g. in relation to temperature and voltage) of the component in the functional statuses, and the customer perception (e.g. visual, acoustic, tactile and thermal), should be defined by the client in the drawing or in the component specifications.

In all functional statuses, program and data storage devices must remain in functional status A until the component is deactivated. The integrity (not the current status) of the non-volatile memory must be ensured at all times.

Damage to the DUT is not permitted in functional statuses A to D. The permissible limit values specified in the data sheets (e.g. electrical, thermal or mechanical) of the electric/electronic components in the DUT must not be exceeded. Evidence of this is provided at least by the parameter check pursuant to section 3.10.

An electrical test begins when the DUT has started up completely and is in functional status A.

Before and after every test, the DUTs should be subjected to a parameter check pursuant to section 3.10 in accordance with specifications.

During each test, the key parameters to be monitored must be recorded as set forth in section 3.11. Component resets should be monitored and documented in an appropriate form.

The measuring results and data from the before/after tests may differ only within the specified permissible tolerances. Any changes in the measured values exceeding the measurement accuracies should be indicated as such. The measuring results must be examined for trends and drifts so that any abnormalities, ageing or malfunctions of the component can be identified.

Damaged DUTs should be removed from the test cycle and documented. In such cases, the test should be repeated with a new DUT, or the following test should be performed with a new DUT. The procedure should be agreed with the client.

The physical analysis pursuant to section 3.12 should be carried out on at least one DUT following completion of all the electrical tests.

3.10 Parameter check

A set of sensitive parameters called key parameters should be defined either in the component specifications or in consultation with the client, e.g. standby current consumption, operating currents, output voltages, contact resistances, input impedances, signal rates (rise and fall times) and bus specifications.

These parameters must be checked before the start and after the completion of each test to verify that they match the specification.

The key parameters must be measured and the functional behaviour of the components at T_{RT} and U_{48n} must be checked. For components with error memory, the error memory should be deleted before the test, read out and documented. After the test, it should be read out and documented again. The components must be inspected visually in accordance with DIN EN 13018 for external damage/changes, e.g. cracks, chipping/peeling, discolouration, distortion, etc., without opening the DUT.

Changes in the values of the key parameters, of functional behaviour, or of the error memory entries, and abnormalities in the visual inspection, must be evaluated regarding the preceding test loads as compared with the new status.

All the results must be documented in the test report.

3.11 Continuous parameter monitoring with drift analysis

The key parameters to be monitored must be recorded throughout the test. In the case of components with error memory, the error memory must be monitored continuously and entries must be documented in the test report. The data collected from the continuous parameter monitoring must be examined for trends and drifts in order to identify abnormalities, ageing or malfunctions of the component.

3.12 Physical analysis

For the physical analysis, the DUT must be opened and a visual inspection must be performed in accordance with DIN EN 13018.

Additional analyses (e.g. x-ray investigation and metallographic examination of the set-up and connecting technology) should be co-ordinated between the client and the contractor.

Any changes in the component relating to the new status must be evaluated. It should be shown that there is an unequivocal technical link between the malfunction identified in the test and the defect in the DUT identified by the following physical analysis.

If a DUT demonstrates abnormalities, the further analysis must, if applicable, be agreed with the client involving additional DUTs or the application of additional analytical methods.

The results must be documented and evaluated in the test report.

4 Electrical requirements and tests

4.1 E48-01a Long-term Overvoltage

4.1.1 Purpose

The component's resistance to long-term overvoltages is tested.

4.1.2 Test

Table 8: Testing parameters for E48-01a Long-term Overvoltage

DUT mode of operation	Modes II.a, II.b and II.c
t_0	Functional status A assumed
t_r	0.1 s
t_1	60 min
t_f	0.1 s
t_2	1 s
$U_{48\text{test}}$	$U_{48\text{r,dyn}}$
T_{test}	$T_{\max} - 20^\circ\text{C}$
Number of cycles	1
Number of DUTs	6

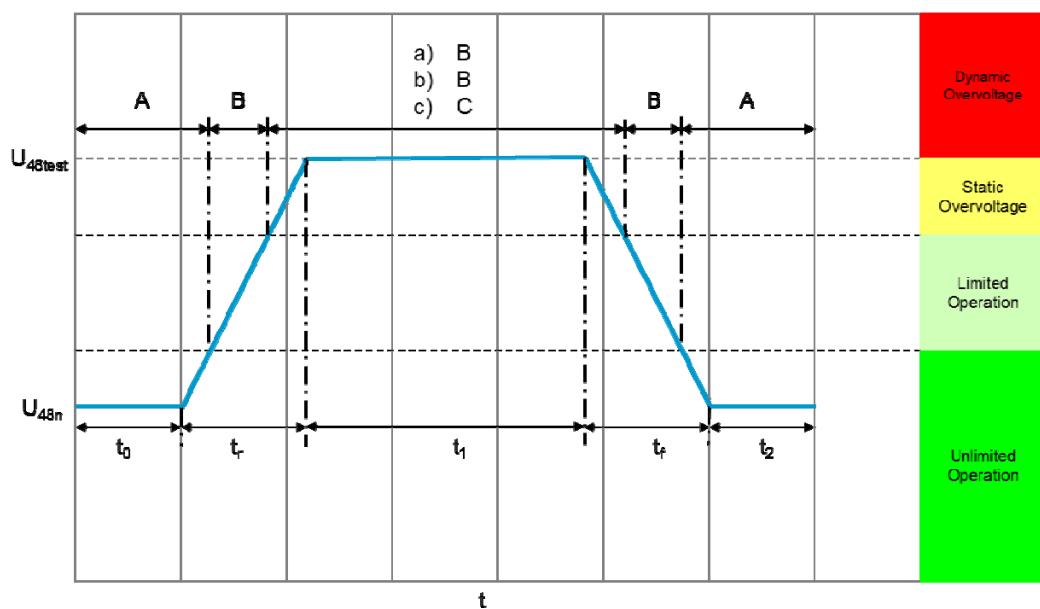


Figure 3: Test pulse for E48-01a Long-term Overvoltage

4.1.3 Requirement

Evaluation of the test result depends on how the component is used. Distinctions are made between:

- a) components that can convert significant amounts of electrical energy (e.g. ohmic loads):
functional status B;
- b) functions necessary during driving:
functional status B;
- c) for all other components:
functional status C.

4.2 E48-01b Overvoltage with Components that Return Electrical Energy

4.2.1 Purpose

The test is applicable to all components that return electrical energy, as they have to be equipped with a voltage-limiting function to ensure compliance with the voltage specification pursuant to section 2.5. The situation is replicated in which such a component feeds energy into the 48 V supply system, which cannot be absorbed in the vehicle power supply and therefore leads to an increase in the voltage.

4.2.2 Test Part 1

The DUT is connected to a powerful electrical source. The source must not act as a sink while the energy is being returned. A resulting feedback current $\leq 10 \text{ mA}$ is permitted. This should be demonstrated by measuring the current.

Table 9: Test parameters for E48-01b with Components that Return Electrical Energy, Part 1

DUT mode of operation	Mode II.c
T_{test}	T_{\min}, T_{RT} and T_{\max}
U_1	$U_{48\text{max},\text{unlimited}}$
U_2	U_{48r}
U_3	$U_{48\text{max},\text{high,limited}}$
t_0	$\geq 1 \text{ s}$ (the return of electrical energy begins after this time)
t_1	$\leq 300 \text{ ms}$
Number of cycles	3 cycles at all 3 temperatures
Number of DUTs	6

See “Figure 4: Test pulse for E48-01b Overvoltage with Components that Return Electrical Energy”.

4.2.3 Test Part 2

The DUT is connected to a powerful 4-quadrant amplifier and should be operated at U_1 for at least t_0 . After this, activation of the energy feedback begins and when the DUT's feedback current has reached its maximum, absorption of the returned energy should be terminated abruptly (t_{off}). A resulting feedback current ≤ 10 mA is permitted. This should be demonstrated by measuring the current.

Table 10: Test parameters for E48-01b Overvoltage with Components that Return Electrical Energy, Part 2

DUT mode of operation	Mode II.c
T_{test}	T_{min} , T_{RT} and T_{max}
U_1	$U_{48max,unlimited}$
U_2	U_{48r}
U_3	$U_{48max,high,limited}$
t_0	≥ 1 s
t_1	≤ 300 ms
t_{off}	≤ 10 μ s
Number of cycles	3 cycles at all 3 temperatures
Number of DUTs	6

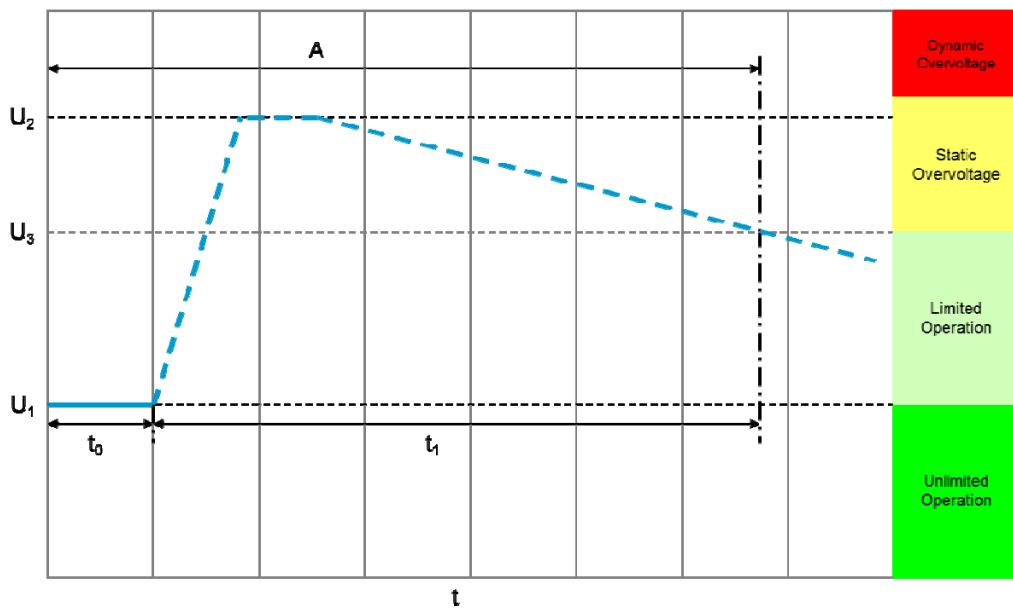


Figure 4: Test pulse for E48-01b Overvoltage with Components that Return Electrical Energy

4.2.4 Requirements for Part 1 and Part 2

Functional status A.

The time from exceeding the voltage U_1 to falling below the voltage U_3 should be determined and must not exceed t_1 .

4.3 E48-02 Transient Overvoltage

4.3.1 Purpose

Transient overvoltages can occur in the 48 V power supply. This test simulates such overvoltages.

4.3.2 Test

Table 11: Test parameters for E48-02 Transient Overvoltage

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	70 V
U_2	U_{48r}
t_0	100 ms
t_r	1 ms
t_1	40 ms
t_f	1 ms
t_2	600 ms
t_{3a}	2.5 s
t_{3b}	9 s
R_i	$10 \text{ m}\Omega \leq R_i \leq 100 \text{ m}\Omega$
Number of cycles	1. Short test: 3 times with t_{3a} 2. Endurance test: 1,000 times with t_{3b} The two tests are carried out in sequence.
Number of DUTs	6

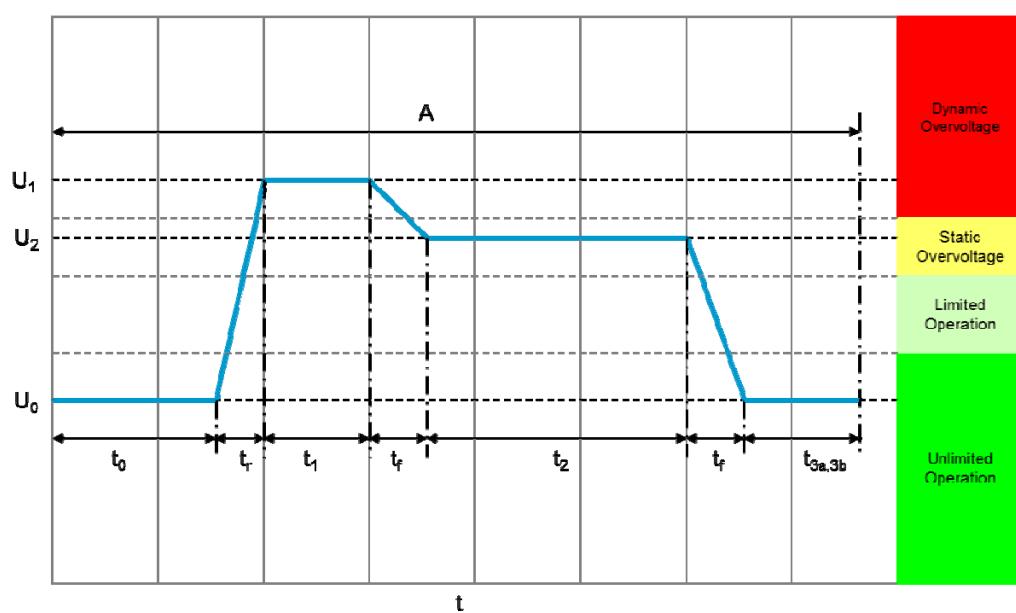


Figure 5: Test pulse for E48-02 Transient Overvoltage

4.3.3 Requirement

Functional status A

4.4 E48-03 Transient Event in Lower Limited Operation Range

4.4.1 Purpose

Switching on loads can cause transient undervoltages in the vehicle power supply. This test simulates such undervoltages.

4.4.2 Test

Table 12: Test parameters for E48-03 Transient Event in Lower Limited Operation Range

DUT mode of operation	Mode II.c
U_0	$U_{48\min,\text{unlimited}}$
U_1	$U_{48\min,\text{low,limited}}$
t_0	60 s
t_f	2 ms
t_1	500 ms
t_r	2 ms
t_2	500 ms
Number of cycles	1
Number of DUTs	6

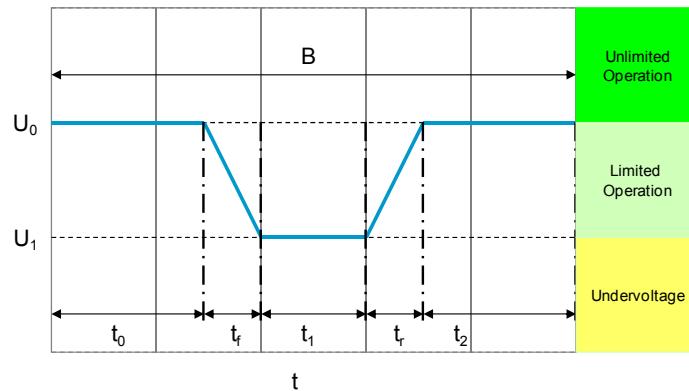


Figure 6: Test pulse for E48-03 Transient Event in Lower Limited Operation Range

4.4.3 Requirement

Functional status B

4.5 E48-04 Recuperation

4.5.1 Purpose

This test models a longer recuperation phase.

4.5.2 Test

Table 13: Test parameters for E48-04 Recuperation

DUT mode of operation	Mode II.c
U_0	$U_{48\text{max},\text{unlimited}}$
U_1	$U_{48\text{max},\text{high,limited}}$
t_0	60 s
t_r	100 ms
t_1	60 s
t_f	100 ms
t_2	60 s
Number of cycles	1
Number of DUTs	6

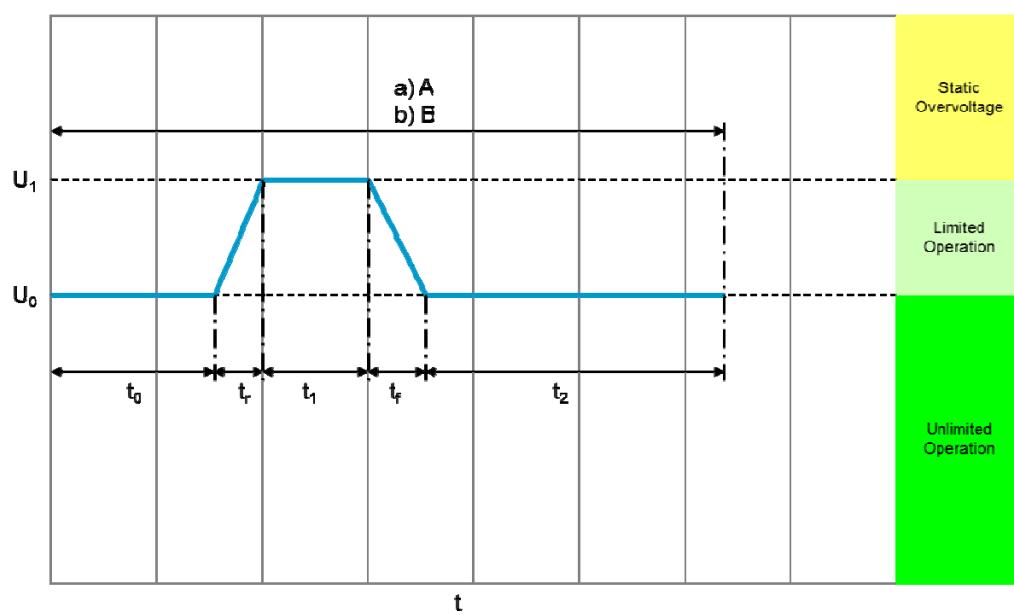


Figure 7: Test pulse for E48-04 Recuperation

4.5.3 Requirements

Evaluation of the test result depends on how the component is used. The following distinction is made:

- a) for components relevant to recuperation and driving:
functional status A;
- b) for all other components:
functional status B

4.6 E48-05 Superimposed Alternating Voltage

4.6.1 Purpose

Alternating voltages can be superimposed on the vehicle power supply. The superimposed alternating voltage can occur at any time during generator operation. This situation is simulated in this test.

4.6.2 Test Part 1

Table 14: Test parameters for E48-05 Superimposed Alternating Voltage, Part 1

DUT mode of operation	Mode II.c
R_i	$\leq 60 \text{ m}\Omega$ The maximum ripple current occurring here should be agreed with the client's specialist department.
$U_{48\text{test}}$	$U_{48\text{min},\text{unlimited}}$
t_{test}	30 min
f	F1: 15 Hz to 30 kHz F2: 30 kHz to 200 kHz
Wobble period	2 min
Wobble type	Triangle, logarithmic
$U_{48\text{pp}}$	For F1: 6 V $\pm 2\%$ (to be set before connection to DUT) For F2: 2 V $\pm 2\%$ (to be set before connection to DUT)
Number of DUTs	6

See "Figure 8: Test pulse for E48-05 Superimposed Alternating Voltage".

4.6.3 Test Part 2

Table 15: Test parameters for E48-05 Superimposed Alternating Voltage, Part 2

DUT mode of operation	Mode II.c
R_i	$\leq 60 \text{ m}\Omega$ The maximum ripple current occurring here should be agreed with the client's specialist department.
$U_{48\text{test}}$	$U_{48\text{max,unlimited}}$
t_{test}	30 min
f	F1: 15 Hz to 30 kHz F2: 30 kHz to 200 kHz
Wobble period	2 min
Wobble type	Triangle, logarithmic
$U_{48\text{pp}}$	For F1: $6 \text{ V} \pm 2 \%$ (to be set before connection to DUT) For F2: $2 \text{ V} \pm 2 \%$ (to be set before connection to DUT)
Number of DUTs	6

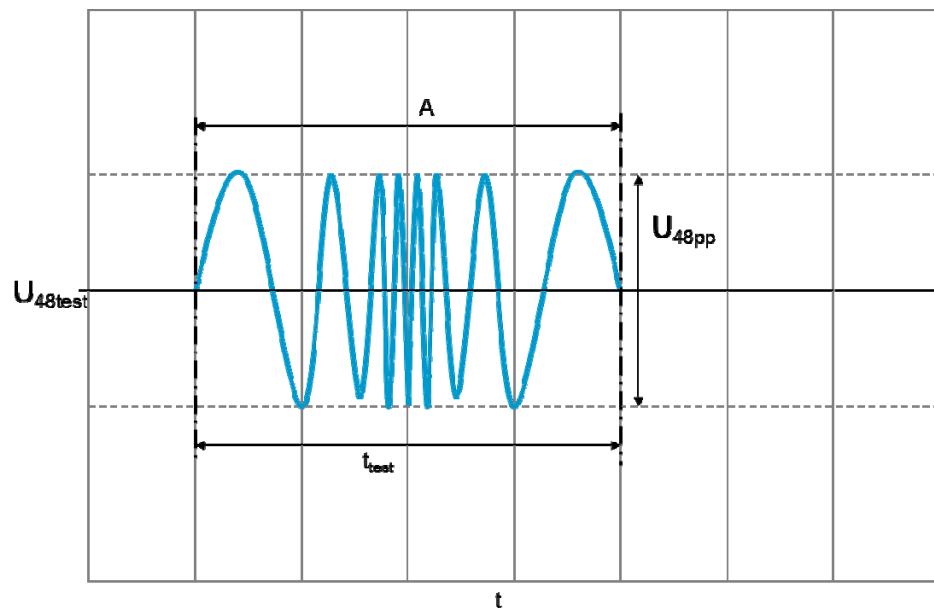


Figure 8: Test pulse for E48-05 Superimposed Alternating Voltage

4.6.4 Requirements for Part 1 and Part 2

Functional status A

4.7 E48-06 Slow Decrease and Increase of the Supply Voltage

4.7.1 E48-06a for Operation without Storage

4.7.1.1 Purpose

The test investigates slow decrease and increase of the supply voltage, as occurs during slow discharging and charging processes.

4.7.1.2 Test

Table 16: Test parameters for E48-06a Slow Decrease and Increase of the Supply Voltage

DUT mode of operation	Modes II.a and II.c
U_0	$U_{48\max,\text{unlimited}}$
Voltage gradient	$\pm 2 \text{ V/min}$
U_1	$U_{48\min,\text{unlimited}}$
U_2	0 V
t_1	Until the error memory has been read out completely
Number of cycles	1 cycle in mode of operation II.a 1 cycle in mode of operation II.c
Number of DUTs	6

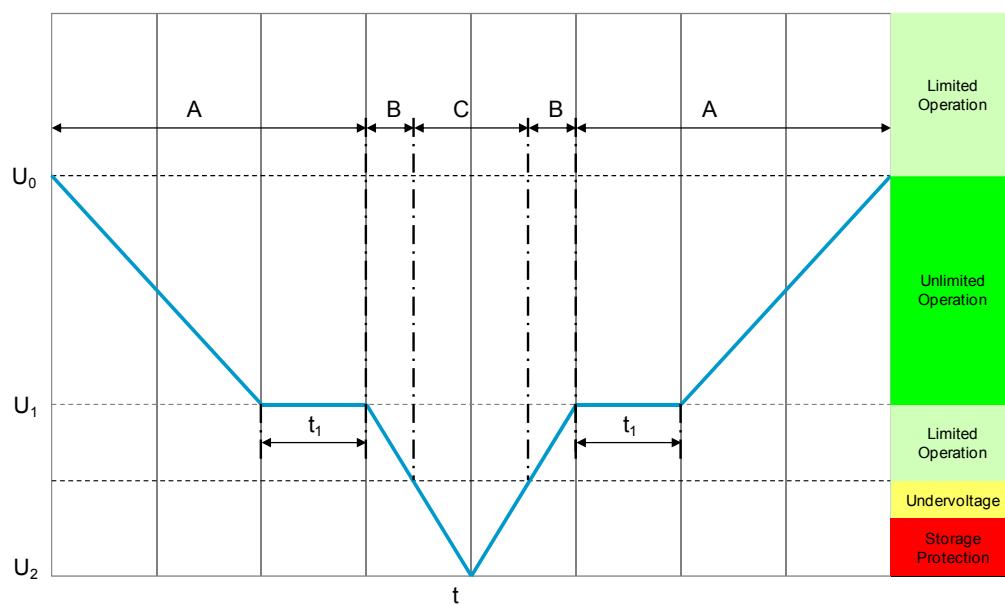


Figure 9: Test pulse for E48-06a Slow Decrease and Increase of the Supply Voltage

4.7.2 E48-06b for Operation with Storage, Part 1

4.7.2.1 Purpose

The test investigates slow decrease of the supply voltage to the storage protection voltage, after which the storage is disconnected.

4.7.2.2 Test

Table 17: Test parameters for E48-06b for Operation with Storage, Part 1

DUT mode of operation	Mode II.a
U_0	$U_{48\text{max},\text{unlimited}}$
U_1	$U_{48\text{min},\text{unlimited}}$
U_2	$U_{48\text{stopprotect}}$
U_3	0 V
t_0	100 ms
t_{f1}	8 min
t_1	≥ 60 s (during this phase the error memory is read out)
t_{f2}	8 min
t_2	60 s
t_{f3}	3 s
t_3	60 s
Number of cycles	1
Number of DUTs	6

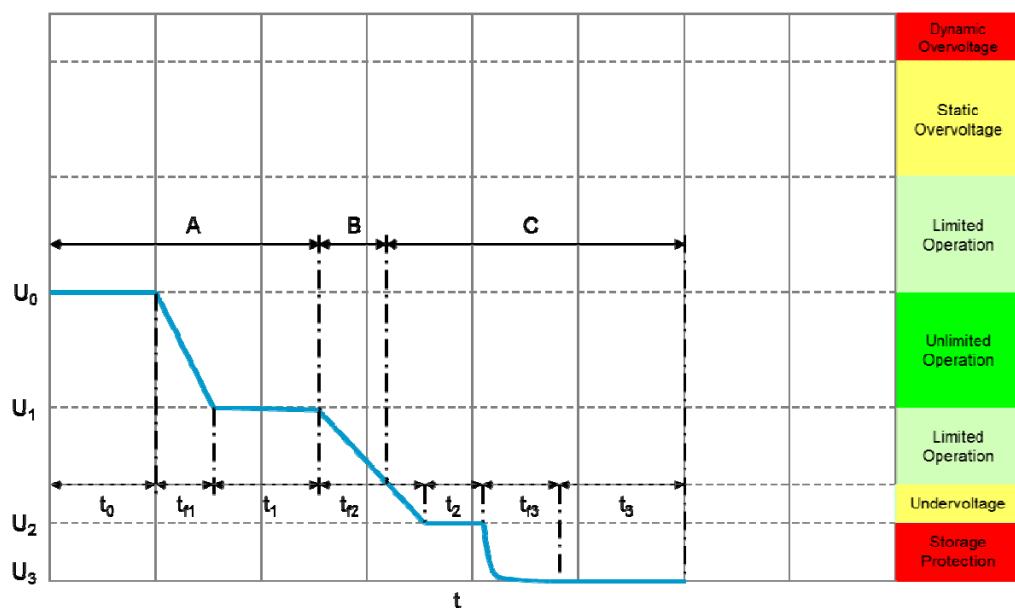


Figure 10: Test pulse for E48-06b for Operation with Storage, Part 1

Slow decrease of the supply voltage with disconnection of the storage.

4.7.3 E48-06c for Operation with Storage, Part 2

4.7.3.1 Purpose

The test examines connection of the generator while the storage is disconnected, followed by connection of the discharged storage.

4.7.3.2 Test

Table 18: Test parameters for E48-06c for Operation with Storage, Part 2

DUT mode of operation	Mode II.b after the final voltage has been reached
R_i	$\leq 60 \text{ m}\Omega$
U_0	0 V
U_1	U_{48n}
U_{48pp}	6 V at 10 kHz
U_2	$U_{48stoprotect}$
t_0	100 ms
t_{r1}	300 ms
t_1	$\geq 60 \text{ s}$ (during this phase the error memory is read out)
t_{f1}	1 ms
t_{r2}	14 min
t_3	100 ms
Number of cycles	1
Number of DUTs	6

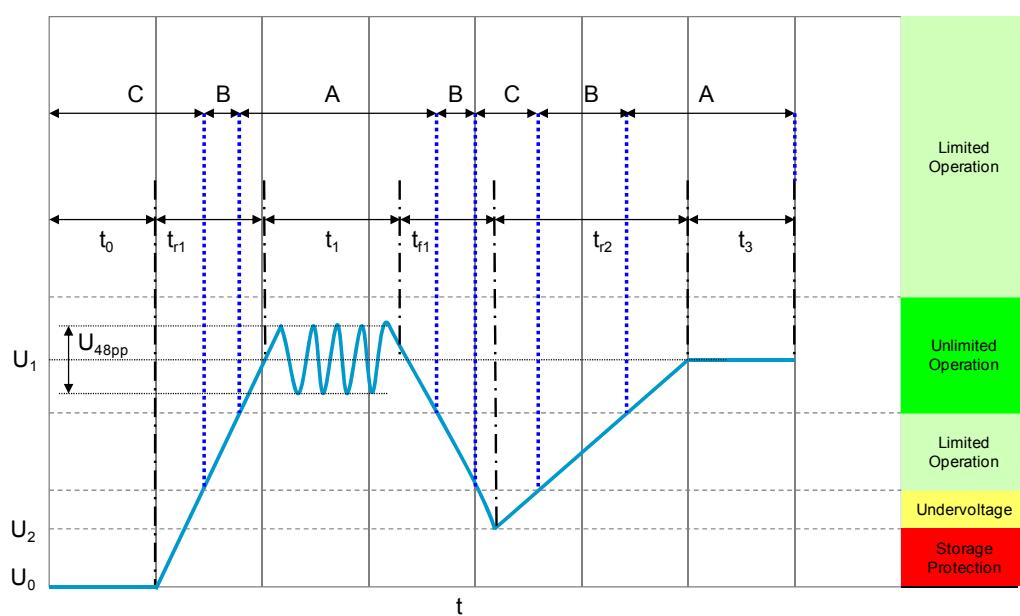


Figure 11: Test pulse E48-06c for Operation with Storage, Part 2

First the generator is connected, then the storage is connected.

4.7.4 Requirement

Evaluation of the test result depends on the voltage range applied to the component during the test, see Figure 9, Figure 10 and Figure 11.

4.8 E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage

4.8.1 Purpose

This test simulates slow decrease of the power supply voltage to the storage protection voltage followed by switching off to 0 V and abrupt reapplication of the storage voltage by means of either a charged storage or a new storage. Please note: The storage is not activated until after the vehicle power supply is connected (no contact bounce).

4.8.2 Test

Table 19: Test parameters for E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage

DUT mode of operation	Mode II.a
U_0	$U_{48\text{max},\text{unlimited}}$
U_1	$U_{48\text{min},\text{unlimited}}$
U_2	$U_{48\text{stopprotect}}$
U_3	0 V
U_4	U_{48n}
t_0	100 ms
t_{f1}	8 min
t_1	≥ 60 s (during this phase the error memory is read out)
t_{f2}	8 min
t_2	60 s
t_{f3}	3 s
t_3	300 s
t_{r1}	≤ 100 ms
t_4	100 ms
Number of cycles	1
Number of DUTs	6

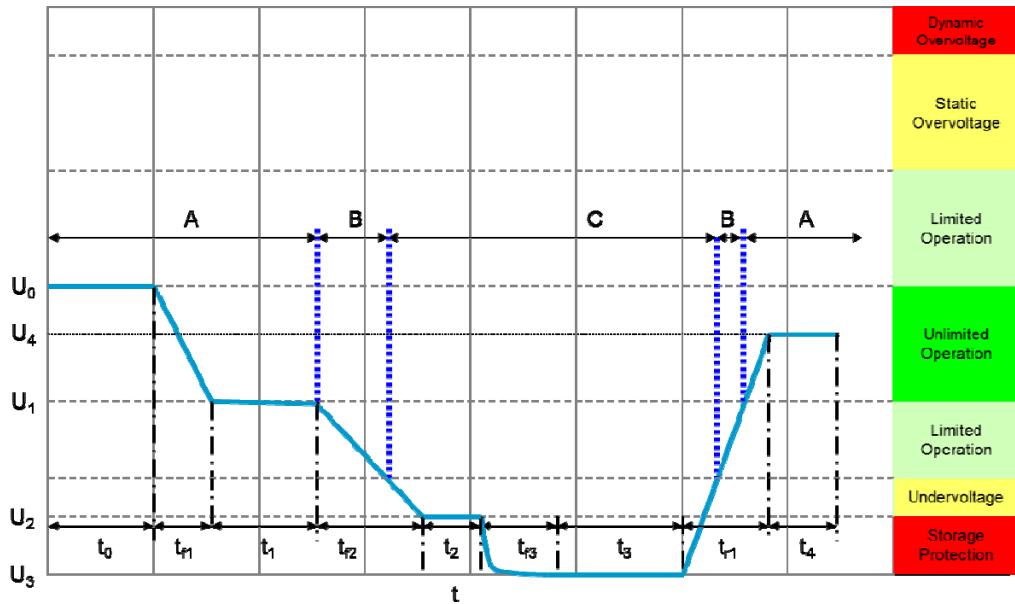


Figure 12: Test pulse for E48-07 Slow Decrease and Abrupt Increase of the Supply Voltage

4.8.3 Requirement

At the end of the test the system is in functional status A.

4.9 E48-08 Reset Behaviour

4.9.1 Purpose

The reset behaviour of a component (control device logic) is supplied from the 48 V system in its environment is modelled and tested. Test boundary conditions (e.g. assembly, terminal, and system) should be described in detail.

Any sequence of repeated powering on / off is possible during operation and must not lead to undefined behaviour of the component.

The reset behaviour is reflected in a voltage variance and can also vary over time. Two different test sequences are required to simulate a range of power-off times. A component has always to undergo both sequences.

The test is valid only for components with a logic supply from the 48 V system.

4.9.2 Test

Table 20: Test parameters for E48-08 Reset Behaviour

DUT mode of operation	Mode II.c
U_0	$U_{48\text{min},\text{unlimited}}$
ΔU_1 (range from U_0 to U_1)	2 V
U_1	$U_{48\text{min},\text{low},\text{limited}}$
ΔU_2 (range from $U_{48\text{min},\text{low},\text{limited}}$ to 0 V)	0.5 V
U_2	0 V
t_0	At least 10 s and until the DUT has regained 100% operability (all systems have restarted perfectly)
t_1 – test sequence 1	5 s
t_1 – test sequence 2	100 ms
$t_{f/r}$	≤ 100 ms (valid for all test pulses)
Number of cycles	1
Number of DUTs	6

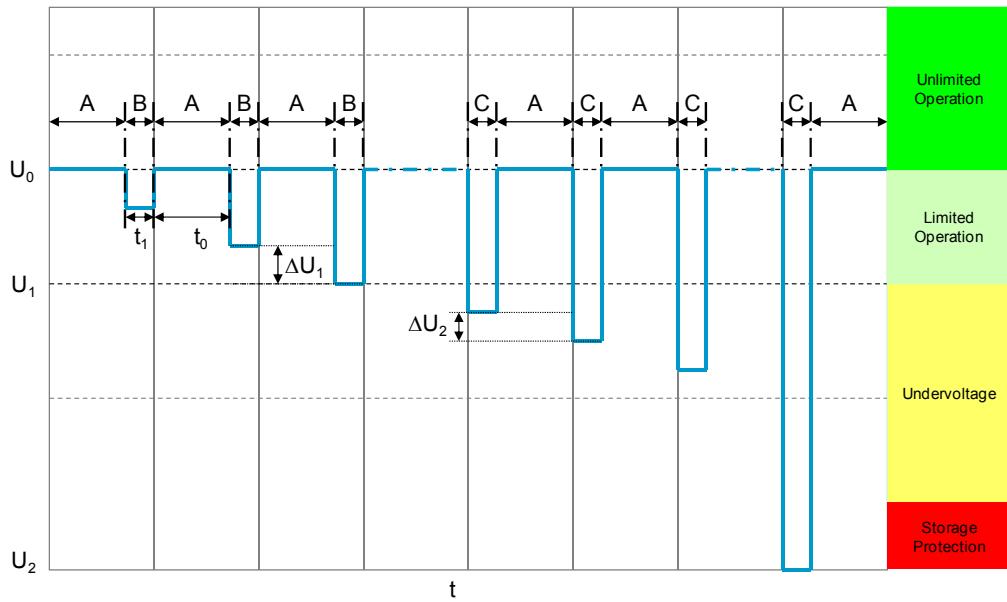


Figure 13: Test pulse for E48-08 Reset Behaviour

4.9.3 Requirements

- Functional status A when $U_{48\min,\text{unlimited}}$ is reached,
- Functional status B up to $U_{48\min,\text{low},\text{limited}}$,
- Functional status C below $U_{48\min,\text{low},\text{limited}}$.

Undefined modes of operation are never permitted.

Evidence of compliance with the specified threshold value should be provided, and the voltage at which the component initially exits functional status A should be recorded.

An undervoltage error entry should be demonstrated.

4.10 E48-09 Brief Interruptions

4.10.1 Purpose

The behaviour of the component when subjected to brief interruptions of varying duration is tested.

4.10.2 Test

Table 21: Test parameters for E48-09 Brief Interruptions

DUT mode of operation	Mode II.c									
Test set-up	Basic circuit according to Figure 15. The modelling of the vehicle power supply should be agreed with the client's specialist department.									
R_i	$\leq 60 \text{ m}\Omega$ incl. switch S1									
R	$\leq 100 \text{ m}\Omega$ total resistance incl. layout of wiring harness and switch S2									
Z_1	S1 closed and S2 open									
Z_2	S1 open and S2 closed									
$U_{48\text{test}}$	U_{48n}									
t_1	<p>The supply voltage of $U_{48\text{test}}$ is interrupted at varying intervals in the following sequence:</p> <table border="1"> <tbody> <tr> <td>$100 \mu\text{s}$ to 1 ms</td> <td>$100 \mu\text{s}$ intervals</td> </tr> <tr> <td>1 ms to 10 ms</td> <td>1 ms intervals</td> </tr> <tr> <td>10 ms to 100 ms</td> <td>10 ms intervals</td> </tr> <tr> <td>100 ms to 2 s</td> <td>100 ms intervals</td> </tr> </tbody> </table>		$100 \mu\text{s}$ to 1 ms	$100 \mu\text{s}$ intervals	1 ms to 10 ms	1 ms intervals	10 ms to 100 ms	10 ms intervals	100 ms to 2 s	100 ms intervals
$100 \mu\text{s}$ to 1 ms	$100 \mu\text{s}$ intervals									
1 ms to 10 ms	1 ms intervals									
10 ms to 100 ms	10 ms intervals									
100 ms to 2 s	100 ms intervals									
t_2	<p>$> 10 \text{ s}$</p> <p>The test voltage $U_{48\text{test}}$ must be maintained at least long enough for the DUT to become 100% operational again (all systems have restarted perfectly).</p>									
t_f	$\leq 10 \mu\text{s}$									
t_r	$\leq 10 \mu\text{s}$									
Number of cycles	1									
Number of DUTs	6									

The duration of the voltage failure increases by the increments given in Table 21. This results in a scheme as shown in "Figure 14: Test pulses for E48-09 Brief Interruptions".

In each case one reference measurement should be performed and documented with $1 \text{ k}\Omega$ ($\pm 5 \%$) and one with 10Ω ($\pm 5 \%$) as a DUT substitute. Verification of the steepness of the slope should be provided with this set-up. Low-inductance components should be used as resistors.

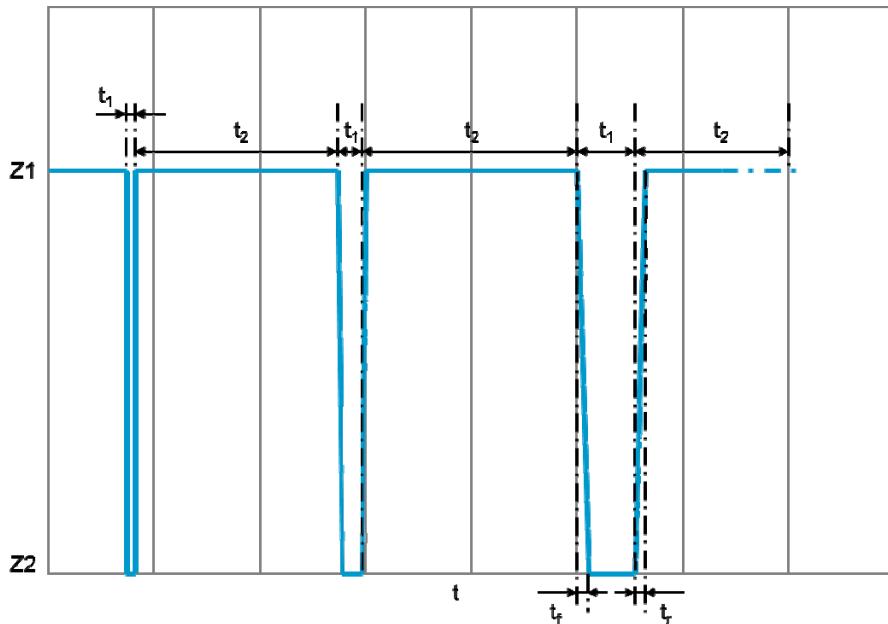


Figure 14: Test pulses for E48-09 Brief Interruptions

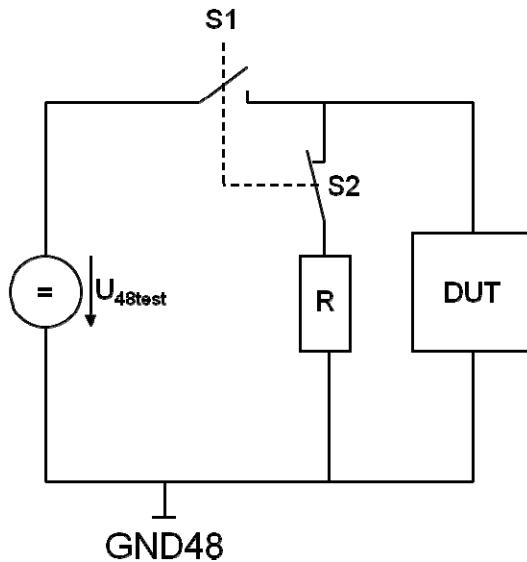


Figure 15: Basic circuit for E48-09 Brief Interruptions

4.10.3 Requirements

The time t_1 after which the DUT initially departs from functional status A must be recorded.

The test is deemed to have a positive result if the DUT achieves functional status A when $t_1 \leq 100 \mu\text{s}$, but otherwise achieves functional status C. A different value for the permissibility of functional status C should be defined in the component specifications.

4.11 E48-10 Starting Pulses

4.11.1 Purpose

In the case of a cold start (starting the engine), the storage voltage falls to a low value for a short period, after which it rises again. In the case of a warm start, the voltage does not depart from the range with unlimited operation, and is not considered here.

4.11.2 Test

Table 22: Test parameters for E48-10 Starting Pulses

DUT mode of operation	a) For components relevant to starting: mode II.c b) For components not relevant to starting: mode II.b
Test pulse	Test pulse “normal” and “severe”
U_0	U_{48n} for cold start normal 40 V for cold start severe
U_1	$U_{48\min,\text{low},\text{limited}}$
t_0	2 s
t_f	1 ms
t_1	1 s
t_r	1 ms
t_2	2 s
Number of cycles	10
Number of DUTs	6

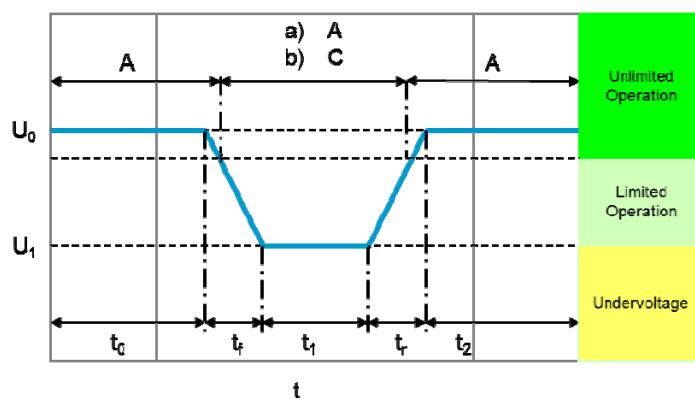


Figure 16: Test pulse: E48-10 Starting Pulses

4.11.3 Requirements

No entries may be made in the error memory.
It must always be possible to start the vehicle.

4.11.3.1 Components relevant to starting (a)

Test pulse "normal": functional status A
Test pulse "severe": functional status A

4.11.3.2 Components not relevant to starting (b)

Test pulse "normal": functional status C
Test pulse "severe": functional status C

4.12 E48-11 Ground Loss in 48 V Power Supply

4.12.1 Purpose

The test simulates a loss of ground by a component in the 48 V power supply system, which is supplied solely from the 48 V system and has interfaces to 12/24 V components (e.g. CAN, LIN, or FlexRay bus or other analogue or digital signal lines).

Care must be taken to ensure that the loss of ground by the 48 V system component does not disrupt the other communication participants in the 12/24 V system (e.g. through excessive voltages or reversed polarity). It must also be ensured that the loss of ground does not destroy any components.

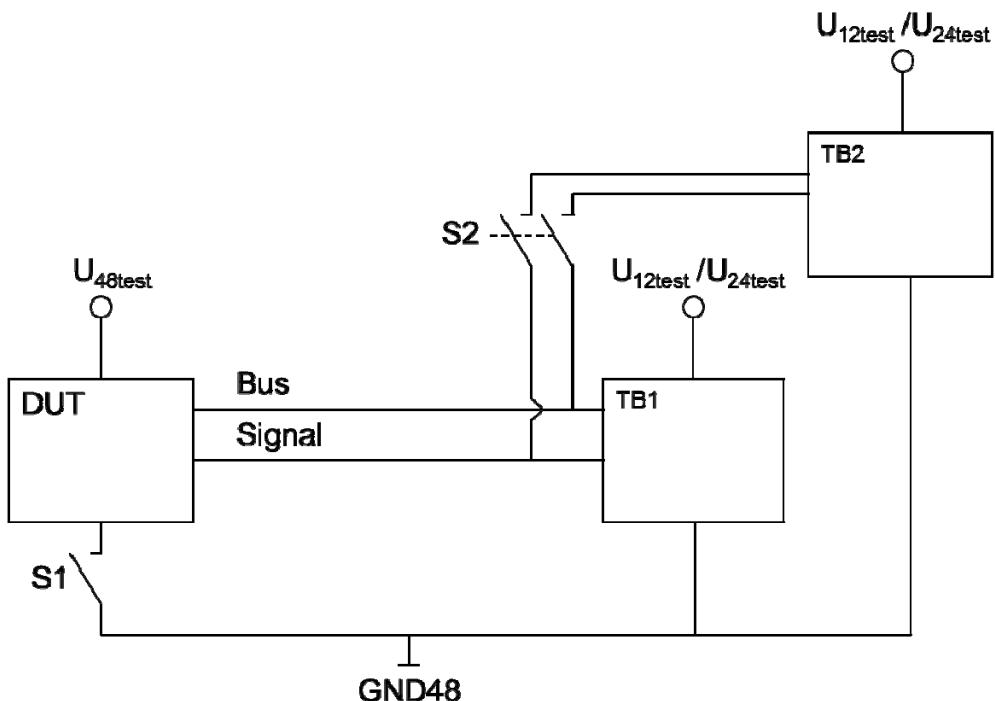
4.12.2 Test, general

- The 48 V system device under test (DUT) is connected to the test apparatus, to its components TB1 (subsystem 1) and TB2 (subsystem 2) (see Figure 17).
- All signal and bus lines of the DUT are connected to TB1 and TB2:
 - o Signals sent by the DUT are distributed to TB1 and TB2.
 - o Signals received by the DUT are sent by TB1.
- TB1 and TB2 simulate the restbus, and with their interface components they satisfy the requirements of the component specifications (automotive-qualified and released interface components).
- Bus communication is established between TB1 and TB2, which is:
 - o high-performance and
 - o bidirectional,
 - o has a message counter and is verified with a CRC, and
 - o is monitored (any errors are immediately recognised and logged).
- The signal lines between DUT and TB1/TB2 are:
 - o monitored in TB1 and TB2 (signal content);
 - o any errors are recognised and logged in TB1/TB2.
- The voltages and currents of all communication lines (bus and signal lines) should be monitored in or at TB1 and TB2 for exceedances of the specification limits.

The details are co-ordinated with the person responsible for the component specifications.

Table 23: Test parameters for E48-11 Ground Loss in 48 V Power Supply

DUT mode of operation	Mode II.c
t_{test}	See tests
U_{48test}	U_{48n}
T_{test}	$T_{max} - 20 \text{ }^{\circ}\text{C}$
Number of cycles per test	1
Number of DUTs	6

**Figure 17: Basic circuit diagram for E48-11 Ground Loss in 48 V Power Supply**

4.12.3 Test 1

S1 closed

S2 closed

All the components DUT/TB1/TB2 function perfectly.

S2 is opened.

4.12.4 Requirements 1

Errors in TB1 and TB2 must be logged:

- TB1: bus communication with TB2 disrupted
- TB2: bus communication with TB1 disrupted
- TB2: signal lines disrupted

No errors in the DUT – functional status A.

4.12.5 Test 2

S1 closed.

S2 closed.

All the components DUT/TB1/TB2 function perfectly.

S1 is opened.

The test lasts for 30 minutes after S1 is opened.

4.12.6 Requirements 2

In TB1 and TB2, no voltages may occur that are greater than the defined interface voltages and no currents may occur that are greater than the defined interface current. This applies to all bus and signal lines.

Bus communication: the bus communication between TB1 and TB2 functions perfectly – there are no errors in the error memory.

Signal line:

Distinction:

- a) DUT reads this line, i.e. TB1 is the sender.

Requirement: no error entry in TB1 or TB2.

- b) DUT is the sender.

Requirement: error entry in TB1 and TB2 owing to loss of signal.

4.13 E48-12 Ground Offset

4.13.1 Purpose

For components with several subsystems, potential differences can arise between the individual supply points. A potential difference from ground of up to ± 1.0 V must not influence the component's function.

4.13.2 Test

If the DUT has several voltage and ground connections for the 48 V power supply, the test must be performed separately for each connection point. In general, a ground offset of ± 1.0 V should be taken into consideration when dimensioning the interface between two components. The component is connected as shown in Figure 18.

Table 24: Test parameters for E48-12 Ground Offset

DUT mode of operation	Mode II.c
$U_{48\text{test}}$	U_{48n}
U_0	1.0 V
Number of cycles	Both switch positions
Number of DUTs	At least 6

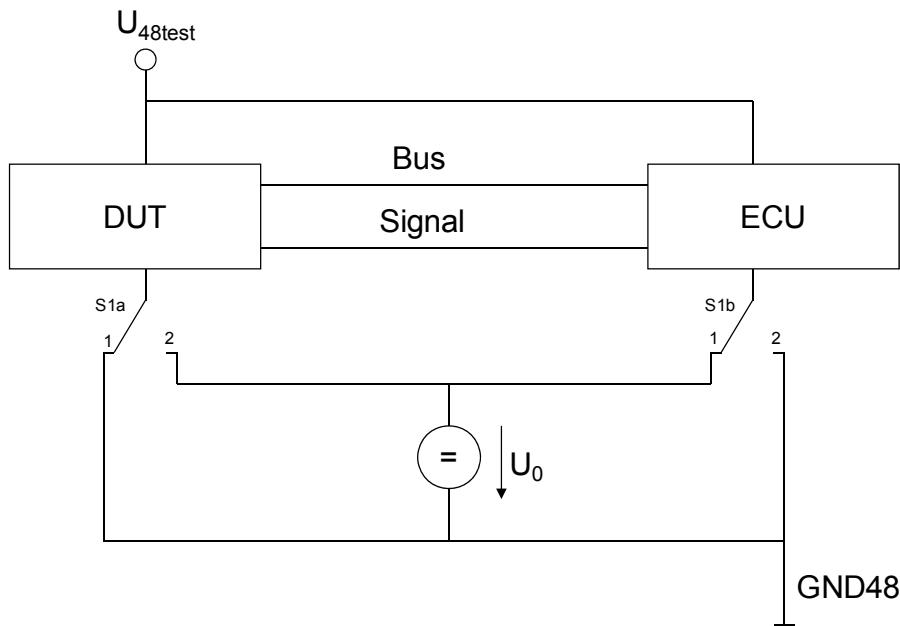


Figure 18: Basic circuit diagram for E48-12 Ground Offset (U_{B48})

4.13.3 Requirement

Functional status A

4.14 E48-13 Internal Dielectric Strength

4.14.1 Purpose

The test determines the steady-state internal dielectric strength between 48 V system pins and 12/24 V system pins, if both voltages are used in one component.

4.14.2 Test

Table 25: Test parameters for E48-13 Internal Dielectric Strength

DUT mode of operation	Mode I.a
$U_{48\text{test}}$	$U_{48\text{r,dyn}}$
t_{test}	60 min
F_{rel}	50 %
T_{test}	35 °C
Test points	Application of the test voltage between – both supply connections, – additional test points agreed with the relevant client department. See Figure 19
Number of cycles	1
Number of DUTs	6

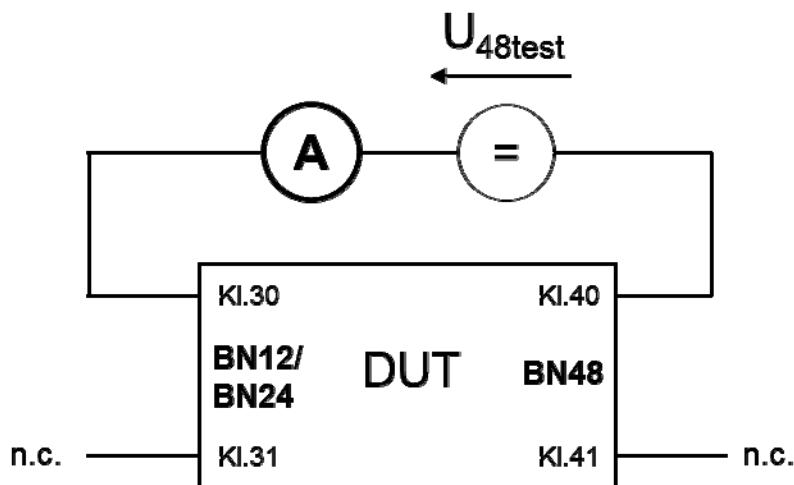


Figure 19: Basic circuit diagram for E48-13 Internal Dielectric Strength

4.14.3 Requirement

The resistance resulting from the required dielectric strength must be at least $1 \text{ M}\Omega$. It must be shown that the DUT has not suffered any damage. After the test, functional status A should be demonstrated.

4.15 E48-14 Standby Current

4.15.1 Purpose

The standby current consumption is determined for components relevant to standby current.

4.15.2 Test

For components with post-run function (e.g. the cooling fan), the standby current consumption should be determined after this function has ceased.

Table 26: Test parameters for E48-14 Standby Current

DUT mode of operation	Mode II.a	
$U_{48\text{test}}$	U_{48n}	
Test condition	Temperature range	Max. standby current
	T_{\min} to 40 °C	0.1 mA
	40 °C to T_{\max}	0.2 mA
T_{test}	T_{\min} , T_{RT} and T_{\max}	
Number of DUTs	6	

4.15.3 Requirement

The target for all DUTs is a standby current consumption of 0 mA. The test should be evaluated separately for all three test temperatures.

Post-run functions should be approved by client's specialist department responsible for standby current management.

4.16 E48-15 Operation in Unlimited Operation Range

4.16.1 Purpose

The operating behaviour at the boundaries is tested.

4.16.2 Test

Table 27: Test parameters for E48-15 Operation in Unlimited Operation Range

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	$U_{48\min,\text{unlimited}}$
U_2	$U_{48\max,\text{unlimited}}$
t_0	100 ms
t_{f1}	1 ms
t_1	1 s
t_r	1 s
t_2	10 s
t_{f2}	1 s
t_3	100 ms
T_{test}	$T_{\max}, T_{\text{RT}} \text{ and } T_{\min}$
Number of cycles	10
Number of DUTs	6

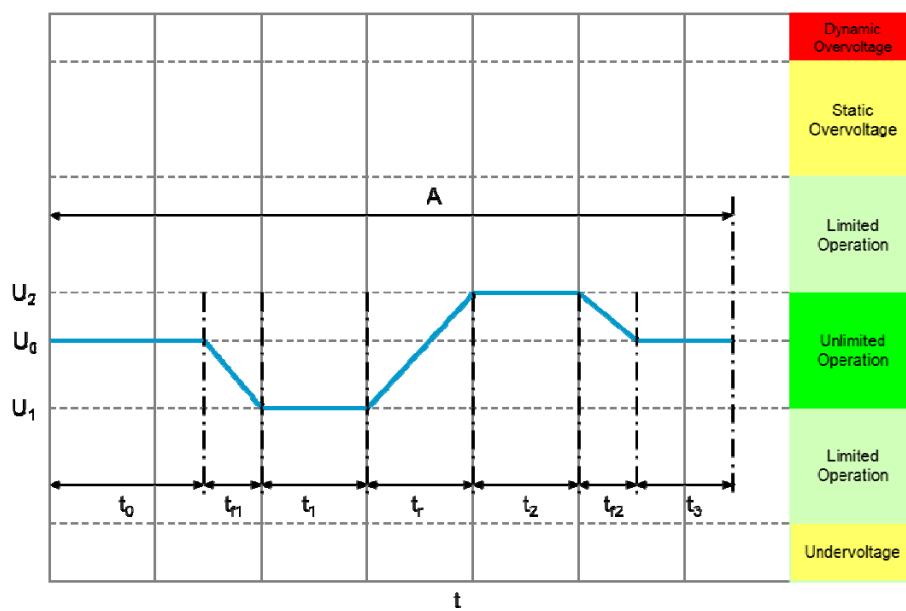


Figure 20: Test pulse for E48-15 Operation in Unlimited Operation Range

4.16.3 Requirement

Functional status A

4.17 E48-16 Operation in Upper Limited Operation Range

4.17.1 Purpose

Operating behaviour is examined, switching between unlimited and limited operation and at the boundaries.

4.17.2 Test

Table 28: Test parameters for E48-16 Operation in Upper Limited Operation Range

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	$U_{48\max,\text{high},\text{limited}}$
U_2	$U_{48\max,\text{unlimited}}$
U_3	$U_{48\max,\text{unlimited}} + 1 \text{ V}$
t_0	100 ms
t_{r1}	4 s
t_1	10 s
t_{f1}	2 s
t_2	10 s
t_{r2}	2 s
t_3	10 s
t_{f2}	2 s
t_4	100 ms
T_{test}	T_{\max} , T_{RT} and T_{\min}
Number of cycles	10
Number of DUTs	6

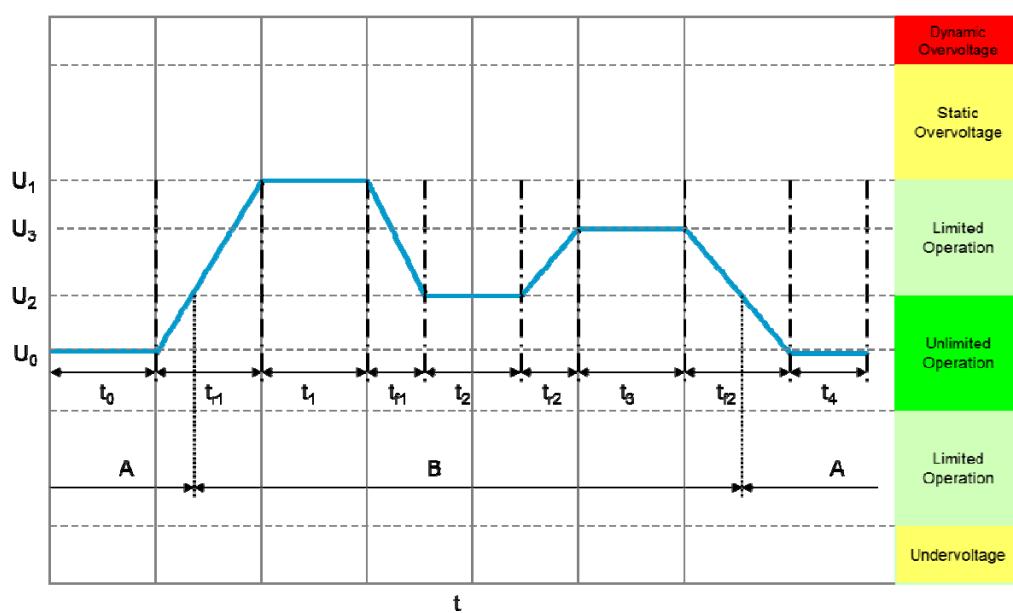


Figure 21: Test pulse for E48-16 Operation in Upper Limited Operation Range

4.17.3 Requirement

See Figure 21. No errors are logged in the error memory.

4.18 E48-17 Operation in Lower Limited Operation Range

4.18.1 Purpose

Operating behaviour is examined, switching between unlimited and limited operation and at the boundaries.

4.18.2 Test

Table 29: Test parameters for E48-17 Operation in Lower Limited Operation Range

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	$U_{48\min,\text{low},\text{limited}}$
U_2	$U_{48\min,\text{unlimited}}$
U_3	$U_{48\min,\text{low},\text{limited}} + 1 \text{ V}$
t_0	100 ms
t_{f1}	2 s
t_1	10 s
t_{r1}	4 s
t_2	10 s
t_{f2}	2 s
t_3	10 s
t_{r2}	2 s
t_4	100 ms
T_{test}	T_{\max} , T_{RT} and T_{\min}
Number of cycles	10
Number of DUTs	6

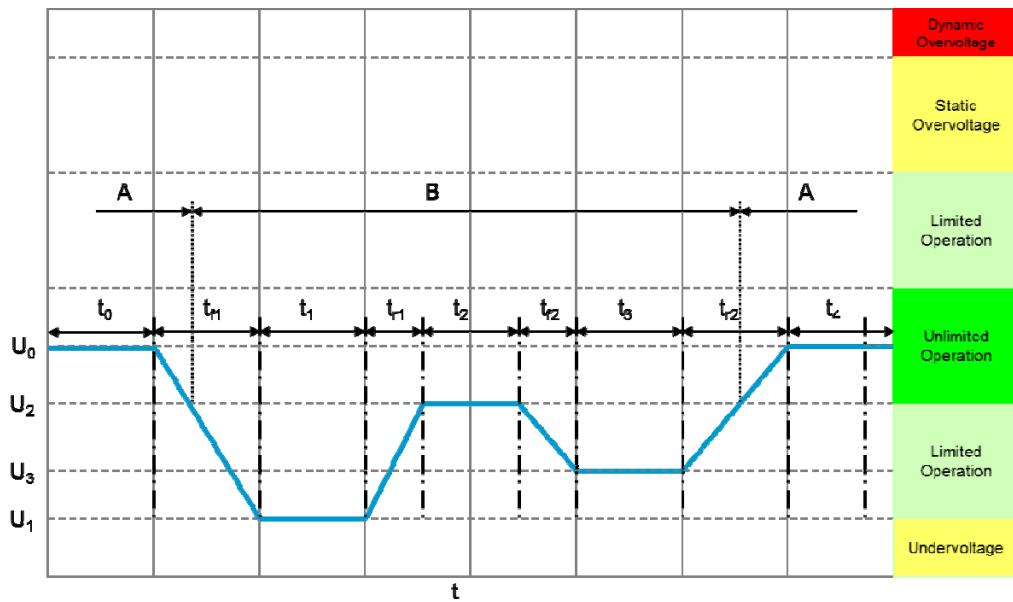


Figure 22: Test pulse for E48-17 Operation in Lower Limited Operation Range

4.18.3 Requirement

See Figure 22: No errors are logged in the error memory.

4.19 E48-18 Overvoltage Range

The test should investigate switching off a load while the storage is being charged and switching the operating behaviour between unlimited and limited operation, into the overvoltage range.

4.19.1 Test

Table 30: Test parameters for E48-18 Overvoltage Range

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	U_{48r}
U_2	$U_{48\max,\text{unlimited}} + 1 \text{ V}$
t_0	100 ms
t_{r1}	10 ms
t_1	1 s
t_{f1}	1 s
t_2	10 s
t_{r2}	1 ms
t_3	2 s
t_{f2}	1 s
t_4	5 s
t_{r3}	10 s
t_5	2 s
t_{f3}	10 s
t_6	100 ms
T_{test}	T_{\max}, T_{RT} and T_{\min}
Number of cycles	10
Number of DUTs	6

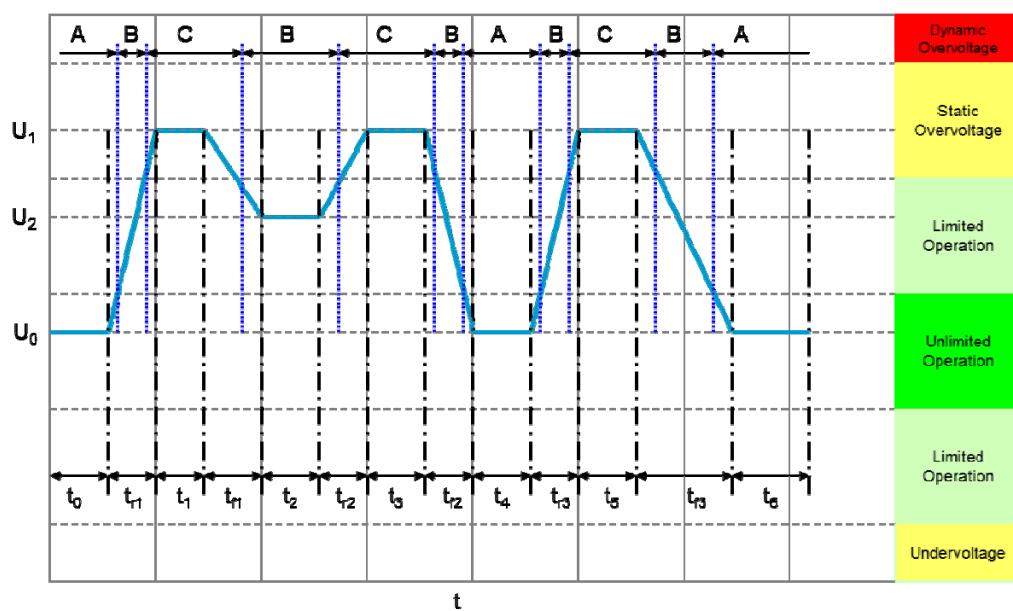


Figure 23: Test pulse for E48-18 Overvoltage Range

4.19.2 Requirements

See “Figure 23: Test pulse for E48-18”.

4.20 E48-19 Undervoltage Range

4.20.1 Purpose

The test investigates switching the operating behaviour between unlimited and limited operation, into the undervoltage range.

4.20.2 Test

Table 31: Test parameters for E48-19 Undervoltage Range

DUT mode of operation	Mode II.c
U_0	U_{48n}
U_1	$U_{48stopprotect}$
U_2	$U_{48min,low,limited} + 6 \text{ V}$
t_0	100 ms
t_{f1}	1 s
t_1	1 s
t_{r1}	10 ms
t_2	10 s
t_{f2}	1 s
t_3	2 s
t_{r2}	1 ms
t_4	5 s
t_{f3}	10 s
t_5	2 s
t_{r3}	10 s
t_6	100 ms
T_{test}	T_{max} , T_{RT} and T_{min}
Number of cycles	10
Number of DUTs	6

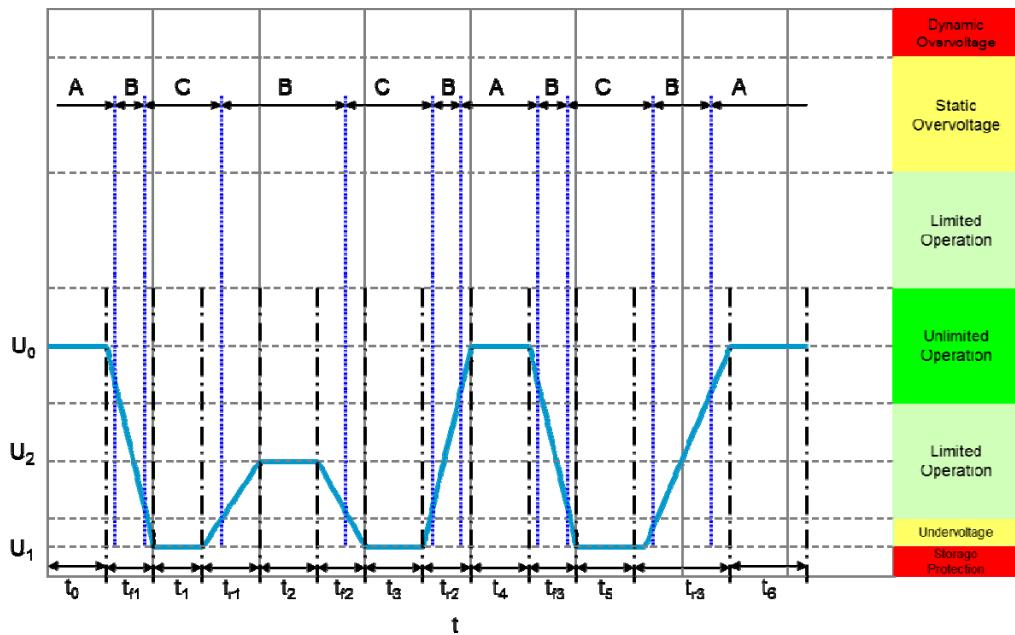


Figure 24: Test pulse for E48-19 Undervoltage Range

4.20.3 Requirement

See Figure 24: Test pulse for E48-19 .

4.21 E48-20a Fault Current, Part 1

4.21.1 Purpose

The fault current resistance of a component with connections to both vehicle power supplies (12/24 V and 48 V) is examined and thus its immunity to disruption by other components.

4.21.2 Test

The DUT is connected to the test apparatus as shown in “Figure 25: Basic circuit diagram for E48-20a Fault Current, Part 1”.

The switch S1 is open (terminal 41 is disconnected).

Terminal 40 is supplied (behaviour is tested at two different voltages).

The 12/24 V part of the component is supplied.

The current flowing through terminal 40 on the component should be measured.

Table 32: Test parameters for E48-20a Fault Current, Part 1

DUT mode of operation	Mode II.a
Test set-up	See Figure 25
$U_{48\text{test}}$	a) U_{48n}
	b) $U_{48r,\text{dyn}}$
t_{test}	10 min
T_{test}	T_{RT}
Number of cycles	1
Number of DUTs	6

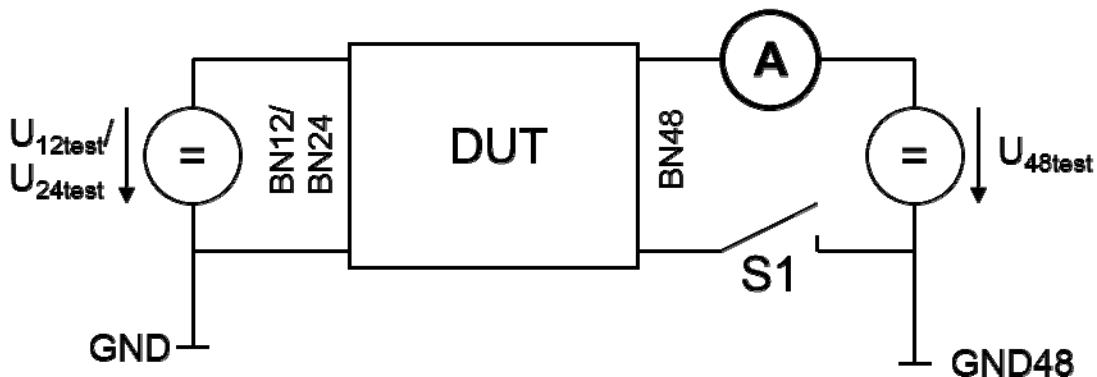


Figure 25: Basic circuit diagram for E48-20a Fault Current, Part 1

4.21.3 Requirement

For the terminal 40 supply current: $|I| \leq 1 \mu\text{A}$

4.22 E48-20b Fault Current, Part 2

4.22.1 Purpose

The fault current resistance of a component with connections to both vehicle power supplies (12/24 V and 48 V) is examined.

4.22.2 Test

The DUT is connected to the test apparatus as shown in “Figure 26: Basic circuit diagram for E48-20b Fault Current, Part 2”.

All 12/24 V contacts (supply and communication) are connected with one another (short circuited).

All 48 V contacts (supply) are connected with one another (short circuited).

A test voltage of U_{test} is applied between the 48 V and the 12/24 V supply systems.

The current then flowing through the component should be measured.

Table 33: Test parameters for E48-20b Fault Current, Part 2

Test set-up	See Figure 26
U_{test}	70 V
t_{test}	10 min
T_{test}	T_{RT}
Number of cycles	1
Number of DUTs	6

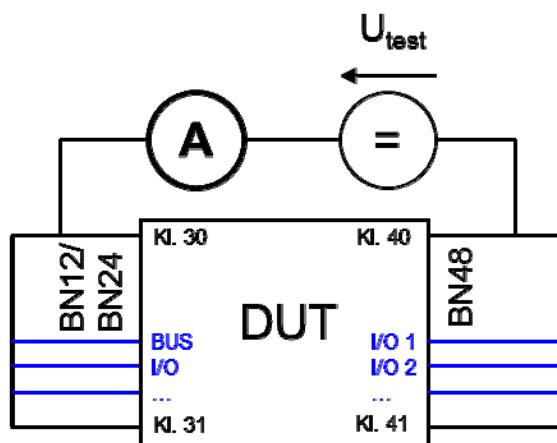


Figure 26: Basic circuit diagram for E48-20b Fault Current, Part 2

4.22.3 Requirement

For the current between the 12/24 V and 48 V systems: $|I| \leq 1 \mu\text{A}$

4.23 E48-21 Short Circuit in Signal Line and Load Circuit

4.23.1 Purpose

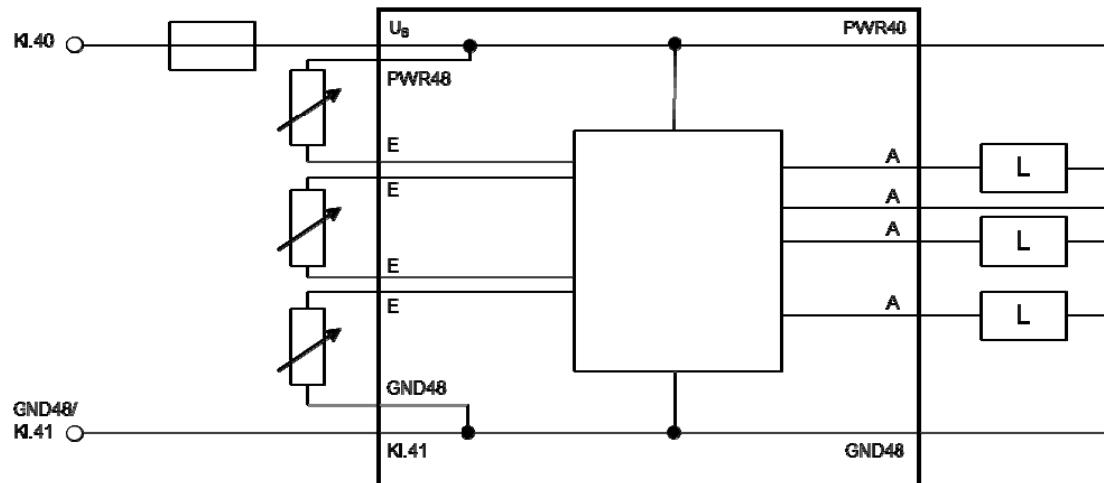
Short circuits on all 48 V system device inputs and outputs are examined, as are short circuits in the 48 V system load circuit. Any 12/24 V part present is not tested. All 48 V supply system inputs and outputs should be designed to be short-circuit proof with respect to the test voltage and GND48. The following tests should be performed:

- with activated and non-activated outputs,
- without voltage supply,
- without ground connection.

4.23.2 Test

Table 34: Test parameters for E48-21 Short Circuit in Signal Line and Load Circuit

DUT mode of operation	Mode II.c
Test duration	Short circuit of each 48 V system pin individually for 60 s to test voltage and GND48
Test voltage	$U_{48\text{max},\text{unlimited}}$ and $U_{48\text{min},\text{unlimited}}$
Test set-up	The power supply used for the test must be able to supply the short-circuit currents expected from the component.
Number of cycles	Each pin, once against the test voltage/terminal 40 and once against GND48/ terminal 41
Number of DUTs	6

**Legend**

- L Load
- E Input
- A Output
- PWR48 Output U_B /terminal 40
- GND48 Input/output terminal 41
- U_B 48 V power supply to the DUT

Figure 27: Basic circuit diagram for E48-21 Short Circuit in Signal Line and Load Circuit

4.23.3 Requirements

The following functional statuses must be achieved for a successful test outcome:

- for inputs and outputs (E and A): functional status C
- for supply voltages (PWR48): functional status D
- for device ground (GND48): functional status E