CS & IT ENGINEERING

Computer Organization Architecture

IO Organization

DPP- 01 Discussion Notes

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[NAT]

#Q. 8-bit characters are transmitted using a synchronous mode of transmission with 1 start bit, 8 data bits and 1 stop bit. The efficiency of the transmission line is ____?

$$\text{efficiency} = \frac{8}{8+1+1} = \frac{8}{10} = \underline{\underline{0.8}} \quad \text{Ans.}$$

[NAT]

Ans = 250

#Q. 8-bit characters are transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit. If the transfer rate of the line is 3000 bits per second, then effective transfer rate is _____ bytes per second?

Eff. transfer rate = efficiency * actual rate

$$= \frac{8}{8+1+2+1} * 3000 \text{ bits/sec}$$

$$= \frac{8}{12} * 3000 \text{ bits/sec}$$

$$= \frac{8 * 3000}{12 * 8} \text{ bytes/sec} = 250 \text{ bytes/sec}$$

[NAT]

Ans = 0.55

#Q. Consider a CPU which takes 0.05 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 5 cycles to service the interrupt. If CPU runs on 10MHz clock rate then total time CPU spends for interrupt service is _____ microseconds (rounded upto 2 decimal places)?

= overhead time + service time

= 0.05 μsec + 5 cycles

= 0.05 μs + $5 * \frac{1}{10\,MHz}$ = 0.55 μsec

[MCQ]

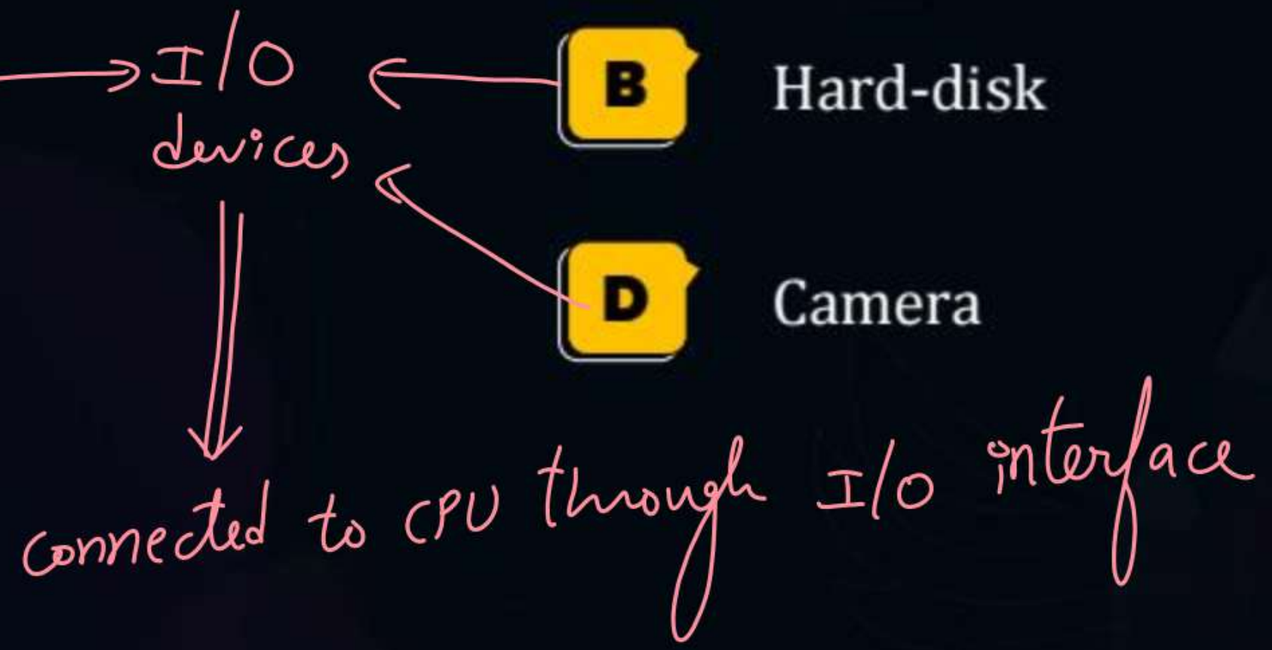
#Q. Which of the following is connected to CPU directly?

A Keyboard

B Hard-disk

C RAM

D Camera



[MCQ]

#Q. Which of the following is/are true?

(1) Data format used in IO devices may differ from CPUs format

(2) IO devices are slower than CPU

(3) IO devices are slower than main memory

A Only 1

B Only 1 & 2

C Only 1 & 3

D All 1, 2 & 3

[MCQ]

#Q. Which of the following is true regarding IO mapped IO as compared to memory mapped IO?

(1) ALU operation cannot be performed on IO data directly

(2) IO devices have their own address space

(3) Less number of Instructions to access IO

(4) Less number of IO devices connected

A Only 2 & 3

B Only 2 & 4

C Only 2, 3 & 4

D All 1, 2, 3 & 4

[MCQ]

#Q. Which of the following is true regarding memory mapped IO as compared to IO mapped IO?

(1) ALU operation cannot be performed on IO data directly

(2) IO devices do not have their own address space

(3) Some memory wastage

(4) More number of IO devices connected

A Only 2 & 3

B Only 2 & 4

C Only 2, 3 & 4

D All 1, 2, 3 & 4

[NAT]

Ans = 12.5 %

#Q. Consider a device operating on 8MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 250 nanoseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is _____ % (rounded upto 1 decimal place)?

% of time CPU is blocked due to DMA = $\frac{\text{transfer to mem. time}}{\text{Preparatn time}} * 100\%$

$= \frac{250 \text{ nsec}}{2000 \text{ nsec}} * 100\%$

$= 12.5\%$

for 8 MB, preparation time = 1 sec

16 B, —— 11 —— = $\frac{1 \text{ sec}}{8 \text{ MB}} * 16 \text{ B}$

= 2 μsec

= 2000 nsec

[NAT]

Ans = 40

#Q. Consider a device operating on cycle stealing mode of DMA and transfer the data to memory in 20nanoseconds when 8 bytes data is ready or prepared. If the DMA blocks 0.1 fraction of CPU time for this transfer, then the transfer rate of the device is _____ megabytes per second?

$$\text{fraction of time CPU is blocked due to DMA} = \frac{20\,\text{nsec}}{\text{preparat}^n\text{ time}}$$

$$0.1 = \frac{20\,\text{ns}}{\text{preparat}^n\text{ time}}$$

$$\text{preparat}^n\text{ time} = \frac{20\,\text{ns}}{0.1} = 200\,\text{ns}$$

if 200 ns, device can prepare data = 8 B

1 sec —— 11 —— = $\frac{8\ B}{200 * 10^{-9} sec}$

$= \frac{8 * 10^9}{200}\ B/sec$

$= \frac{8\,000}{200} * 10^6\ B/sec$

$= 40\ MB/sec$

THANK - YOU