

# CS & IT ENGINEERING

## Computer Organization Architecture Memory Organization

DPP- 01 Discussion Notes



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#Q. The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

A

500 Bytes / Sec

B

2000 Bytes / Sec

C

✓ 2 Mbytes / Sec

D

2 GBytes / Sec

in 500 nsec, Data transferred = 1 B

$$1 \text{ ns}, \frac{\text{---}}{\text{---}} \text{ " } = \frac{1 \text{ B}}{500 \text{ ns}}$$

$$1 \text{ sec}, \frac{\text{---}}{\text{---}} \text{ " } = \frac{1 \text{ B}}{500 * 10^{-9} \text{ sec}}$$

$$= \frac{10^9 \text{ B}}{500 \text{ sec}}$$

$$= \frac{1000}{500} * 10^6 \text{ B/sec}$$

$$= 2 \text{ MB/sec}$$

#Q. The address bus width of a memory of size 4096 × 8 bits is \_\_\_ bits?

$$\text{no. of cells} = 4096 = 2^{12}$$

$$\text{add. size} = \left( \log_2 2^{12} \right) \text{ bits}$$

$$= \underline{\underline{12 \text{ bits}}} \quad \text{Ans.}$$

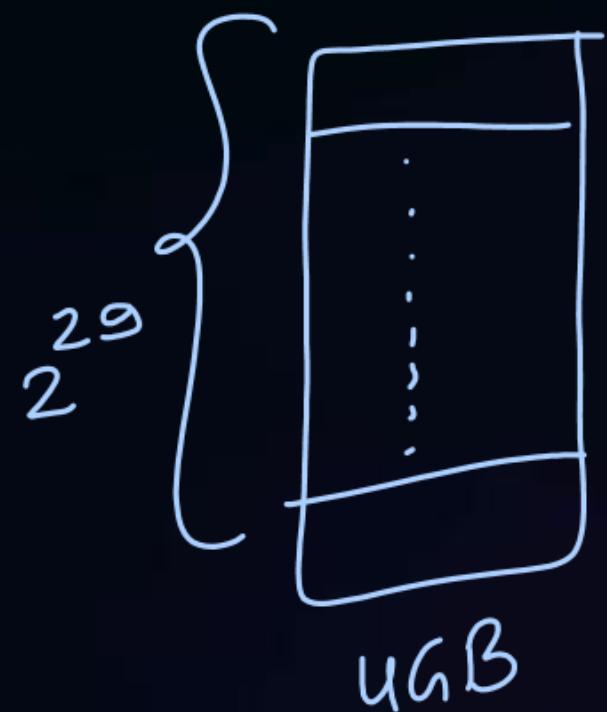
#Q. Consider a byte addressable memory which has 0.2 GBPS writing rate. The memory access time is \_\_ nanoseconds?

0.2 GB, access time = 1 sec

$$\begin{aligned} 1 \text{ B, } \underline{\underline{\text{---}}} &= \frac{1 \text{ sec} * 1 \text{ B}}{0.2 \text{ GB}} \\ &= 5 \text{ nsec} \quad \text{Ans} \end{aligned}$$

Ans = 8B

#Q. Consider a word addressable memory of total capacity of 4GB. The memory is accessed using a minimum of 29 bits address bus. The word size per address in this memory is \_\_\_ bytes?



$$\text{no. of cells} = 2^{29}$$

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$$\text{no. of cells} = \frac{4GB}{\text{1 word size}}$$

$$\text{1 word size} = \frac{4GB}{2^{29}} = \frac{2 \cdot 2^{30} B}{2^{29}}$$

$$= 2^3 B = 8B$$

#Q. Consider a memory with maximum size of X bytes. Memory is word addressable with word size of W bytes. The size of the address bus of the processor is at least \_\_\_\_ bits?

A

$$\log_2(X/W)$$

B

$$2^{(X/W)}$$

C

$$X/W$$

D

$$\log_2(X)$$

$$\begin{aligned}\text{no. of cells in mem.} &= \frac{\text{Mem. Size}}{\text{word size}} \\ &= \frac{x \text{ bytes}}{w \text{ bytes}} \\ &= \frac{x}{w}\end{aligned}$$

$$\text{add. size} = \log_2 \left( \frac{x}{w} \right) \text{ bits} = \left( \log_2 x - \log_2 w \right) \text{ bits}$$

#Q. A DRAM chip of  $64M \times 16$  bits has 128K rows of cells with  $y$  cells in each row. If DRAM takes  $x$ -ns for 1 refresh then total refresh time of the DRAM is microseconds, if  $x = 2 \times \log_2 y$ ?

- A 1200
- B 2304
- C 3202
- D 5444

no. of cells

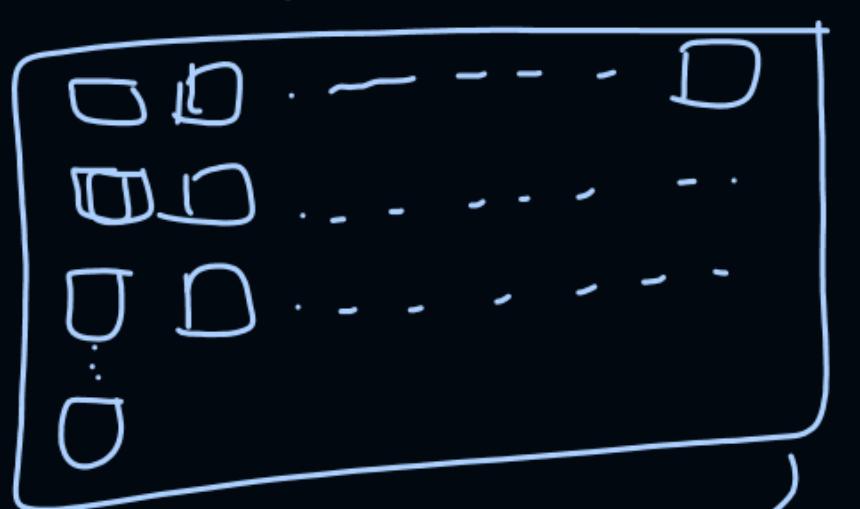
$$\text{no. of rows of cells} \downarrow * 18 \text{ nsec}$$

$$= 128 \underline{k} * 18 \text{ nsec}$$

$$= 128 * 18 \text{ usec}$$

$$= 2304 \text{ usec}$$

DRAM



$$y = 2^9 = 512$$

$$\text{no. of cells} = 128k * y$$

$$64M = 128k * y$$

$$y = \frac{64M}{128k} = \frac{2^6 * 2^{20}}{2^7 * 2^{10}} = \frac{2^{26}}{2^{17}} = 2^9$$

$$\begin{aligned}x &= 2 * \log_2 y \\&= 2 * \log_2 2^9 \\&= 18\end{aligned}$$

$$\text{Ans} = 324$$

4B

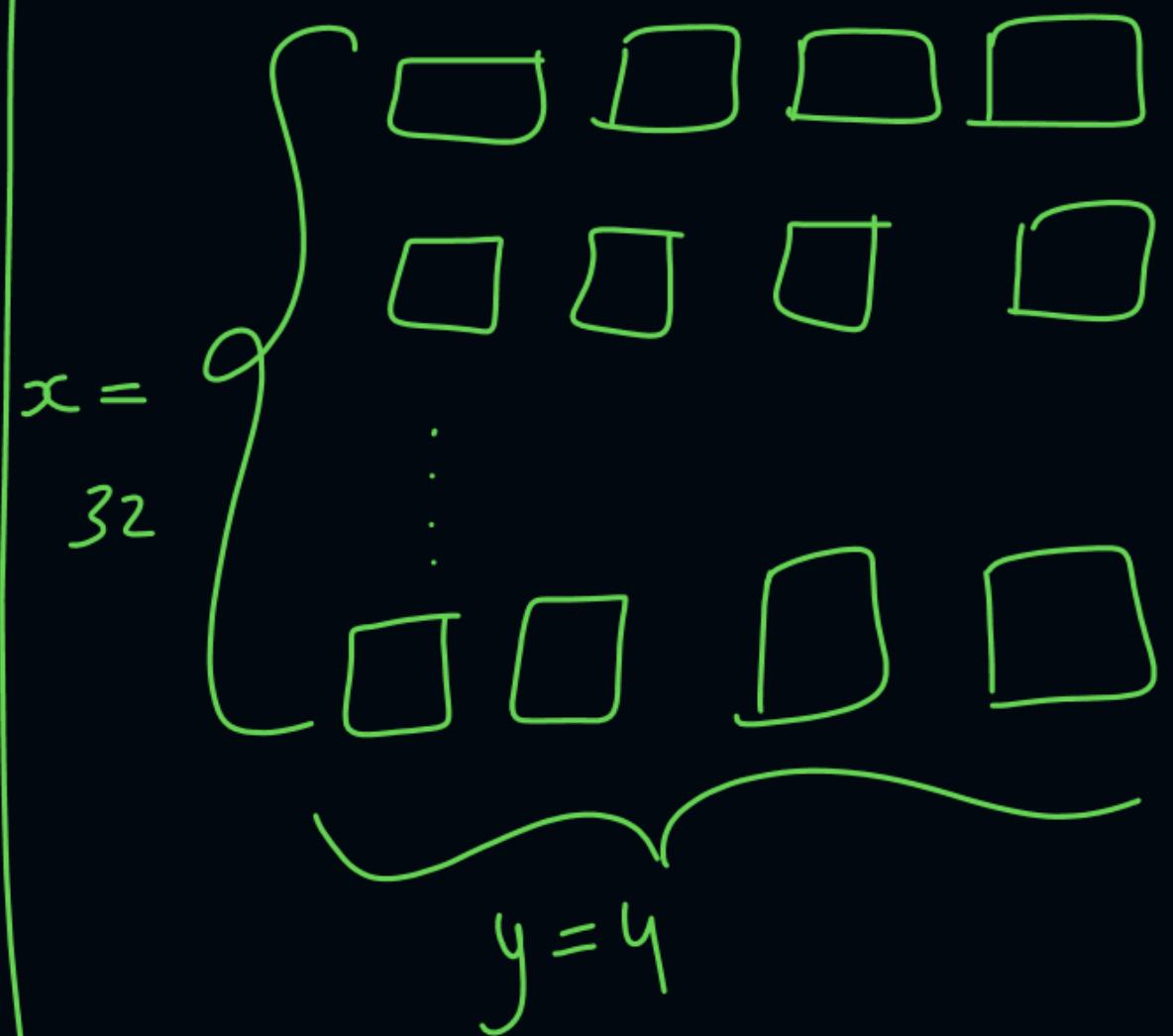
#Q. A 32-bits wide main memory unit with a capacity of 16GB is built using 128M $\times$ 8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of  $10x + y$  is?

$$\text{no. of addresses in expected mem.} = \frac{16\text{GB}}{4\text{B}} = 4G = 2^{32}$$

$$\text{expected mem} = 4G \times 4B = 4G \times 32 \text{ bits}$$

$$\begin{aligned}
 \text{no. of chips} &= \frac{4G \times 32 \text{ bits}}{128M \times 8 \text{ bits}} \\
 &= \frac{2^5 \cancel{32} \times \cancel{32}^4 \text{ bits}}{\cancel{2^7} \times \cancel{8} \text{ bits}} \\
 &= 32 * 4 \\
 &= 128 \text{ chips}
 \end{aligned}$$

arrangement of chips



$$\begin{aligned}
 10x + y &= 10 * 32 + 4 \\
 &= \underline{\underline{324}}
 \end{aligned}$$



THANK - YOU