



# CS & IT ENGINEERING

## Computer Organization Architecture CPU & Control Unit

DPP- 01 Discussion Notes

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#Q. Consider a CPU with clock rate of 200MHz. If the CPU has average CPI of 5 then average instruction execution time is \_\_\_\_nanoseconds?

$$\text{cycle time} = \frac{1}{200\text{MHz}} = \frac{1}{200} \mu\text{sec} = \frac{1000}{200} \text{ ns} = 5 \text{ ns}$$

$$= \text{CPI} * \text{cycle time}$$

$$= 5 * 5 \text{ nsec}$$

$$= 25 \text{ nsec}$$

#Q. A CPU runs on 500MHz clock rate and is executing a program which consists 1000 instructions. If the measured average CPI (Cycles per instructions) for the program is 6 then total time required to run the program on CPU is \_\_\_\_\_ microseconds?

$$\text{Time} = 1000 * 6 * \frac{1}{500 \text{ MHz}}$$

$$= 12 \text{ usec}$$

#Q. A CPU runs on x MHz clock rate and is executing a program which consists 200 instructions. If the measured average CPI (Cycles per instructions) for the program is 4 and total time required to run the program on CPU is 4 microseconds, then the value of x is \_\_\_\_\_?

$$\cancel{4 \mu\text{sec}} = 200 * 4 * \frac{1}{\text{clock rate}}$$

$$\text{Ans} = 200$$

$$\text{clock rate} = \frac{200}{\mu\text{sec}} = 200 \text{ MHz}$$

#Q. A CPU is used for executing  $n$  instructions. For executing these  $n$  instruction CPU has taken 6 cycles per instruction on average. The CPU operates on 2GHz clock rate. The CPU takes total of 0.75 microseconds to execute these  $n$  instructions. Later the same CPU used for executing  $2n$  number of instructions and for executing  $2n$  instructions its CPI (Cycles per Instruction) has been reduced to 5. Total time required by CPU to execute  $2n$  instructions is \_\_\_\_\_ microseconds (correct up to 2 decimal places)?

$$CPI = 6$$

$$\text{clock rate} = 2 \text{GHz}$$

$$0.75 \text{ usec}$$

$$\begin{aligned} & \left| \begin{array}{l} 2n \\ CPI = 5 \\ = 2 \text{GHz} \\ = ? \end{array} \right. \end{aligned}$$

$$0.75 \text{ usec} = n * 6 * \frac{1}{2 \text{GHz}}$$

$$0.75 \text{ usec} = n * 3 \text{ nsec}$$

$$750 \text{ nsec} = n * 3 \text{ nsec}$$

$$n = 250$$

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$$2n = 2 * 250 = 500$$

$$\text{Time} = 500 * 5 * \frac{1}{2 \text{GHz}}$$

$$= 1250 \text{ nsec}$$

$$= \underline{\underline{1.25}} \text{ usec}$$

$$\text{Time} = n * \text{CPI} * \frac{1}{\text{clock rate}}$$

$$\text{clock rate} = \frac{n * \text{CPI}}{\text{time}}$$

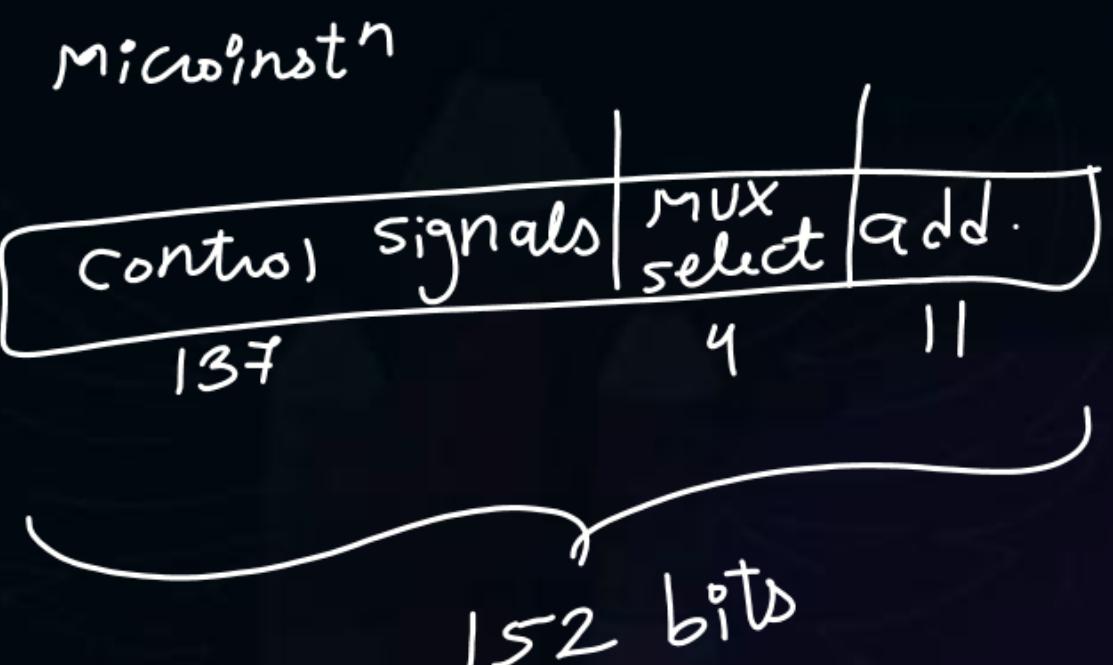
$$\frac{\cancel{n} * 6}{0.75 \text{ usec}} = \frac{2\cancel{n} * 5}{\text{time}}$$

$$\text{time} = \frac{10 * 0.75}{6}$$

$$= \underline{\underline{1.25}} \text{ usec}$$

#Q. Consider a microprogrammed control unit which has to support 64 number of instructions. For each instruction execution, control unit generates a sequence of 32 control words. Each microinstruction contains 3 fields: 137 control signals to support horizontal control unit, a MUX select field to select one of 16 inputs, and a next address field. The size of control memory needed is \_\_\_\_ K bytes?

$$\begin{aligned} \text{no. of microinstns} &= 64 * 32 \\ &= 2^{11} \implies \text{add.} = 11 - \text{bits} \\ &= 2048 \end{aligned}$$



$$\begin{aligned}\text{Control memory size} &= 2^{11} * 152 \text{ bits} \\ &= 2 * 152 \text{ k bits} \\ &= 304 \text{ k bits} \\ &= 38 \text{ k bytes}\end{aligned}$$

#Q. Design of a vertical microprogrammed control unit requires to generate 40 signals. Out of the first 34 those only 3 signals can be active at a time. And for remaining 6, anyone can be active anytime. The microinstruction of the control unit stores control signal information along with 3-bit mux select and 10-bits address field. The size of control memory required is \_\_\_\_ Kbits?



control memory size  
 $= 2^{10} * 37 \text{ bits}$   
 $= 37 \text{ k bits}$  Ans.

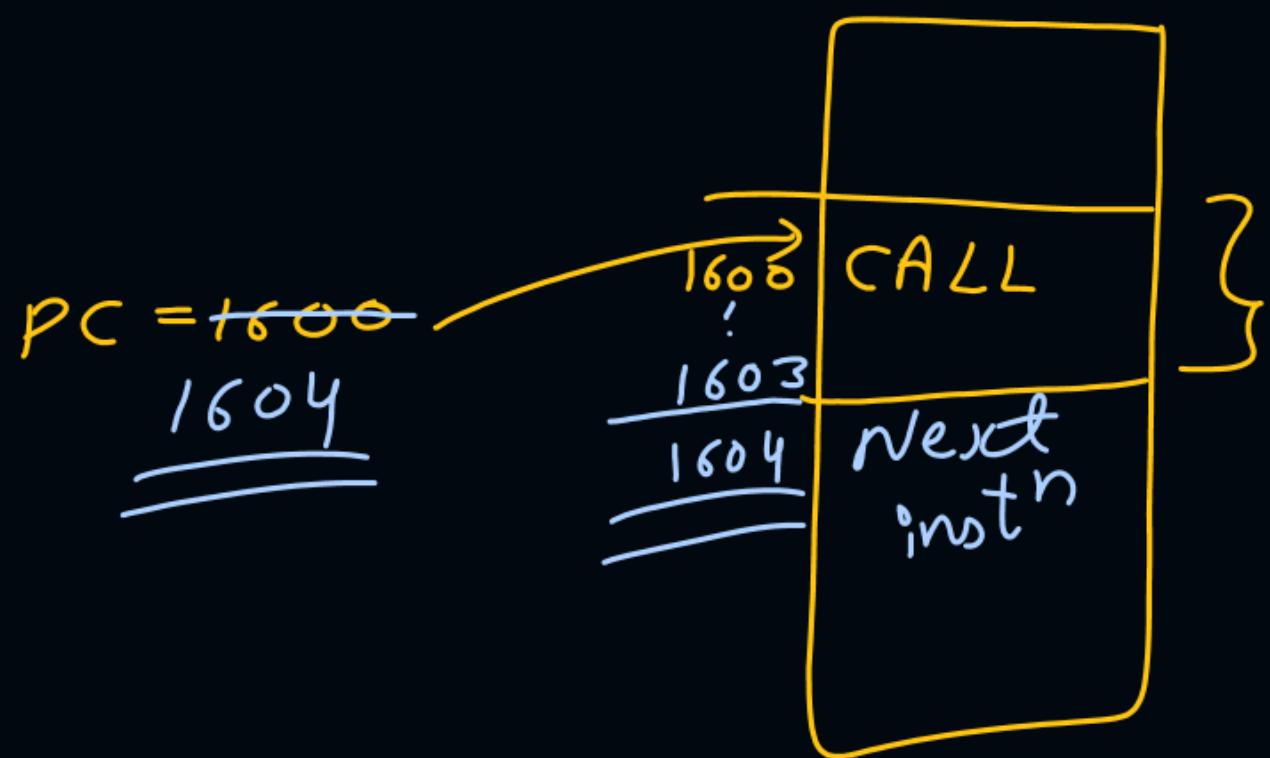
Ans = 1604

#Q. Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of four bytes. A stack in the main memory is implemented from memory location 500 and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is 660. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is 1600. Immediately after the fetch of CALL instruction value of PC will be \_\_\_\_?

Call instrn size = 2 words =  $2 * 2 = 4$  bytes





THANK - YOU