CS & IT ENGINEERING

Computer Organization Architecture

Cache Organization

PW

GATI WALLA

DPP 02 Discussion Notes

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$$2^5 B$$

#Q. Consider a $\overset{\frown}{512KB}$ direct mapped cache with block size of $\overset{\frown}{32}$ bytes. The main memory address is of 34-bits. The size of index and tag in bits are?
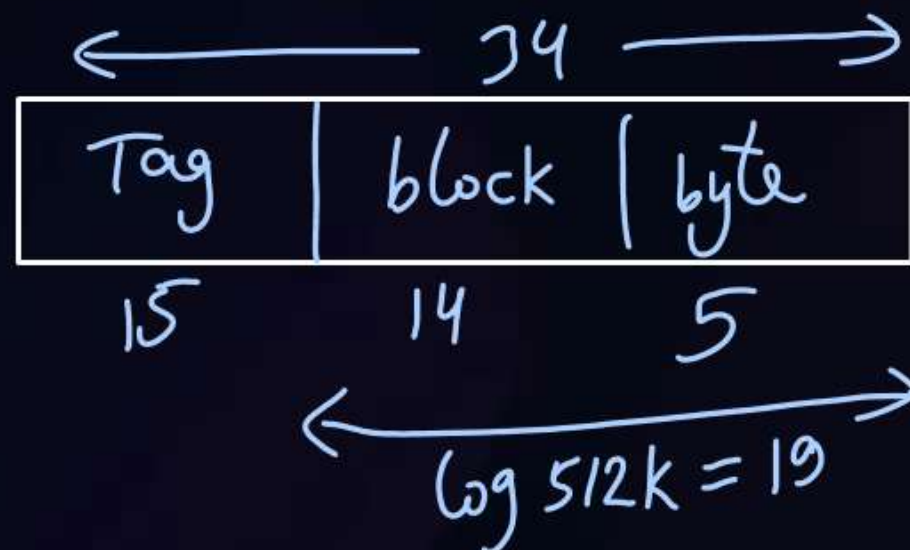
A 15, 14

B 14, 15

C 19, 14

D 14, 19

$$\xleftarrow{\hspace{2cm}} 34 \xrightarrow{\hspace{2cm}}$$

Tag	block	byte
15	14	5

$$\xleftarrow{\hspace{1cm} \log 512k = 19 \hspace{1cm}}$$
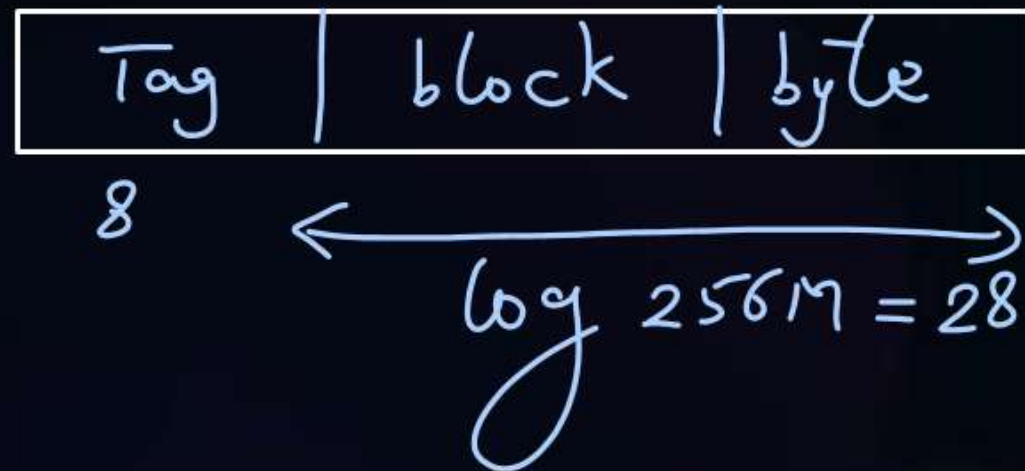
$$\text{no. of blocks in cache} = \frac{512kB}{32B} = \frac{2^{19}}{2^5} = 2^{14}$$

$$Ans = 64$$

#Q. Consider a direct mapped cache of size 256MB. Cache controller maintains 8-bits tag for each block in cache. The maximum size of main memory (byte addressable) supported in the system is _____GB?

Tag	block	byte

8    $\longleftarrow \log 256M = 28 \longrightarrow$

mm add. $= 36$ bits

mm size $= 2^{36}$ bytes

$= 64 \, GB$

$$Ans = 256$$

#Q. The size of memory required at cache controller to store metadata is 2KBytes. The metadata includes tag bits, 1 modified bit and 1 valid bit. The cache contains 1K blocks of 16 bytes each and organized as direct mapped. The size of main memory is___ Mbytes?

mm add.

Tag	Block	byte
14	10	4

mm add. = 28 bits

mm size = 2^{28} bytes

= 256 MB

Tag directory size = no. of blocks * (Tag+2) bits

$2K * 8\ bits = 1K * (Tag + 2)$

Tag = 14 bits

$$\text{Ans} = 32$$

#Q. Consider a direct mapped cache of size 256KB. The CPU generates x- bit addresses. The number of tag bits in main memory address are 14 bits then value of x is _____?

mm add.

Tag	cm block	byte

14

$\longleftarrow \log 256k = 18 \text{ bits} \longrightarrow$
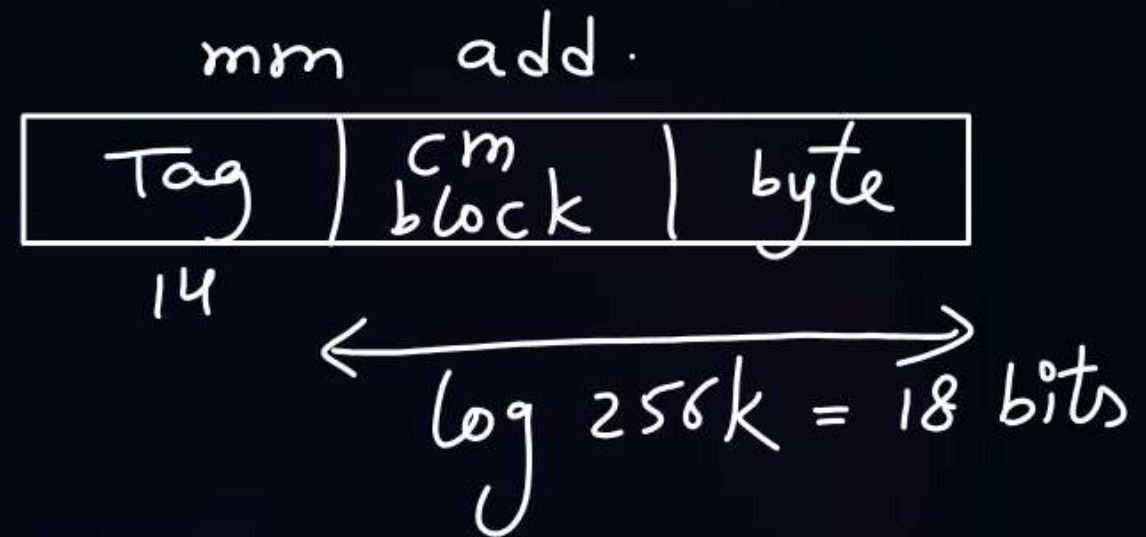
$$mm\ add. = 14 + 18$$
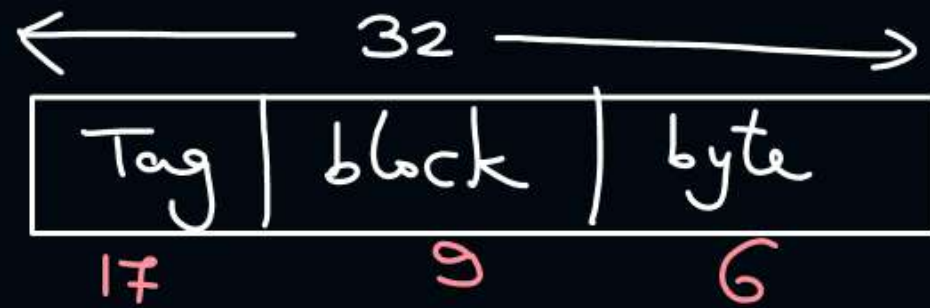$$= \underline{\underline{32}}\ \text{bits}$$

#Q.   Assume a computer has 32-bit addresses. Each block stores 64 bytes. A direct-mapped cache has 512 blocks. Match the block (line) of the cache (in decimal) we look for each of the given hexadecimal addresses in the table?

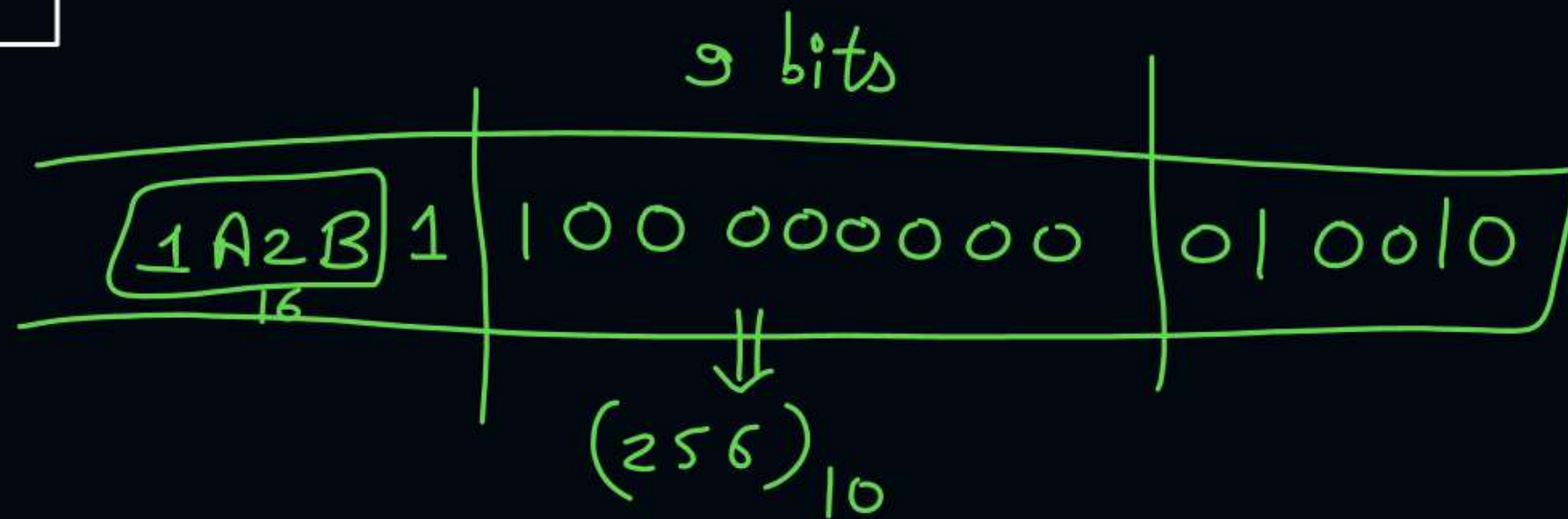**A**   1A2BC012: 256, FFFF00FF: 3, 12345678: 345, C109D532: 340

B   1A2BC012: 512, FFFF00FF: 7, 12345678: 243, C109D532: 320

C   1A2BC012: 128, FFFF00FF: 5, 12345678: 345, C109D532: 420

D   1A2BC012: 255, FFFF00FF: 1, 12345678: 247, C109D532: 240

$$\xleftarrow{\hspace{2cm}} 32 \xrightarrow{\hspace{2cm}}$$

Tag	block	byte
17	9	6

9 bits

1.) 1 A 2 B C 0 1 2

$\boxed{1A2B}\,1 \mid 1\,00\,000\,000 \mid 01\,0010$
   16

$\Downarrow$

$(256)_{10}$

2) $\boxed{FFFF}\,00FF$ $(0\,0000\,0011)_2 = (3)_{10}$

3) $(\boxed{1234}\,5678)_{16}$ $(101\,011\,001)_2 = (345)_{10}$

4) $(C109D532)_{16}$ $(10101010100)_2 = (340)_{10}$

Ans = 4

2^5

#Q.   Consider a cache with 2^{13} blocks of size (32) Bytes each. The CPU generates addresses of 32-bits. The cache controller stores 1 valid bit, 1 modified bit and tag-bits for each metadata entry. The cache controller has a maximum memory of (18Kbytes) to store the metadata. The cache is organized as k-way set associative. Maximum value of k to utilize the cache controller memory in optimized manner is ___?

Tag directory size $= 18KB = 2^{13} * (Tag + 2)$ bits

$18K * 8$ bits $= 2^{13} * (Tag + 2)$ bits

$Tag = 16$ bits

mm add.

$$\xleftarrow{\qquad\qquad 32 \qquad\qquad}$$

Tag	set	byte

16   11   5
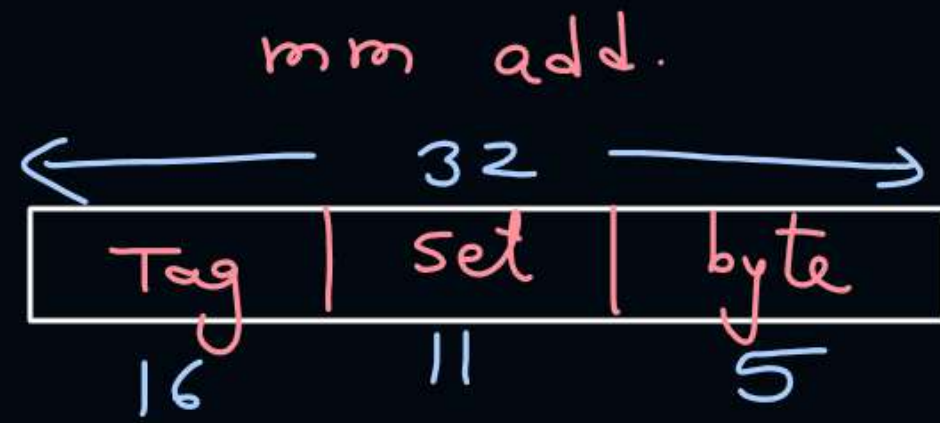
$$\text{no. of sets} = 2^{11} = \frac{\text{no. of blocks in cm}}{k}$$

$$2^{11} = \frac{2^{13}}{k}$$

$$k = \frac{2^{13}}{2^{11}} = 2^{2} = \underline{4}$$

$$Ans = 97.8\%$$

(P)(W)

#Q.   Consider a direct mapped write back data cache of size 2KB with the block size of 128 bytes. The cache is considered to be empty initially. The byte addressable main memory has size 1Mbytes. Further consider that there is an array A[35][20] with each element occupies 4 bytes. The base address of array is $(1A300)_{16}$. The array is accessed 3 times. And between the accesses, there is no any data cache changes happen. Hit ratio (correct upto 1 decimal place) of cache for this array access is ___%?

$$\text{no. of blocks in cache} = \frac{2kB}{128B} = \frac{2^{11}}{2^7} = 2^4 = 16$$

$$\text{Array size} = 35 * 20 = 700 \text{ elements}$$
$$= 700 * 4 = 2800 \text{ Bytes}$$

no. of blocks needed to store array $= \left\lceil \dfrac{2800\,B}{128\,B} \right\rceil = 22$ blocks

overlapping blocks $= 22 - 16 = 6$

	no. of miss
1st access	22
2nd access	$6*2 = 12$
3rd ,,	$6*2 = 12$
Total	46

Total no. of mem. reference $= 700 * 3$
$= 2100$

No. of hits $= 2100 - 46 = 2054$

Hit ratio $= \dfrac{2054}{2100} = 0.978 = 97.8\%$

THANK - YOU