CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction & Addressing Modes
DPP 01 Discussion Notes

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[NAT]

Ans = 2

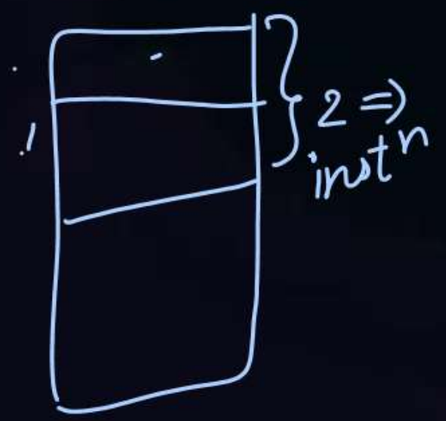
#Q. Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

4 → 32 bits

350 → opcode = 9 bits

opcode	a.1	a.2
9	19	19

47-bits



no. of cells = $\frac{2MB}{4B}$

$= \frac{2^1 \cdot 2^{20}}{2^2} = 2^{19}$ ⇒ add. = 19 bits

[NAT]

Ans = 4000

#Q. Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. If a program has 500 instructions, which is stored in the memory then the amount of memory required to store the entire program is ____ bytes?

for 1 inst^n $\Rightarrow$ 2 locations

500 —11— $\Rightarrow$ 2 * 500 = 1000 locations

= 1000 * 4B

= 4000 Bytes

[MCQ]

2^3 2^{18} ⇒ add. = 18 bits

#Q. The word addressable memory of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields; an operation code field, a mode field to specify one of 8 addressing modes, a register address field to specify one of the 64 processor registers and a memory address field.

↳ Reg. = 6 bits

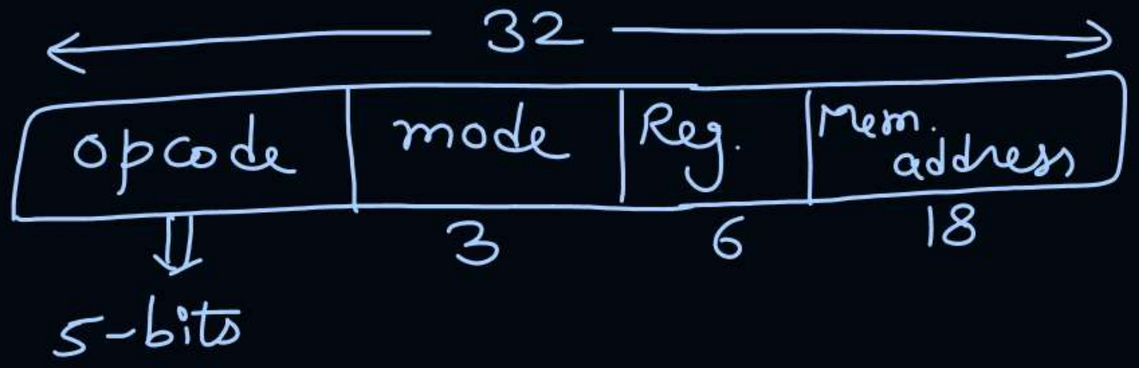
The bits for each field required in instruction format if the instruction is stored exactly in one word in memory?

A Opcode: 5, Addressing mode: 3, Register: 6, Memory address: 20

B Opcode: 3, Addressing mode: 3, Register: 6, Memory address: 20

C Opcode: 5, Addressing mode: 3, Register: 6, Memory address: 18

D Opcode: 3, Addressing mode: 3, Register: 6, Memory address: 18

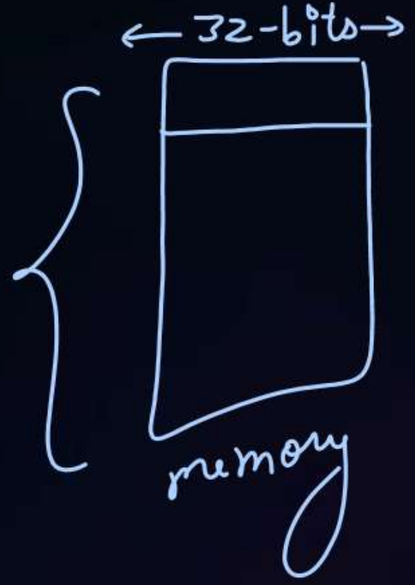

32
opcode
mode
Reg.
Mem. address
3
6
18
5-bits

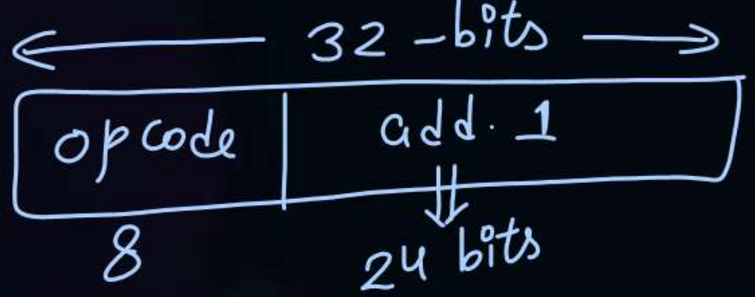
[NAT]

Ans = 64

→ opcode = 8 bits

#Q. A digital computer has a memory unit with 32-bits per word. The instruction set consists of 240 different operations. All the instructions have an operation code part (opcode) and an address part (allowed for only 1 address). Each instruction is stored in one word of memory. The maximum allowable size of memory (word addressable) is _____Mbytes?





no. of cells in mem. = 2^{24}

mem. size = $2^{24} * 32$ bits

$= 2^{24} * 4B$

$= 2^{24} * 2^2 B$

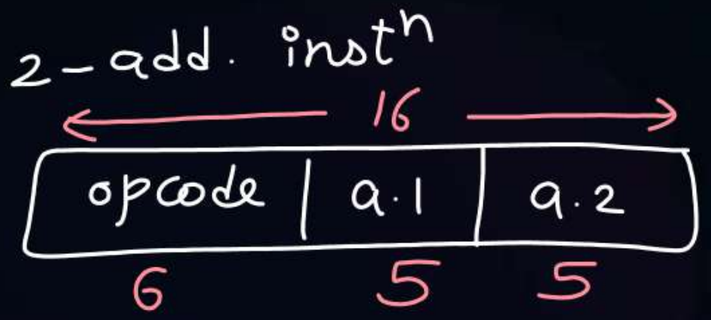
$= 2^{26} B$

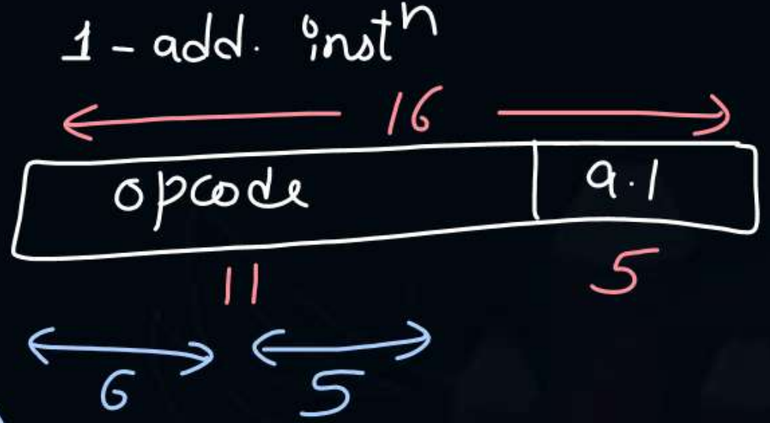
$= 64MB$

[NAT]

Ans = 1024

#Q. Consider a system which supports 2-address and 1-address instructions. The system uses 16 bits instructions and 5-bits addresses. If there are total 32 2-address instructions then maximum how many 1-address instructions can be formulated?





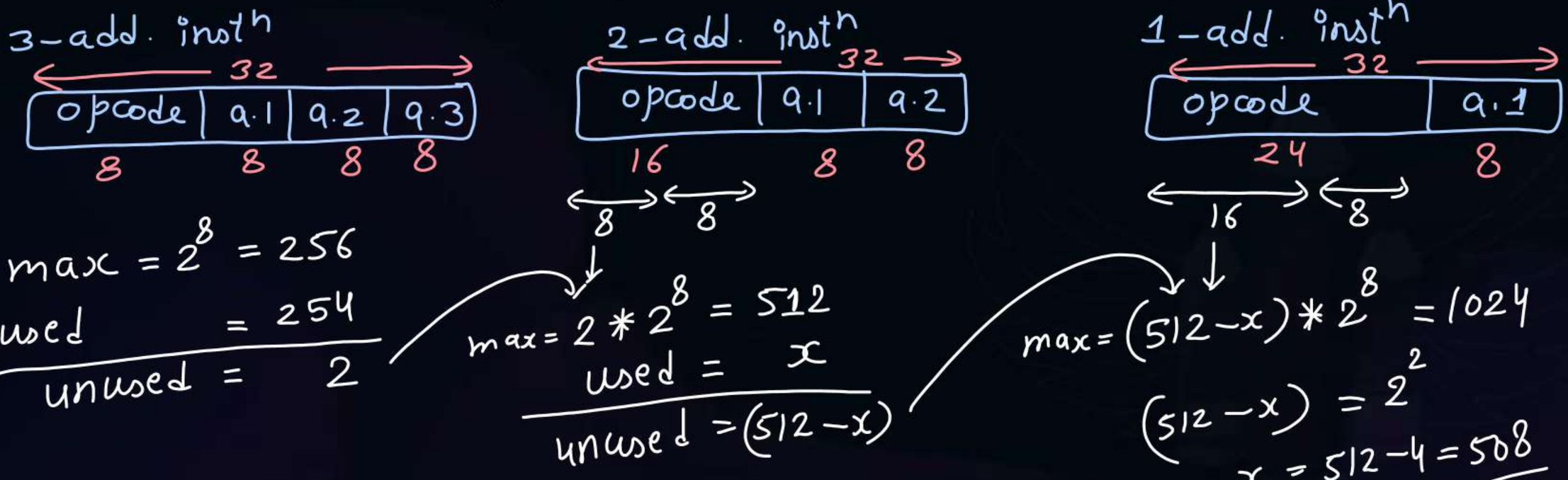
max = 2^6 = 64
used = 32
unused = 32

max = $32 * 2^5 = 2^{10} = 1024$

[NAT]

Ans = 508

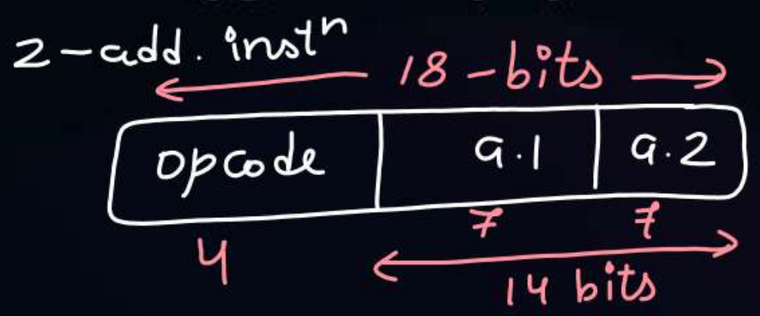
#Q. Consider a system which supports 3-address, 2-address and 1 -address instructions. It has 32-bit instructions with 8-bits addresses. If there are 254 3-address instructions and 1024 1-address instructions, then maximum how many 2-address instructions can be formulated?

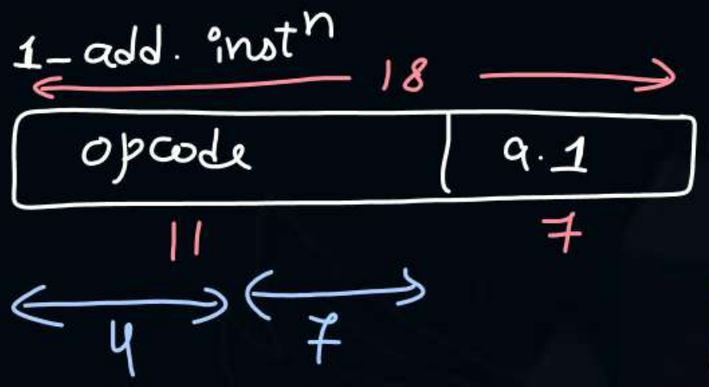


[NAT]

Ans = 128

#Q. Consider a system which supports 2-address and 1-address instructions. The system has 18 bits instructions. If there are 7 2-address instructions and 1152 1-address instructions, then the maximum size of memory supported by system is ____bytes?





max = 2^4 = 16
used = 7
unused = 9

max = $9 * 2^7$ = 1152

No. of cells = 2^7

Mem. size
$= 2^7 * 1B$
$= 128B$

[MCQ]

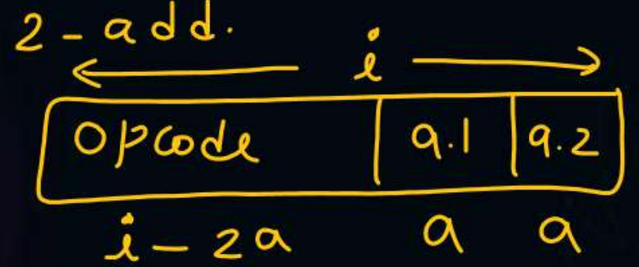
#Q. Consider a system which supports 2-address, 1-address and 0-address instructions. The system has 'i' bits instructions and 'a' bits addresses. If there are 'x' 2-address instructions and 'y' 1-address instructions then which of the following is correct for maximum number of 0-address instructions supported by system?

A $2^i - 2^a x - y$

B $2^i - 2^{2a} x - y$

C $2^i - 2^{2a} x - y2^a$

D $2^i - 2^a x - y2^a$

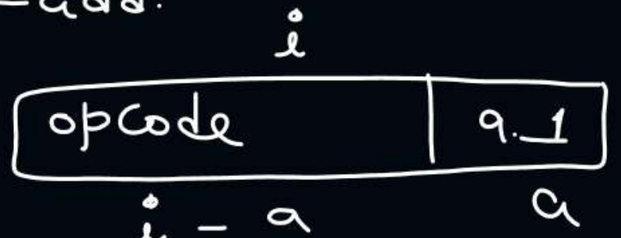


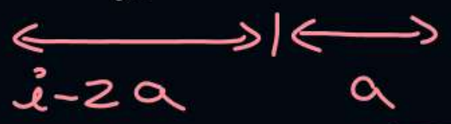
$$\text{max} = 2^{i-2a}$$

$$\text{used} = x$$

$$\text{unused} = 2^{i-2a} - x$$

1-add.





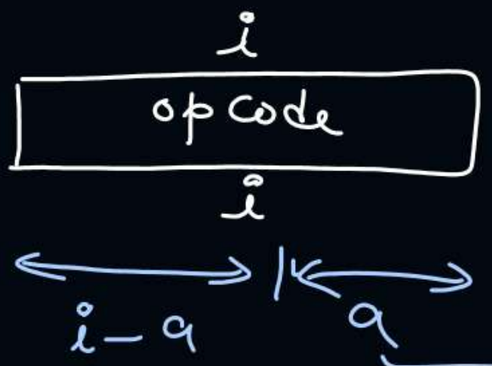
$$max = \left(2^{i-2a} - x\right) * 2^{a}$$

$$= 2^{i-a} - x2^{a}$$

$$used = y$$

$$unused = 2^{i-a} - x2^{a} - y$$

0- add.



$$max = \left(2^{i-a} - x2^{a} - y\right) * 2^{a}$$

$$= 2^{i} - x2^{2a} - y2^{a}$$

[NAT]

Ans = 19

#Q. Consider there are 4 types of instructions in system:

Type 1: One opcode and 2 registers

Type 2: One opcode and 1 register

Type 3: One opcode and 1 memory address

Type 4: One opcode, 1 register and 1 memory address

Number of registers in CPU=128 $= 2^7 \Rightarrow$ Reg. = 7 bits

Maximum instruction length: 32bits (Variable length instructions supported)

Total Instructions: Type-1: 15, Type-2: 20, Type-3: 12, Type-4: 14

Maximum memory address size = 19 bits

Total instns

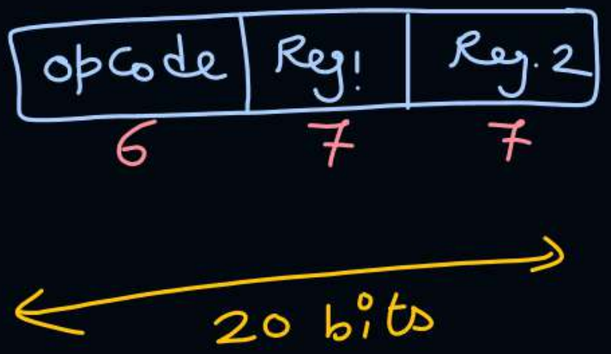
= 15 + 20 + 12 + 14

= 61

⇓

opcode = 6-bits

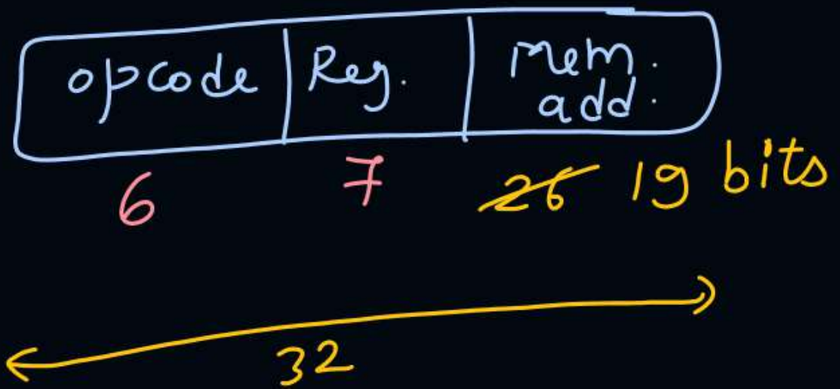
Type 1



Type 2

Type 3

Type 4



[NAT]

Ans = 3

#Q. Consider a register-based architecture system which can support maximum 2-address instructions. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

```
t1 = X + Y
t2 = Z * 2
t3 = t2 + A
t4 = t3 – t1
t5 = t4 + t3
```

```
R1 ← X
R2 ← Y
R1 ← R1 + R2
R2 ← Z
R2 ← R2 * 2
R3 ← A
R2 ← R2 + R3
R3 ← R2
R2 ← R2 – R1
R2 ← R2 + R3
```

Note: X, Y, A and Z are memory operands; and consider first operand as destination operand and there is no any optimization done by compiler.

THANK - YOU