EE 5313 Microprocessor Systems Project

SDRAM Controller for MT48LC16M4A2 memory device interfaced with the 80386DX processor.

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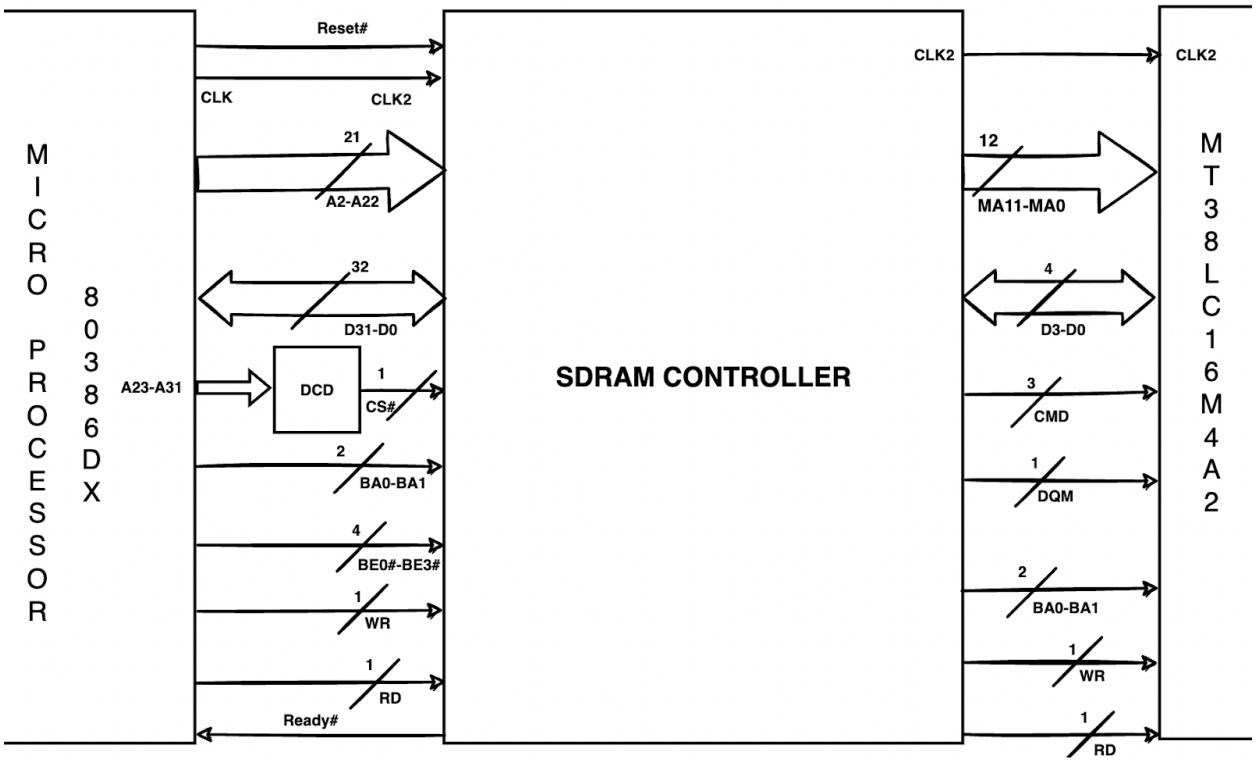
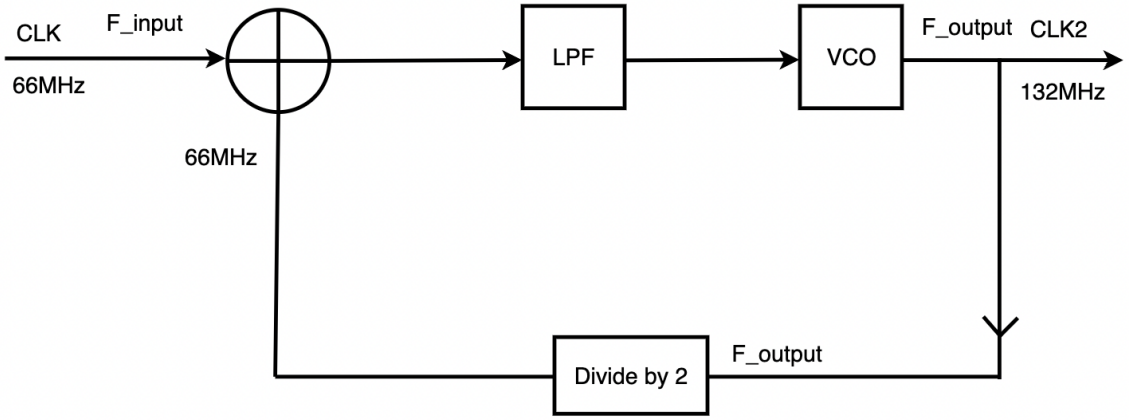
SDRAM Controller

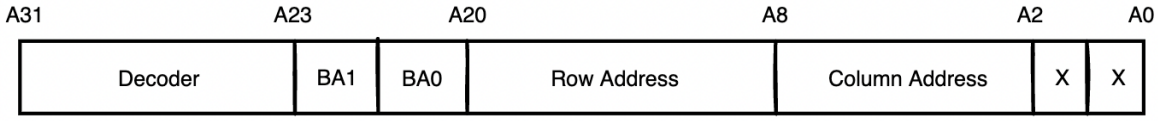


- The Write and Read signal shown here are the combination of M/IO and ADS#, and the generation of these signal are shown in the signal generation section.
- The CS# is coming from the decoder, and the 9 upper bits of the microprocessor goes into the decode, the output of the decode is single, which is CS active low.
- The CLK2 runs as twice the speed of CLK.
- MA11-MA0 are the address lines going into the SDRAM, they will be used for different implementations depending on the CMD.
- CMD is a 3 bit output comprised of RAS#, CAS# and WE#.

Phase Locked Loop



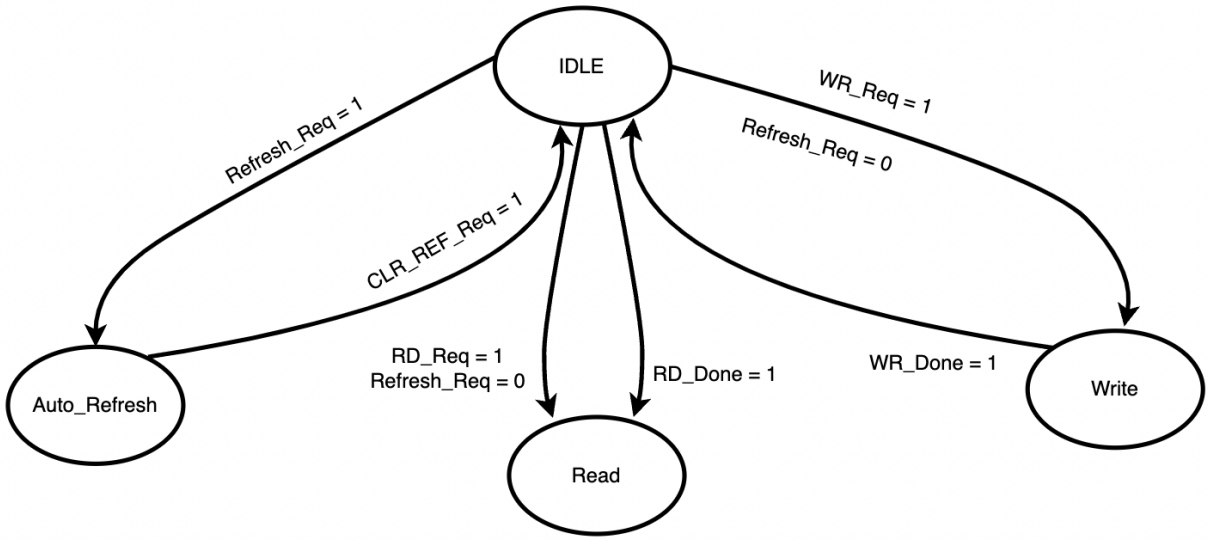
32 bit address lines from µP breakdown



Characteristics

- **MT38LC16M4A2 - 4 Meg x 4 x 4 banks**
- **Speed -7E**
- **Frequency of the controller is $\leq$ 133MHz | 132 MHz with PLL used above**
- **Clock Cycle = 7.5ns**
- **CL = 2 Cycles**
- **Burst Length = 8**
- **Refresh Time is 64ms (Commercial)**
- **Auto Precharge is enabled.**

TOP LEVEL STATE DIAGRAM



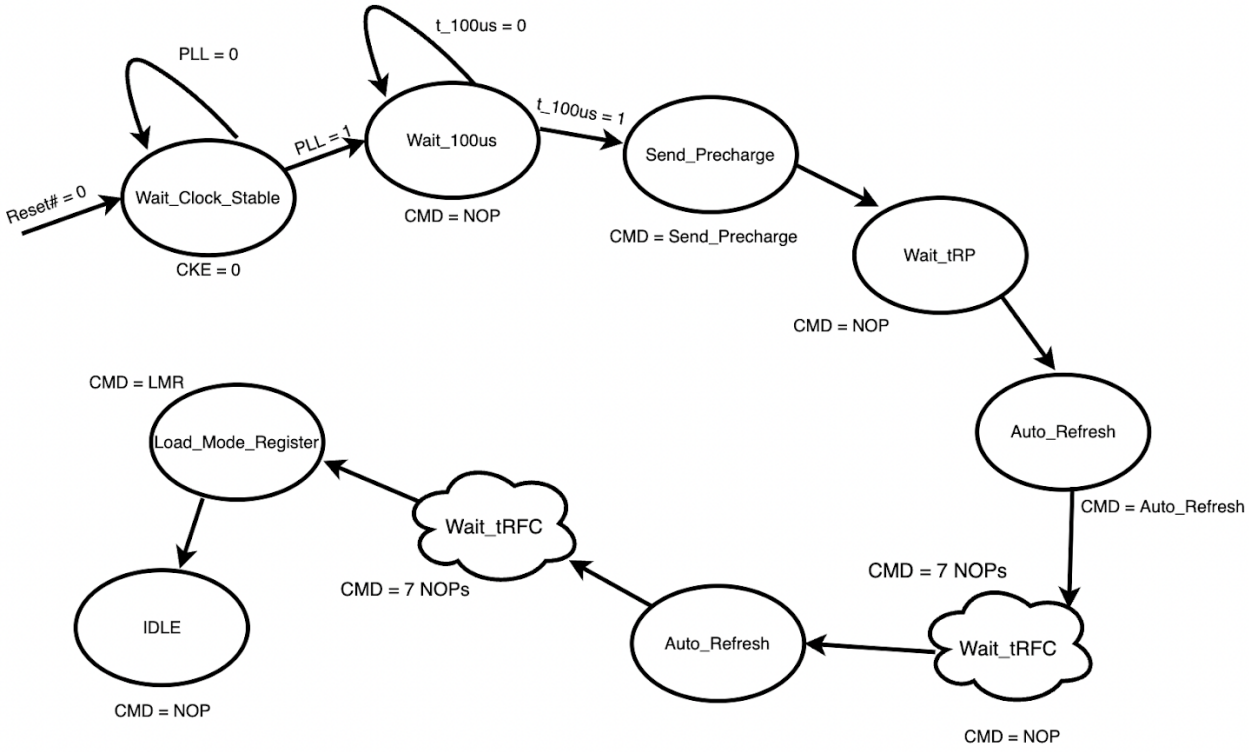
State Transition Table

IDLE	Refresh_Req = 1	Auto_Refresh
IDLE	RD_Req =1 && Refresh_Req = 0	Read
IDLE	WR_Req = 1 && Refresh_Req = 0	Write
Auto_Refresh	CLR_REF_Req = 1	IDLE
Read	RD_Done = 1	IDLE
Write	WR_Done = 1	IDLE

- This is a top level state diagram. The RD_Done = 1 is defined as if we are in the Dout_8 state and no more read or write request is asserted.
- The WR_Done = 1 is defined as if we are in the Din_8 state and no more read or write request is asserted.
- The Dout_8 and Din_8 states are shown in the read and write section.

INITIALIZATION

1. State Diagram



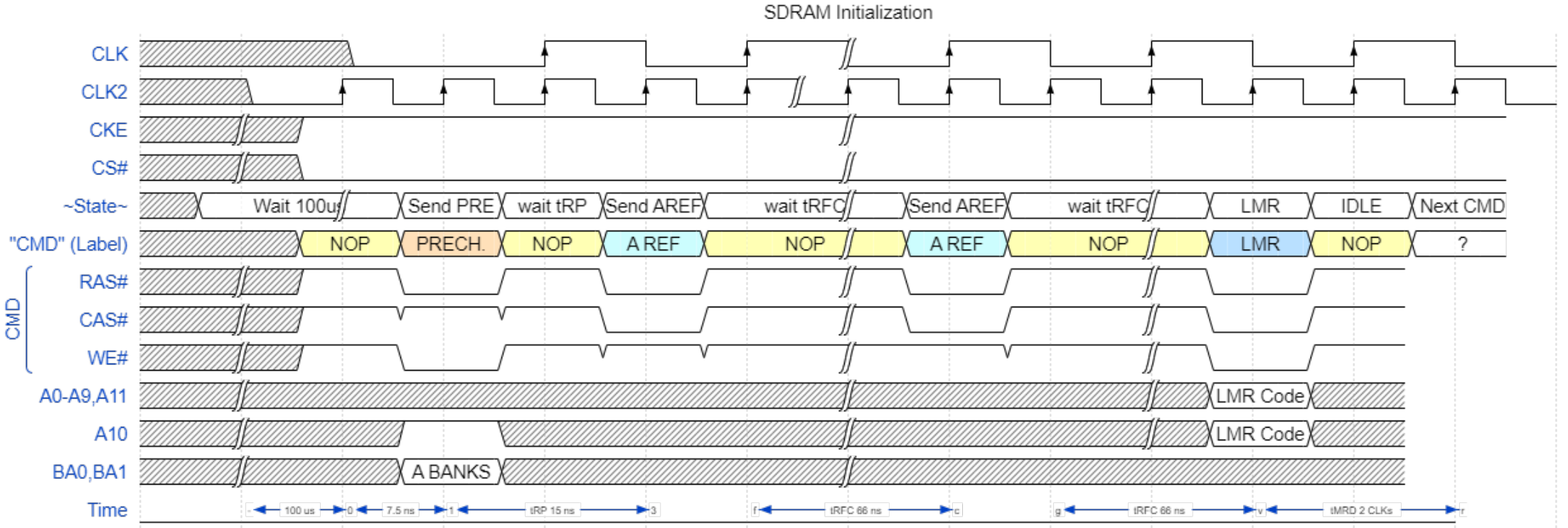
- The Wait_tRFC is 66ns, and this bubble contains 7 wait states from Wait_tRFC1 to Wait_tRFC7. The toal wait time is 9 CLKs, but the two CLK cycles of 7.5 ns are included in the transition from Auto_Refresh to Wait_tRFC and Wait_tRFC to Auto-Refresh.
- In Lode_Mode_Register command, we load the code, failing to do that would result in SDRAM being initialized with default values, which maybe undesired.
- The LMR is explained in the last part of this section.

2. **State Transition Table**

State	**Condition**	**Next State**
X	Reset# = 0	Wait_Clock_Stable
Wait_Clock_Stable	PLL = 0	Wait_Clock_Stable
Wait_Clock_Stable	PLL = 1	Wait_100us
Wait_100us	t_100us = 0	Wait_100us
Wait_100us	t_100us = 1	Send_Precharge
Send_Precharge	X	Wait_tRP
Wait_tRP	X	Auto_Refresh
Auto_Refresh	X	Wait_tRFC1
Wait_tRFC1	…X…	Wait_tRFC7
Wait_tRFC7	X	Auto_Refresh
Auto_Refresh	X	Wait_tRFC
Wait_tRFC1	…X…	Wait_tRFC7
Wait_tRFC7	X	Load_Mode_Register
Load_Mode_Register	X	IDLE

3. Command Table

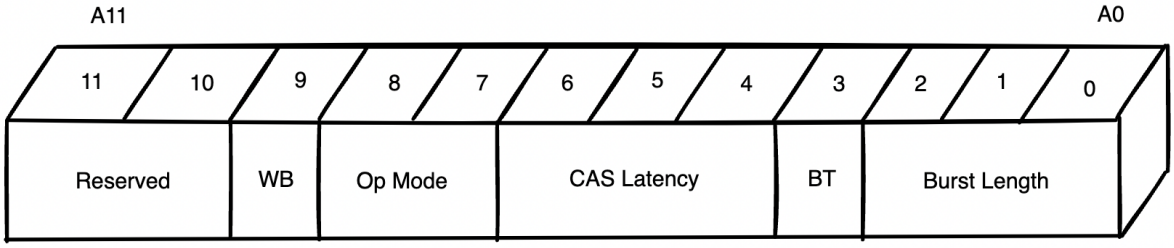
Signal	Enabled for (State(s))
CKE	Precharge, Auto_Refresh, LMR, IDLE
CS#	Precharge, Auto_Refresh, LMR, IDLE
RAS#	Precharge, Auto_Refresh, LMR
CAS#	Auto_Refresh, LMR
WE#	Precharge, LMR
A0-A9, A11	LMR
A10	Precharge
BA0, BA1	Precharge


SDRAM Initialization
CLK
CLK2
CKE
CS#
~State~
"CMD" (Label)
CMD
RAS#
CAS#
WE#
A0-A9,A11
A10
BA0,BA1
Time
Wait 100us
Send PRE
wait tRP
Send AREF
wait tRFC
Send AREF
wait tRFC
LMR
IDLE
Next CMD
NOP
PRECH.
NOP
A REF
NOP
A REF
NOP
LMR
NOP
?
LMR Code
LMR Code
A BANKS
100 us
7.5 ns
tRP 15 ns
tRFC 66 ns
tRFC 66 ns
tMRD 2 CLKs

5. Clock Cycles

Time	Value	No. of Clock Cycles
Waiting 100us before issuing any command	100us	13334
Precharge (tRP)	15ns	2
Auto_Refresh (tRFC) x2	66ns	9 x2 = 18
Load_Mode_Register (tMRD)	15ns	2

6. Load Mode Register

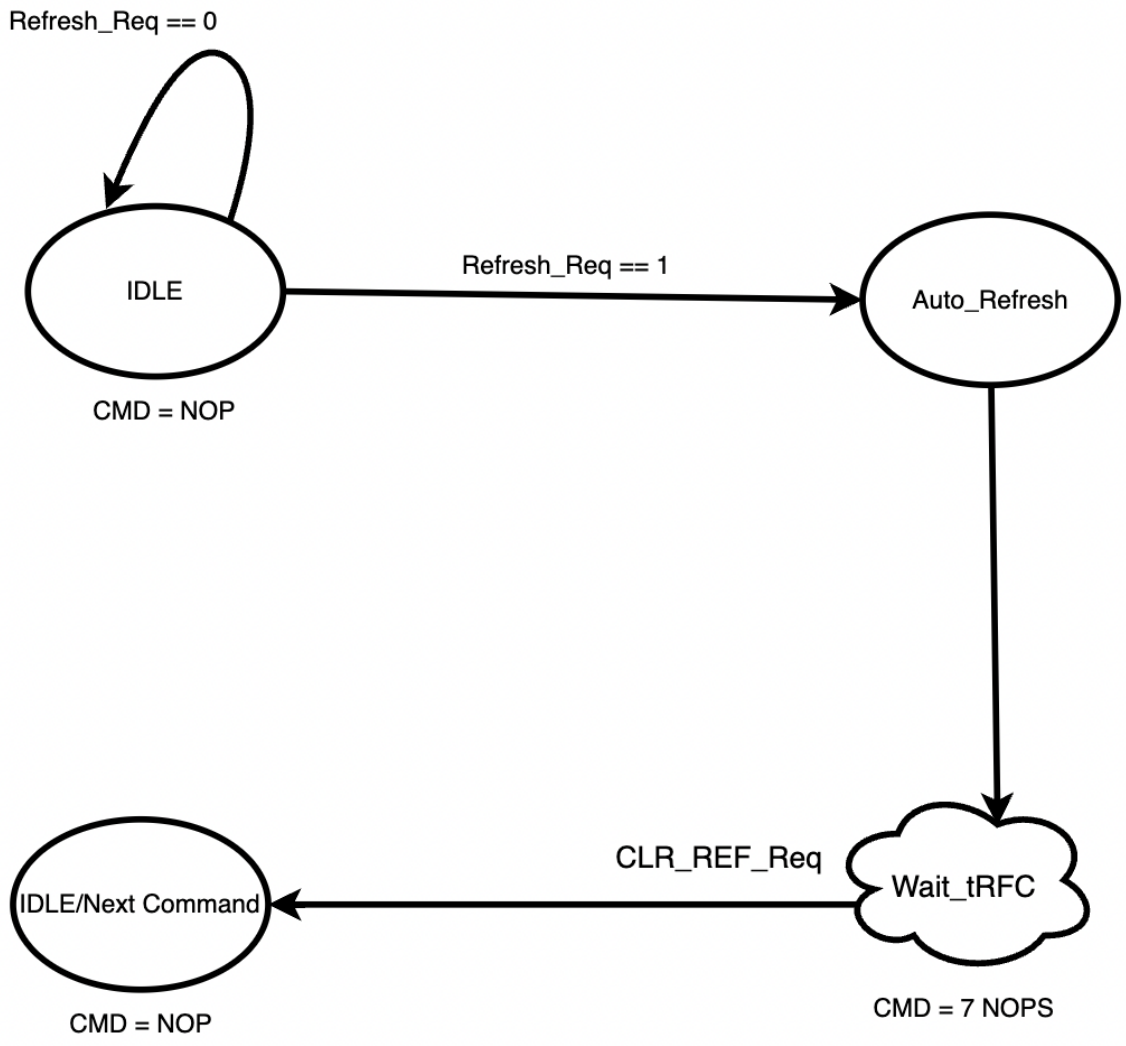


Address Bus	**A11**	**A10**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**

- Burst Length: The address lines A0, A1, A2 (1, 1, 0) are used to determine the burst length.
- Burst Type: The address line A3 (0) is determining the burst type.
- Cas Latency: Address lines A4, A5, A6 (0, 1, 0)determine the CAS latency.
- Op Mode: The Op mode is determined by the A7 and A8 (0,0)
- Write Burst Mode: Determined by A9 (0)
- A11 and A0 (0,0) are reserved and used for compatibility with future devices.

AUTO REFRESH

1. **State Diagram**



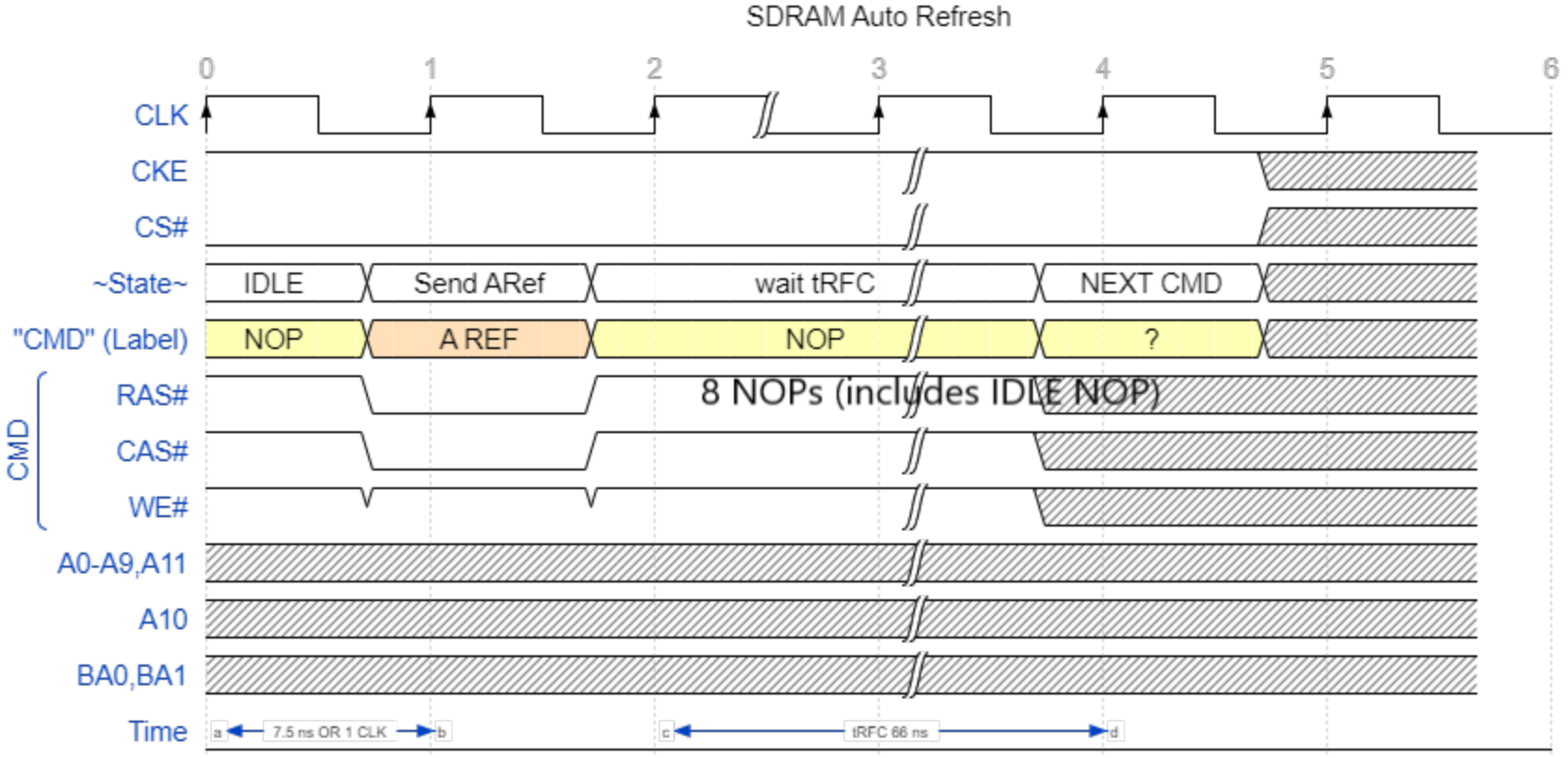
- The Wait_tRFC is 66ns, and this bubble contains 7 wait states from Wait_tRFC1 to Wait_tRFC7. The toal wait time is 9 CLKs, but the two CLK cycles of 7.5 ns are included in the transition from Auto_Refresh to Wait_tRFC and Wait_tRFC to IDLE/Next Command.

2. **State Transition Table**

State	**Condition**	**Next State**
IDLE	Refresh_Req == 0	IDLE
IDLE	Refresh_Req == 1	Auto_Refresh
Auto_Refresh	X	Wait_tRFC
Wait_tRFC1	…X…	Wait_tRFC7
Wait_tRFC7	X	NEXT CMD

3. Command Table

Signal	Enabled for State(s)
CKE	NOP, Auto_Refresh, Precharge
CS#	NOP, Auto_Refresh, Precharge
RAS#	Auto_Refresh, Precharge
CAS#	Auto_Refresh
WE#	Precharge
A10	Precharge

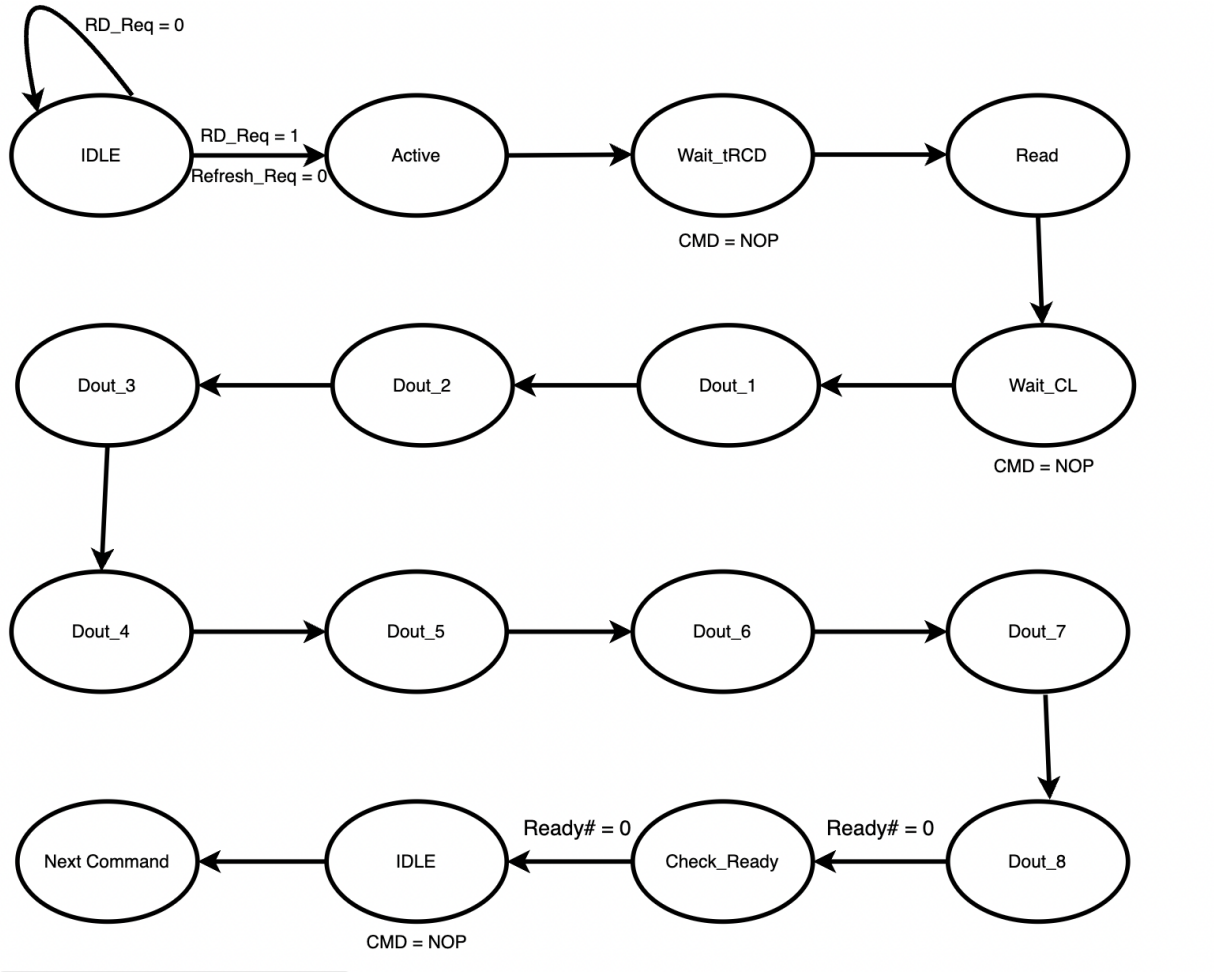

SDRAM Auto Refresh
0
1
2
3
4
5
6
CLK
CKE
CS#
~State~
IDLE
Send ARef
wait tRFC
NEXT CMD
"CMD" (Label)
NOP
A REF
NOP
?
CMD
RAS#
CAS#
WE#
8 NOPs (includes IDLE NOP)
A0-A9,A11
A10
BA0,BA1
Time
a
7.5 ns OR 1 CLK
b
c
tRFC 66 ns
d

5. Clock Cycles

Time	Value	No. of Clock Cycles
Precharge (tRP)	15ns	2
Auto_Refresh (tRFC)	66ns	9

READ

1. State Diagram



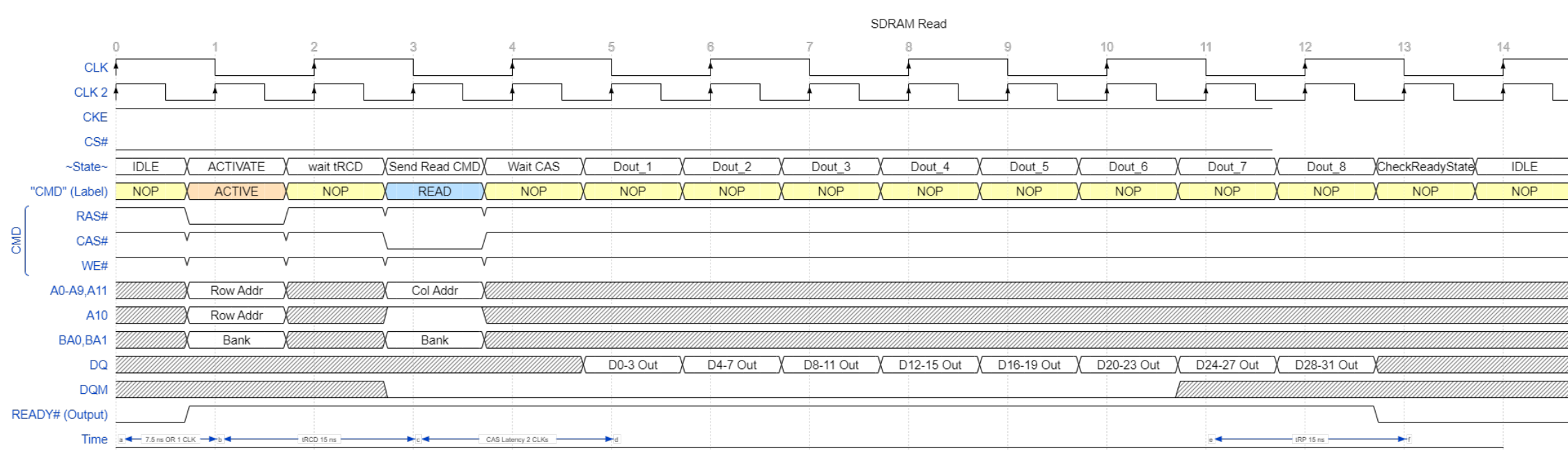
- Once done reading out data (Leaving Dout_8) Assert READY# Low for 2 CLKs (W.S. Check_Ready), leave to IDLE knowing µP has been alerted to READY status.

2. **State Transition Table**

State	Condition(s)	Next State
IDLE	RD_Req = 0	IDLE
IDLE	RD_Req = 1 & Refresh_Req = 0	Active
Active	X	Wait_tRCD
Wait_tRCD	X	Read
Read	X	Wait_CL
Wait_CL	X	Dout_1
Dout_1	X	Dout_2
Dout_2	X	Dout_3
Dout_4	X	Dout_4
Dout_4	X	Dout_5
Dout_5	X	Dout_6
Dout_6	X	Dout_7
Dout_7	X	Dout_8
Dout_8	X	Dout_8
Dout_8	X	Check_Ready
Check_Ready	X	IDLE

3. Command Table

Signal	Enabled for State(s)
CKE	NOP, Active, Precharge, Read, Dout_N, IDLE
CS#	NOP, Active, Precharge, Read, IDLE
RAS#	Active
CAS#	Read
WE#	WE# is high
A0-A9/A11	Active, Read
A10	Precharge, Read, Active
BA0,BA1	Precharge, Active
DQ	Read

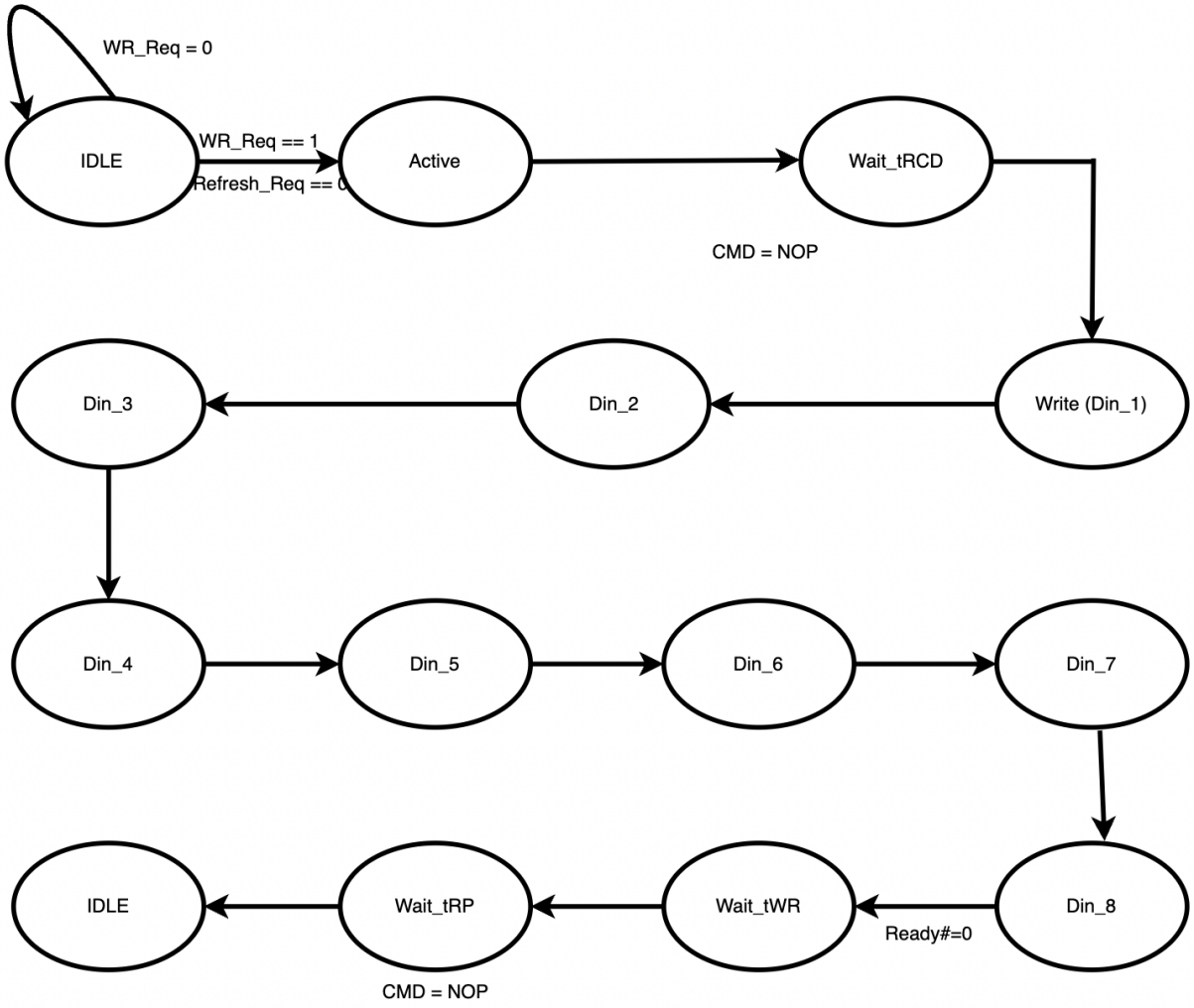

SDRAM Read
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
CLK
CLK 2
CKE
CS#
~State~
IDLE
ACTIVATE
wait tRCD
Send Read CMD
Wait CAS
Dout_1
Dout_2
Dout_3
Dout_4
Dout_5
Dout_6
Dout_7
Dout_8
CheckReadyState
IDLE
"CMD" (Label)
NOP
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
CMD
RAS#
CAS#
WE#
A0-A9,A11
Row Addr
Col Addr
A10
Row Addr
BA0,BA1
Bank
Bank
DQ
D0-3 Out
D4-7 Out
D8-11 Out
D12-15 Out
D16-19 Out
D20-23 Out
D24-27 Out
D28-31 Out
DQM
READY# (Output)
Time
a
7.5 ns OR 1 CLK
b
tRCD 15 ns
c
CAS Latency 2 CLKs
d
e
tRP 15 ns
f

5. Clock Cycles

Time	Value	No. of Clock Cycles
Precharge (tRP)	15ns	2
Auto_Refresh (tRFC)	66ns	9
CAS Latency (Wait_CL)	15ns	2
Active to Read/Write Delay (tRCD)	15ns	2

WRITE

State Diagram

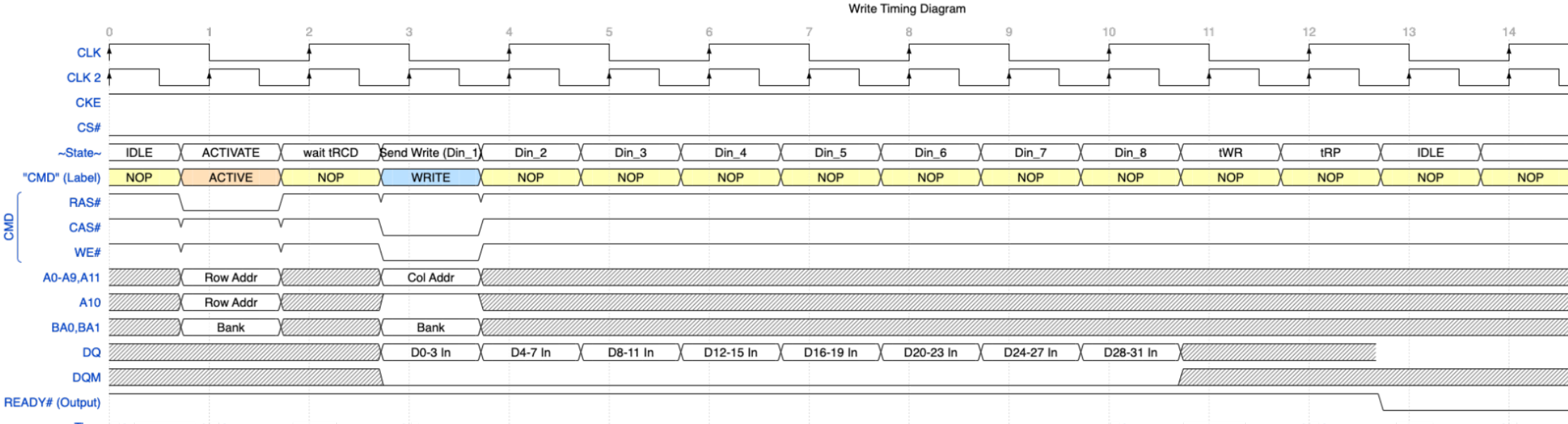


1. **State Transition Table**

State	Condition	Next State
IDLE	WR_Req = 0	IDLE
IDLE	WR_Req = 1 && Refresh_Req = 0	Active
Active	X	tRCD
tRCD	X	Write (Din_1)
Write (Din_1)	X	Din_2
Din_2	X	Din_3
Din_3	X	Din_4
Din_4	X	Din_5
Din_5	X	Din_6
Din_6	X	Din_7
Din_7	X	Din_8
Din_8	X	tWR
tWR	X	tRP
tRP	X	IDLE

2. Command Table

Signal	Enabled for State(s)
CKE	NOP, Active, Precharge, Write, Din_N, IDLE
CS#	NOP, Active, Precharge, Write, IDLE
RAS#	Active
CAS#	Write
WE#	Write
A0-A9/A11	Active, Write
A10	Precharge, Write, Active
BA0,BA1	Precharge, Active
DQ	Write

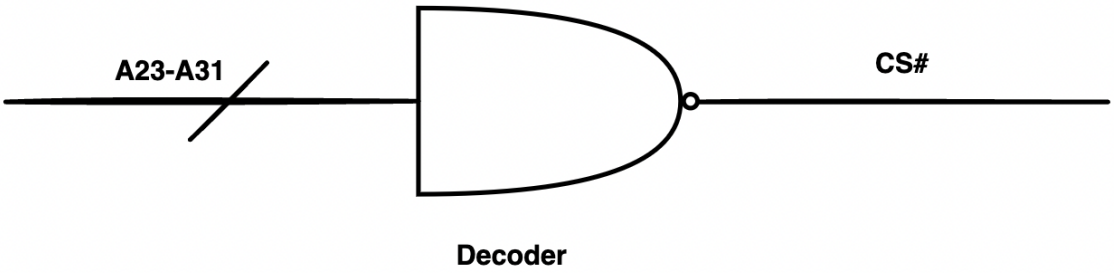

Write Timing Diagram
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
CLK
CLK 2
CKE
CS#
~State~
IDLE
ACTIVATE
wait tRCD
Send Write (Din_1)
Din_2
Din_3
Din_4
Din_5
Din_6
Din_7
Din_8
tWR
tRP
IDLE
"CMD" (Label)
NOP
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
CMD
RAS#
CAS#
WE#
A0-A9,A11
Row Addr
Col Addr
A10
Row Addr
BA0,BA1
Bank
Bank
DQ
D0-3 In
D4-7 In
D8-11 In
D12-15 In
D16-19 In
D20-23 In
D24-27 In
D28-31 In
DQM
READY# (Output)
Time
a
7.5 ns OR 1 CLK
b
tRCD 15 ns
c
d
tWR 1CLK + 7 ns
e
tRP 15 ns
f

4. Clock Cycles

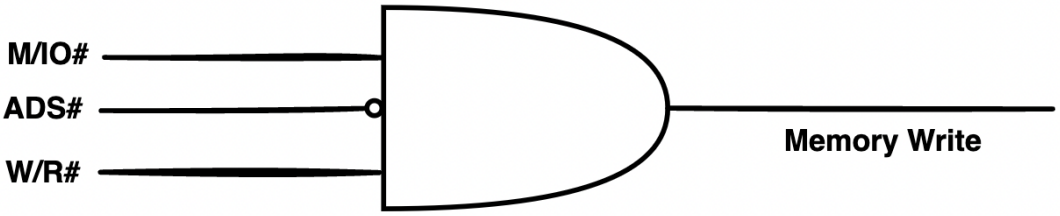
Time	Value	No. of Clock Cycles
Precharge (tRP)	15ns	2
Auto_Refresh (tRFC)	66ns	9
Active to Read/Write Delay (tRCD)	15ns	2
Write Recovery Time (tWR)	15ns	2

Signal Generation

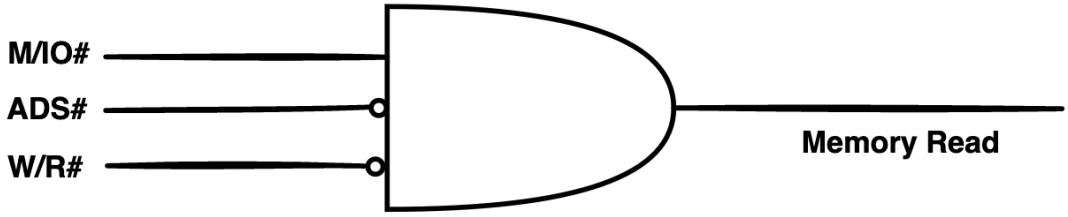
1. **Chip Select**



2. **Memory Write**

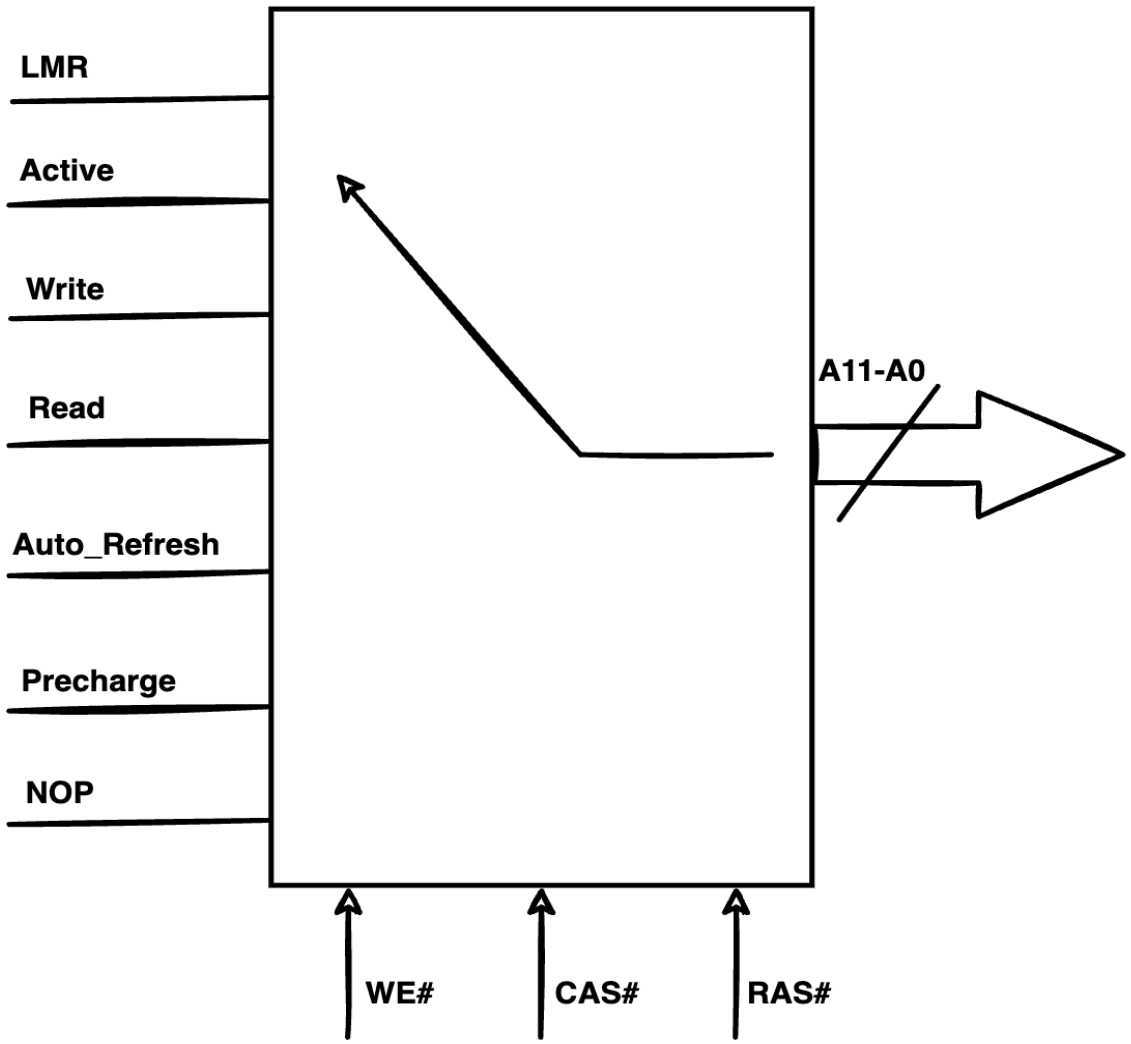


3. **Memory Read**



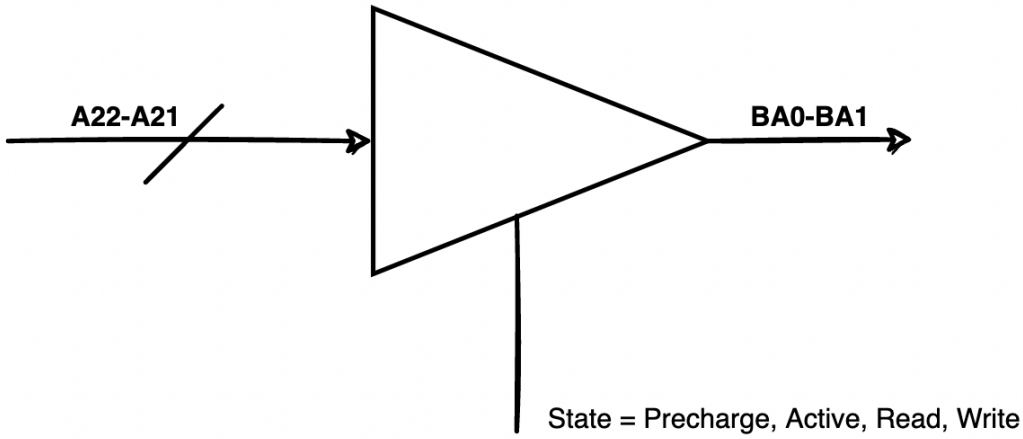
M/IO#	W/R#	Output
1	1	Memory W
1	0	Memory R
0	1	I/O Write
0	0	I/O Read

4. **Command Signal**

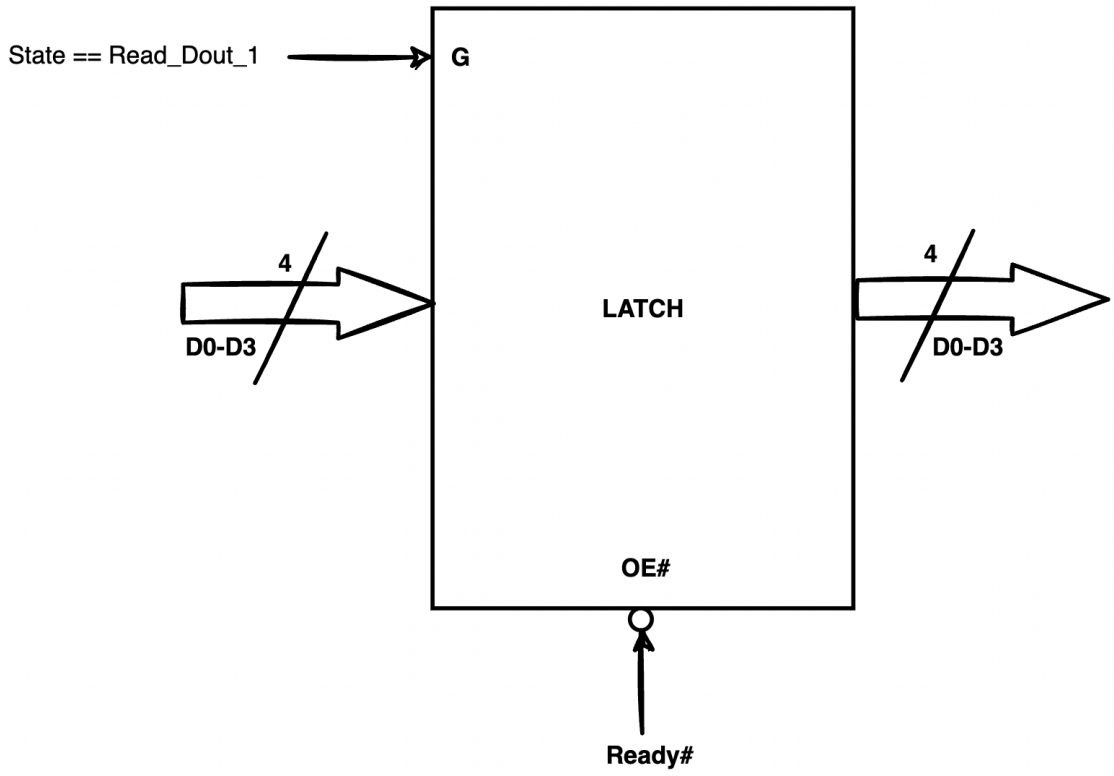


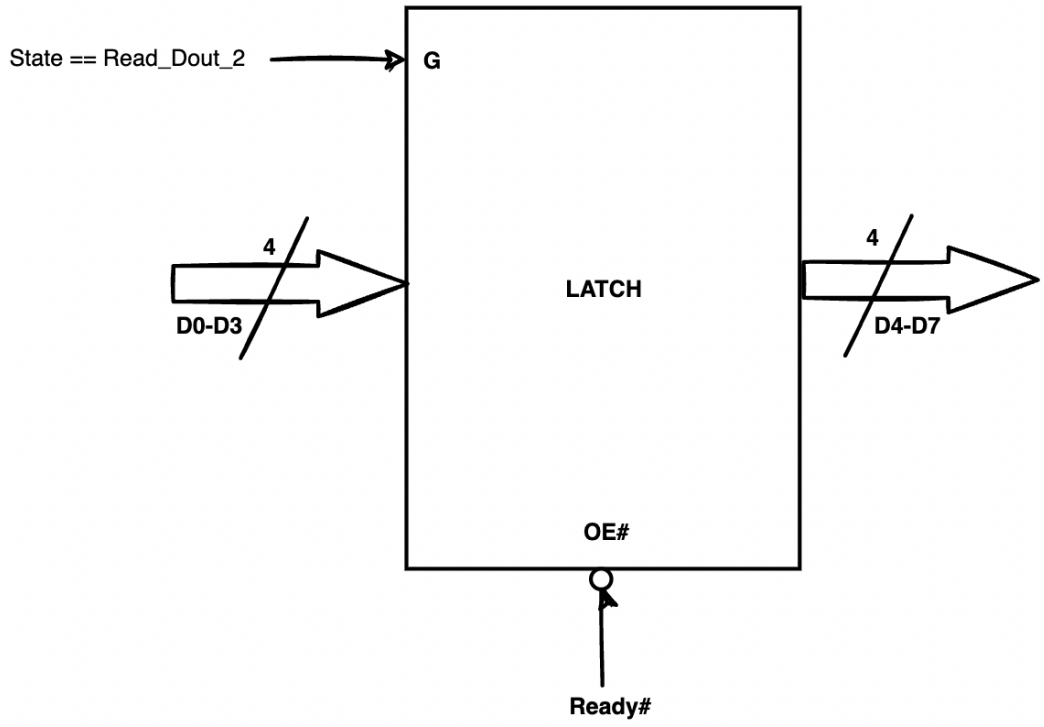
Command	WE#	CAS#	RAS#
LMR	0	0	0
Active	1	1	0
Write	0	0	1
Read	1	0	1
Auto_Refresh	1	0	0
NOP	1	1	1

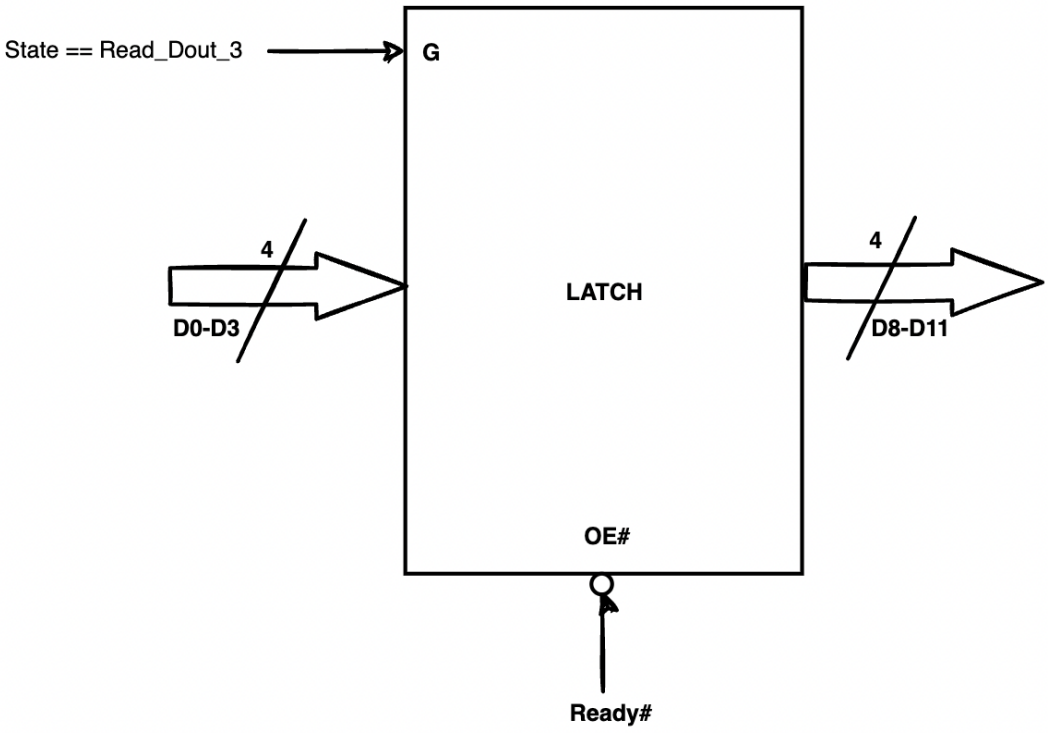
5. **Bank Addresses (Tri-State Buffer)**

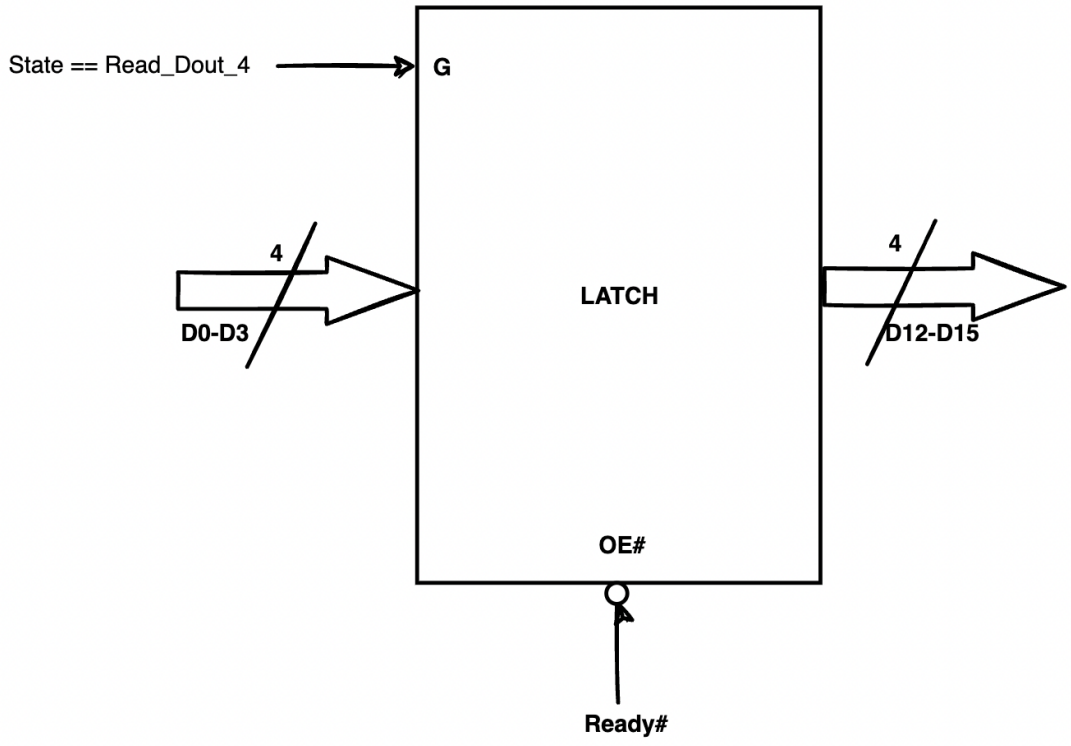


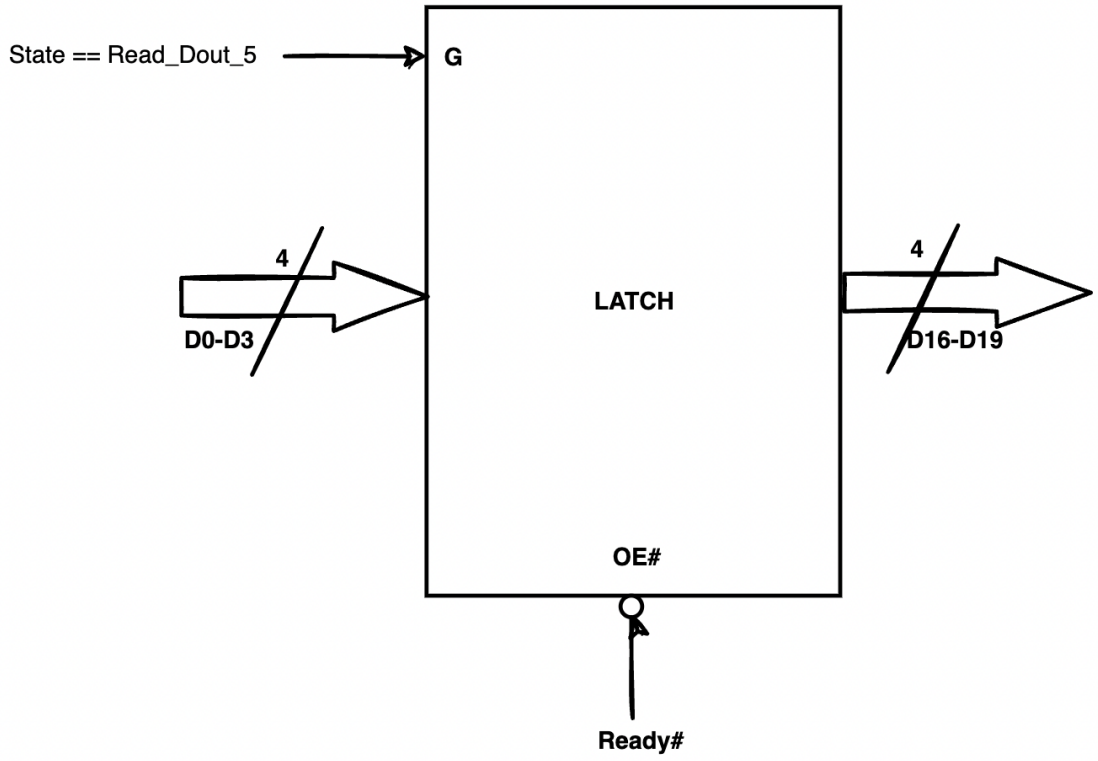
6. Latches for Read

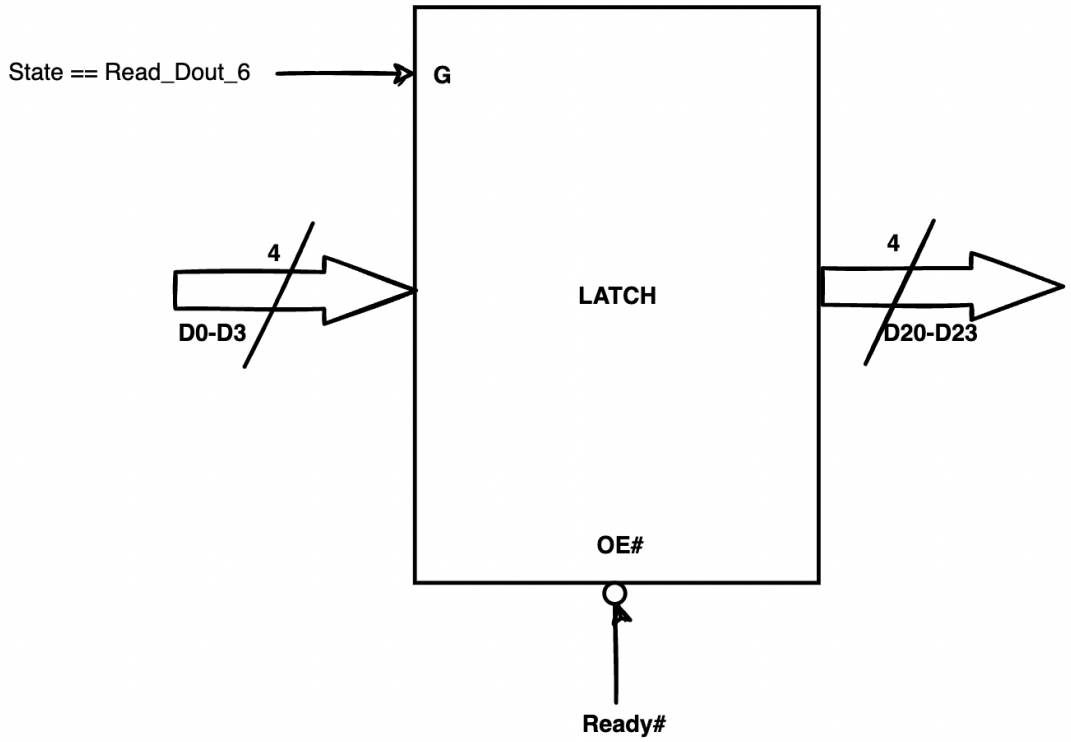


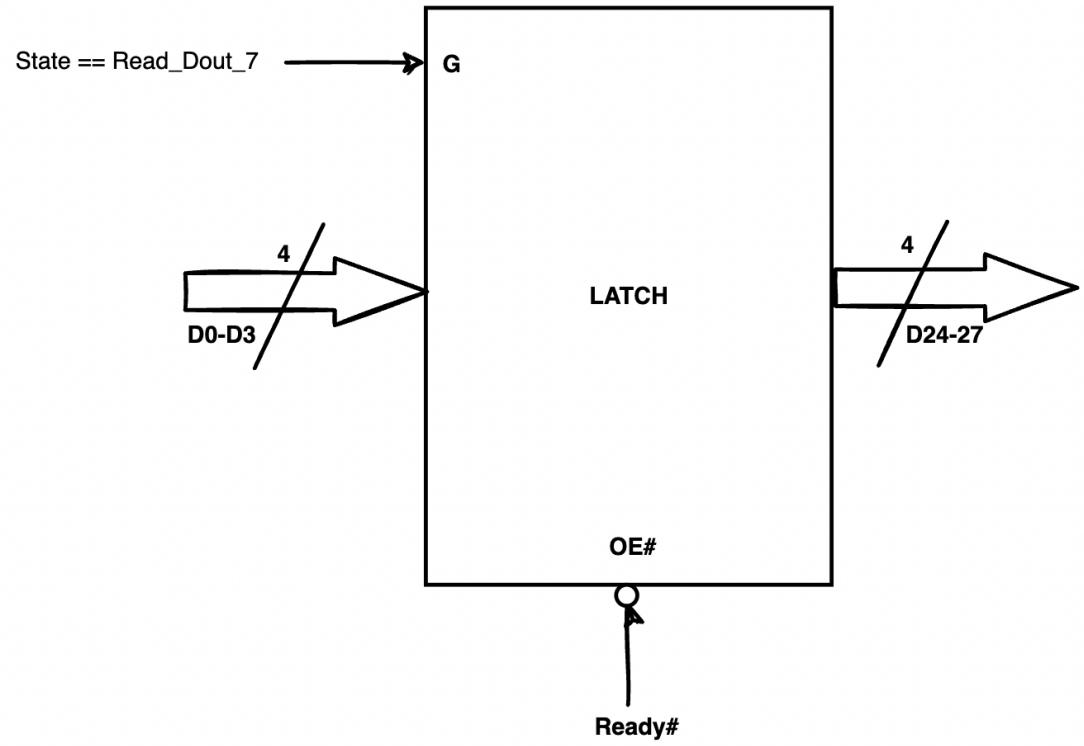


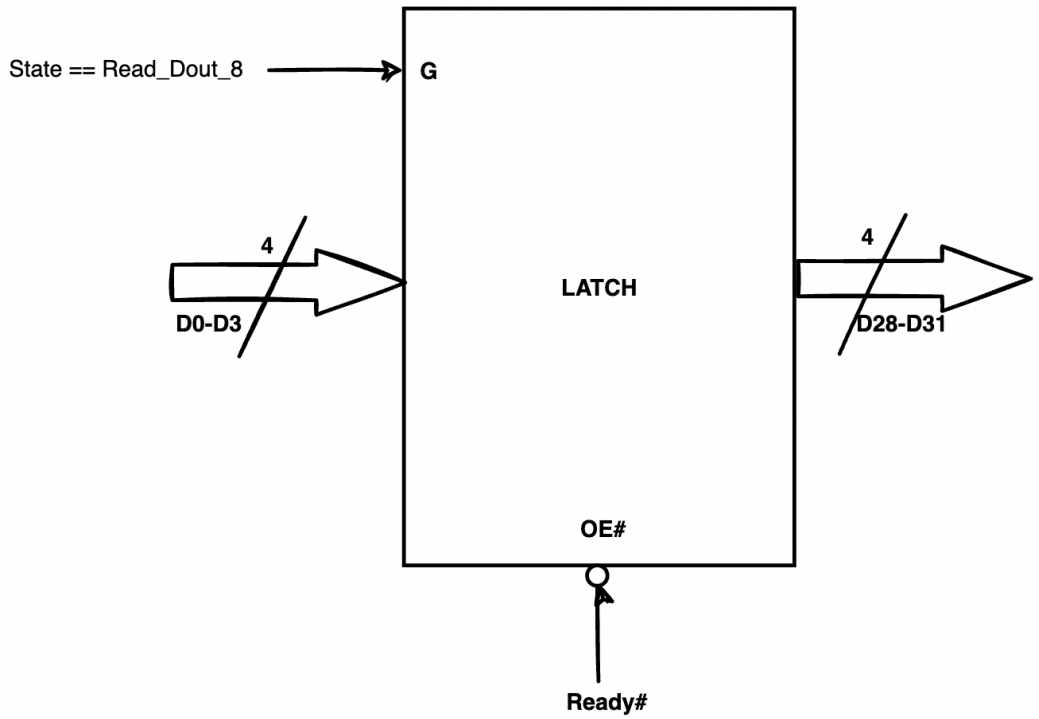

State == Read_Dout_3
G
4
D0-D3
LATCH
4
D8-D11
OE#
Ready#


State == Read_Dout_4
G
4
D0-D3
LATCH
4
D12-D15
OE#
Ready#


State == Read_Dout_5
G
4
D0-D3
LATCH
4
D16-D19
OE#
Ready#

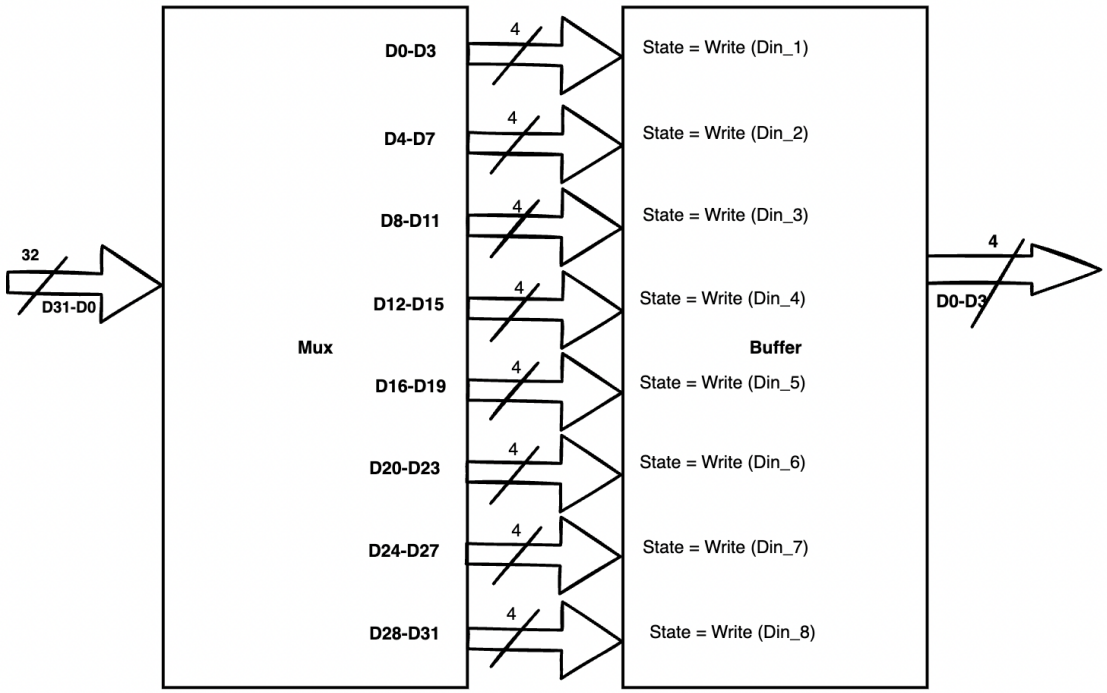

State == Read_Dout_6
G
4
D0-D3
LATCH
4
D20-D23
OE#
Ready#



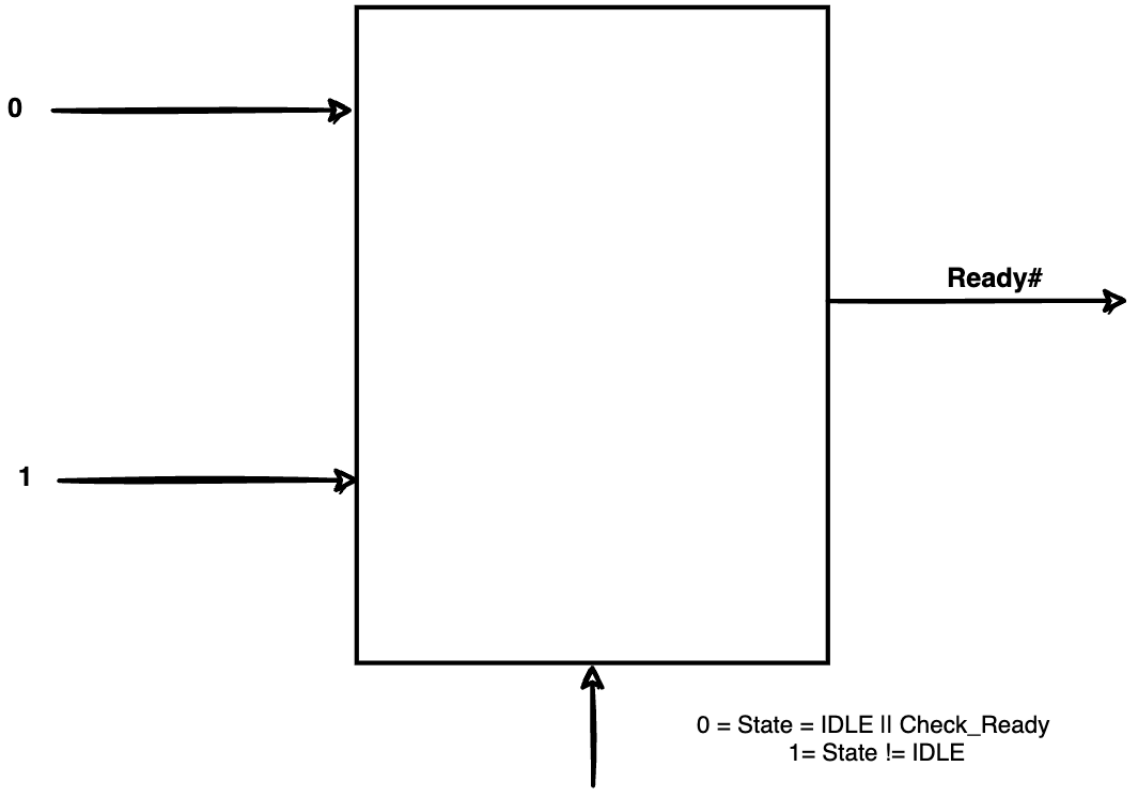


- Latches are done individually, but all 32 bits are outputted all at once, once done with an Output Enable pin.

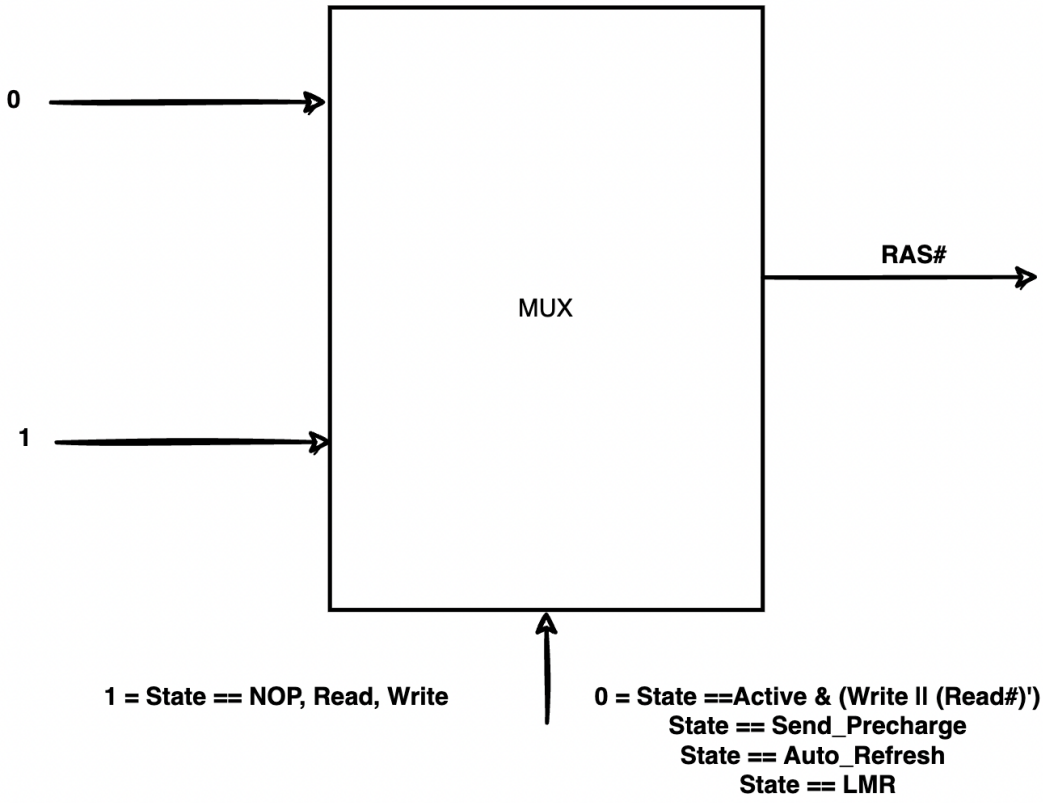
7. Buffer for Write



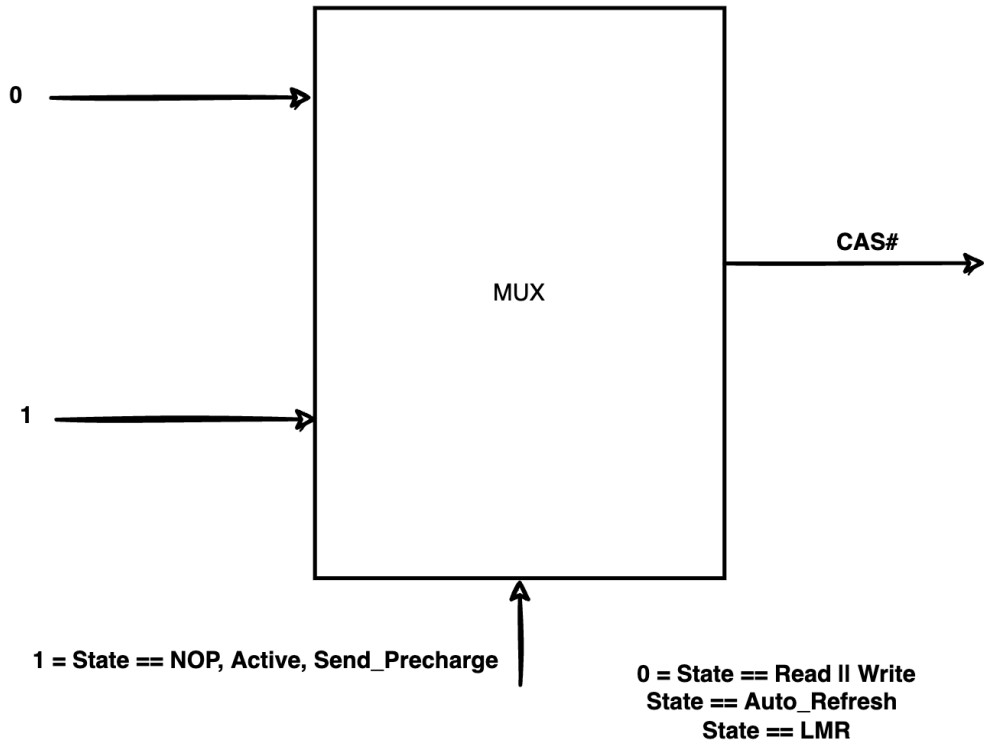
8. **Ready#**



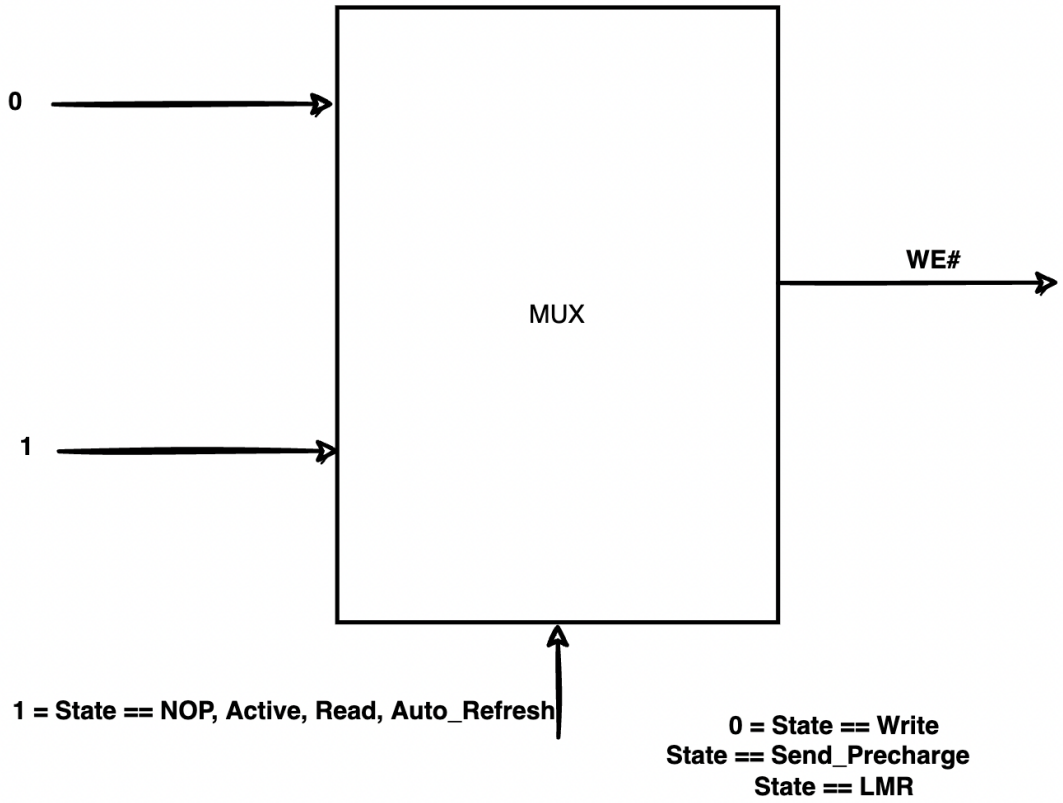
9. RAS#


0
1
MUX
RAS#
1 = State == NOP, Read, Write
0 = State ==Active & (Write II (Read#)')
State == Send_Precharge
State == Auto_Refresh
State == LMR

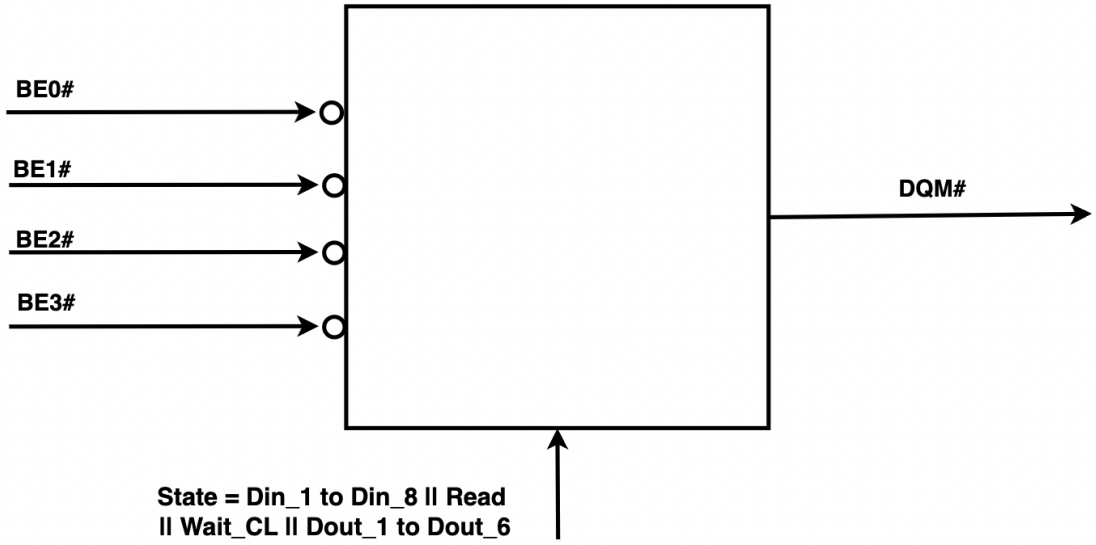
10. CAS#


0
1
MUX
CAS#
1 = State == NOP, Active, Send_Precharge
0 = State == Read II Write
State == Auto_Refresh
State == LMR

11. WE#

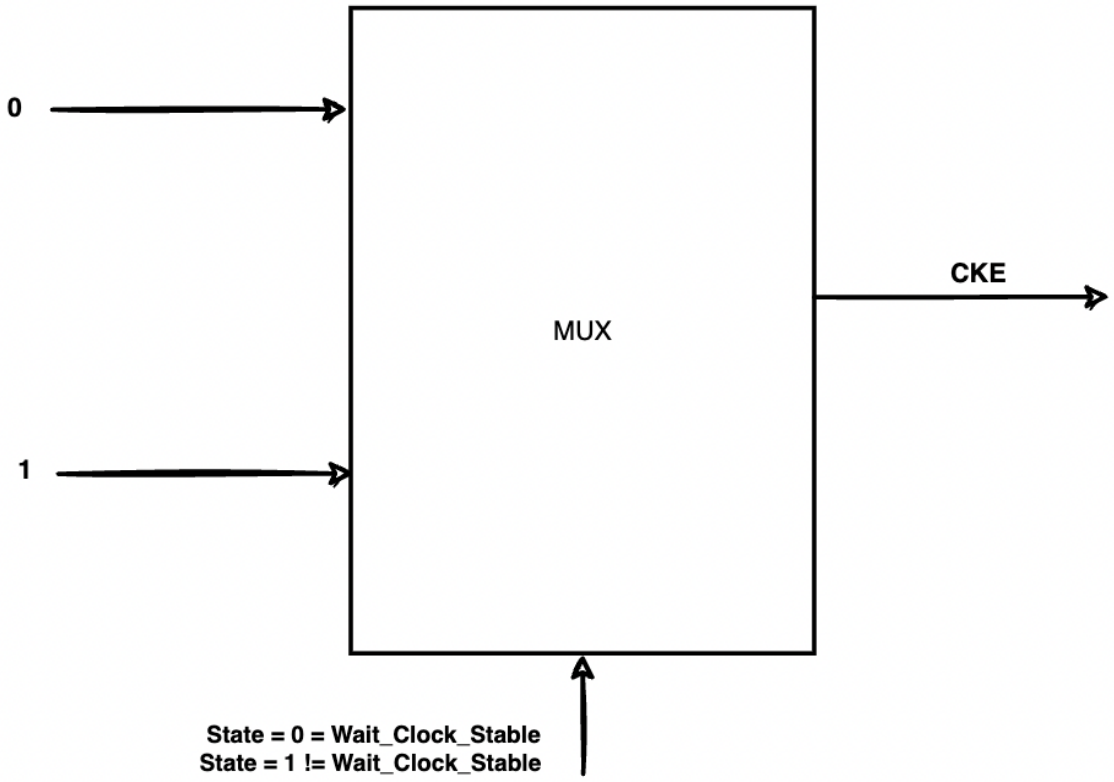

0
1
MUX
WE#
1 = State == NOP, Active, Read, Auto_Refresh
0 = State == Write
State == Send_Precharge
State == LMR

12. DQM

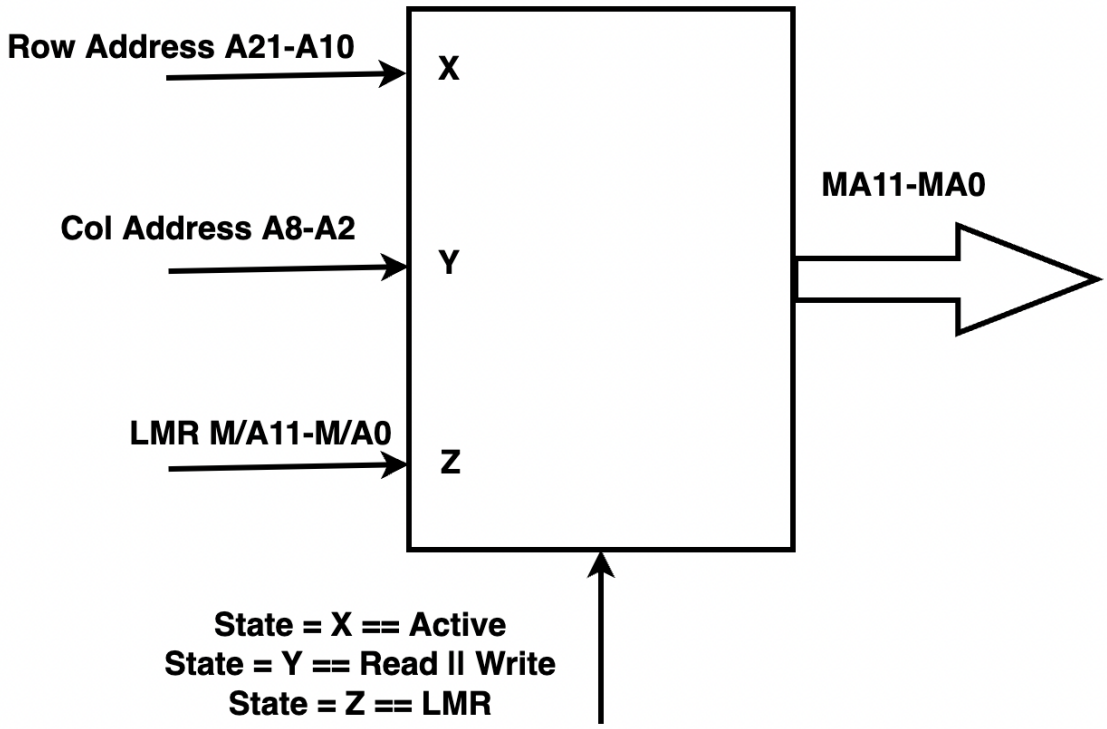


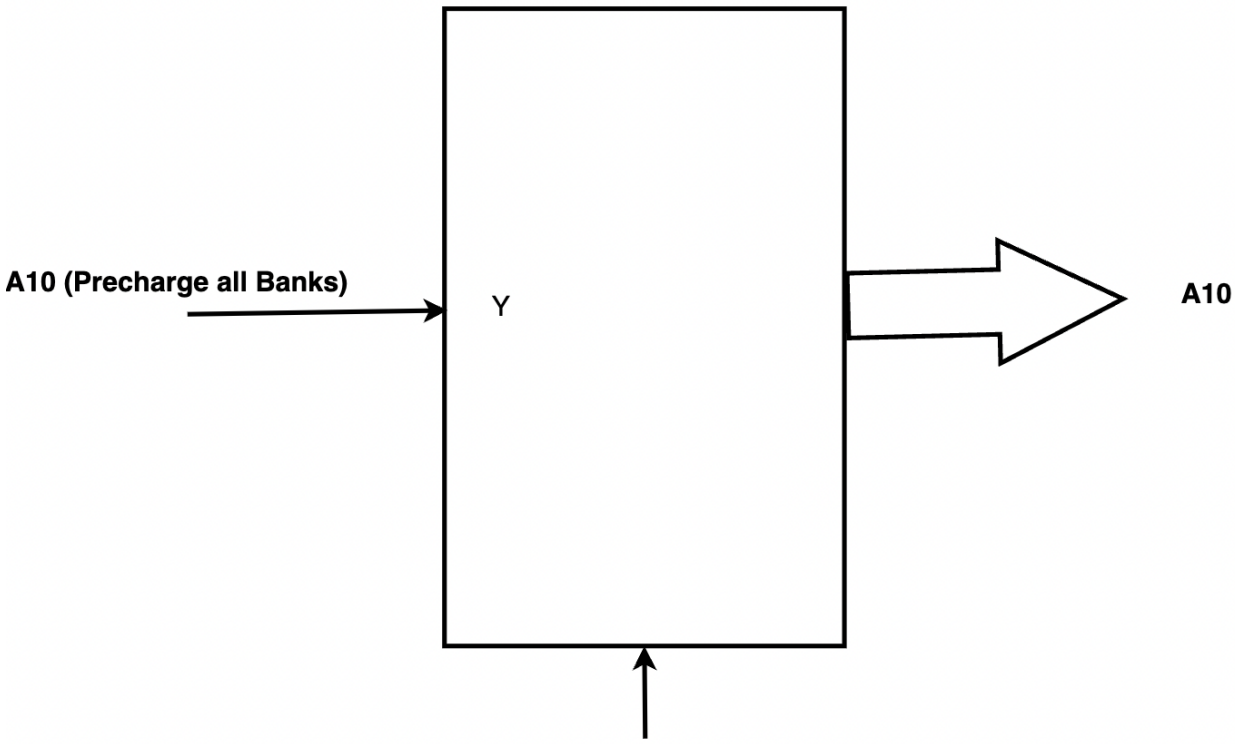
- BE0# -> D0-7
- BE1# -> D8-15
- BE2# -> D16-23
- BE3# -> D24-31
- Input of BE0# -> BE3# and CMD 3
- Bit state value (all of the D_x states), single output of DQM#.

13. CKE


0
1
MUX
CKE
State = 0 = Wait_Clock_Stable
State = 1 != Wait_Clock_Stable

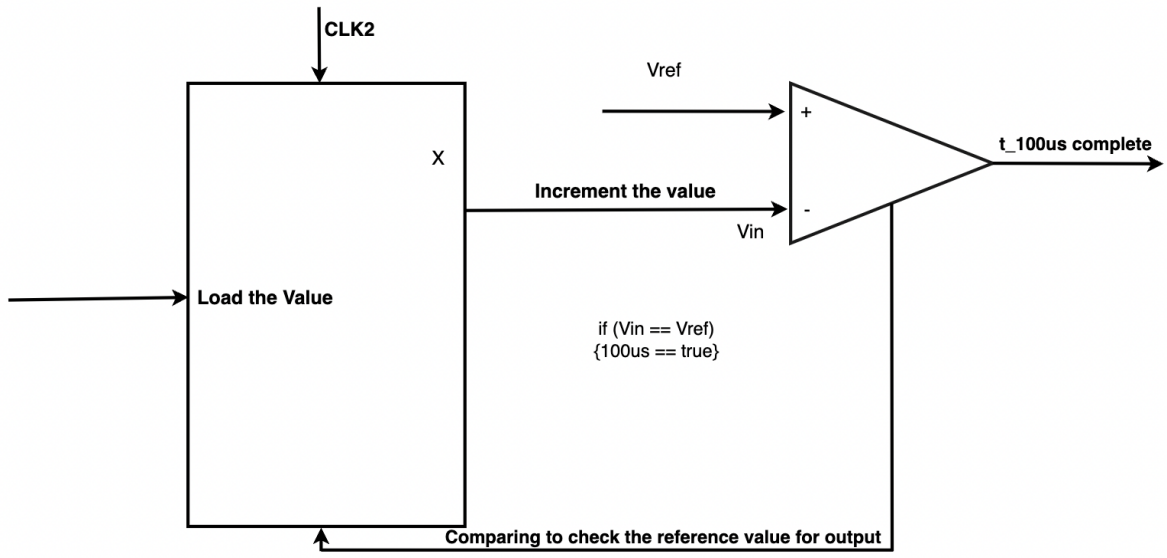
14. A0-A11 AND A10



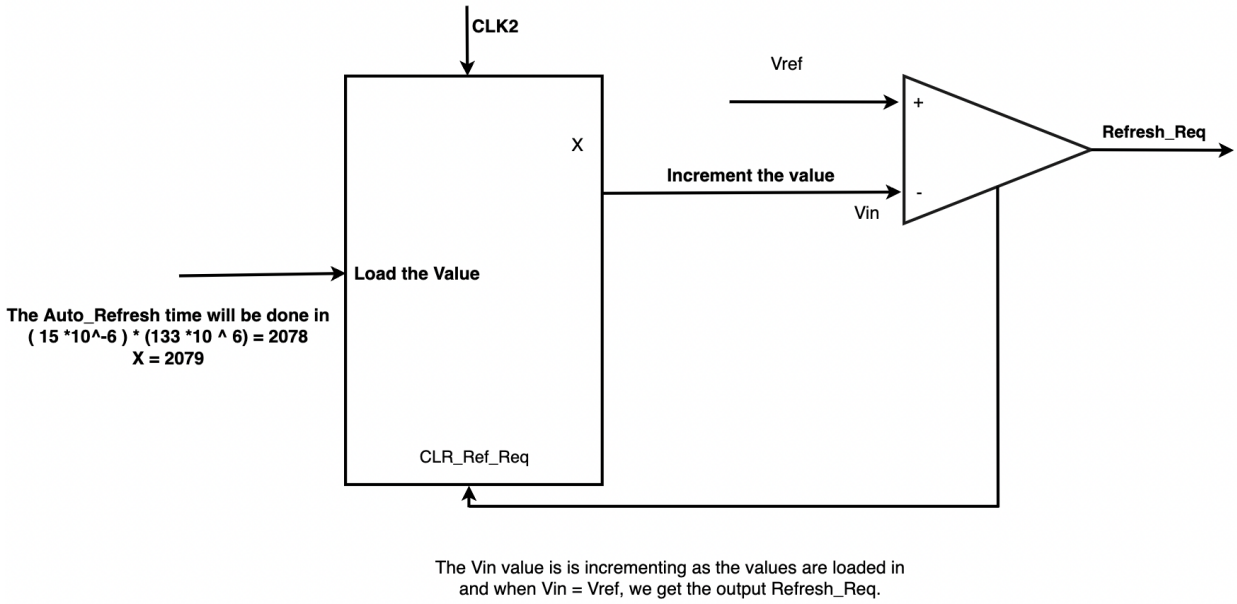


State = Y == Send_Precharge
When A10 is low, the Send_Precharge to selected banks is done through BA1,BA0

15. Counter



16. Refresh Timer



The Vin value is is incrementing as the values are loaded in and when Vin = Vref, we get the output Refresh_Req.