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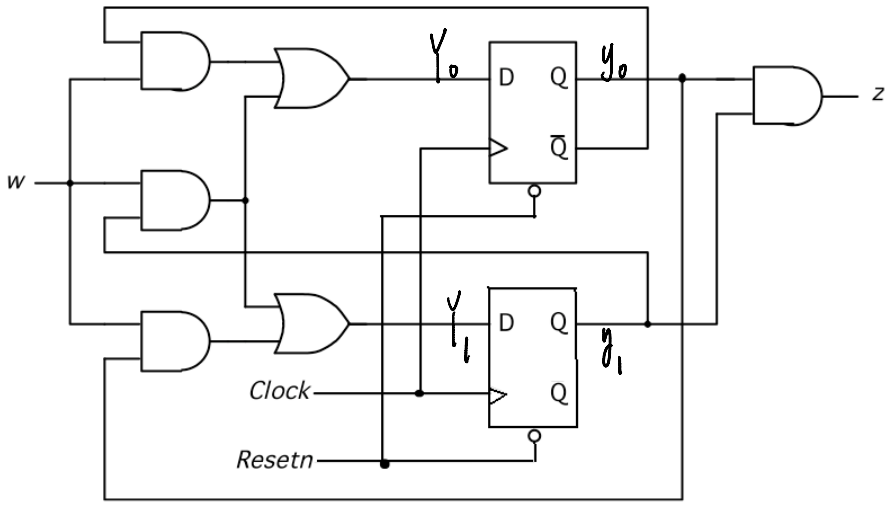
What is this logic circuit doing?



more or mealy?

$z = y_1 y_0$

$Y_0 = \bar{y}_0 w + y_1 w$, $Y_1 = y_0 w + y_1 w$

Decoded state table

Present state $y_1 y_0$	Next state $Y_1 Y_0$ w=0	Next state $Y_1 Y_0$ w=1	output z
A = 0 0	A = 0 0	B = 0 1	0
B = 0 1	A = 0 0	C = 1 0	0
C = 1 0	A = 0 0	D = 1 1	0
D = 1 1	A = 0 0	D = 1 1	1

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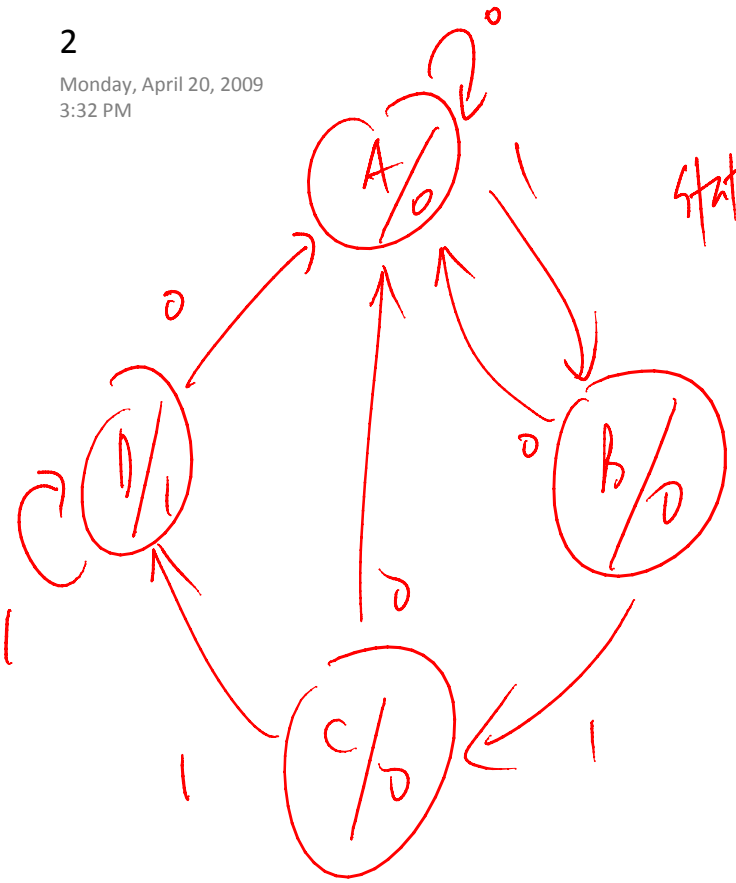

state diagram from decoded state table

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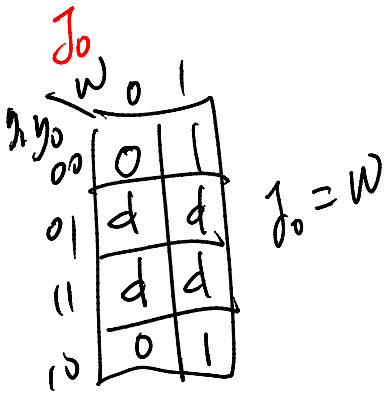
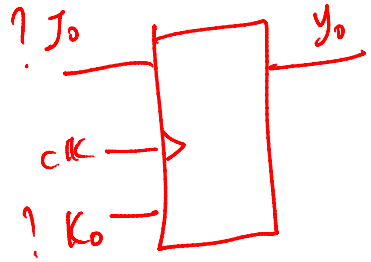
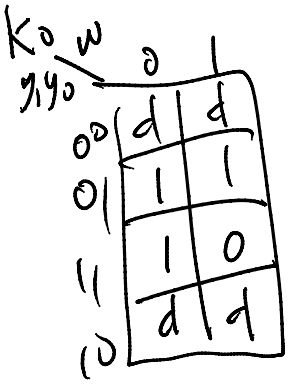
Figure 8.79 (a) page 557 Implement using jk-flip-flop

Present y_1y_0	Next State $w=0$ Y_1Y_0	J_1K_1 J_0K_0	$w=1$ Y_1Y_0	J_1K_1 J_0K_0	output
0 0	0 0	0d 0d	0 1	0d 1d	0
0 1	0 0	0d d1	1 0	1d d1	0
1 0	0 0	d1 0d	1 1	d0 1d	0
1 1	0 0	d1 d1	1 1	d0 d0	1

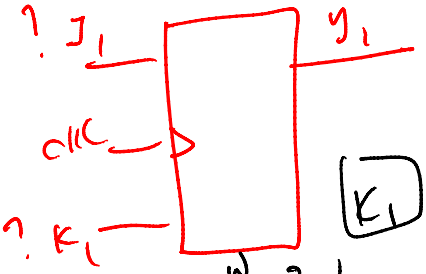


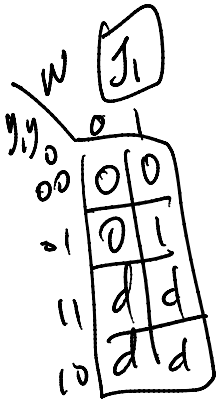
$J_0 = w$



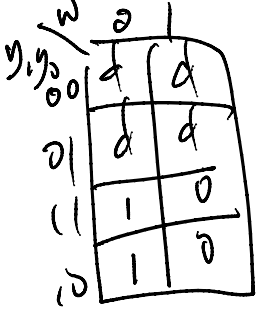


$K_0 = \bar{w} + y_1$





$J_1 = w y_0$



$K_1 = \bar{w}$