Boise State University
Department of Electrical and Computer Engineering
EE 230 Digital Systems
Test 3 – April 21, 2005

Name: Key

Instructions: Show all steps and logic circuits for full or partial credits. It is very important that you write clearly, so that your test can be graded appropriately and fairly. This is a closed book and closed notes test.

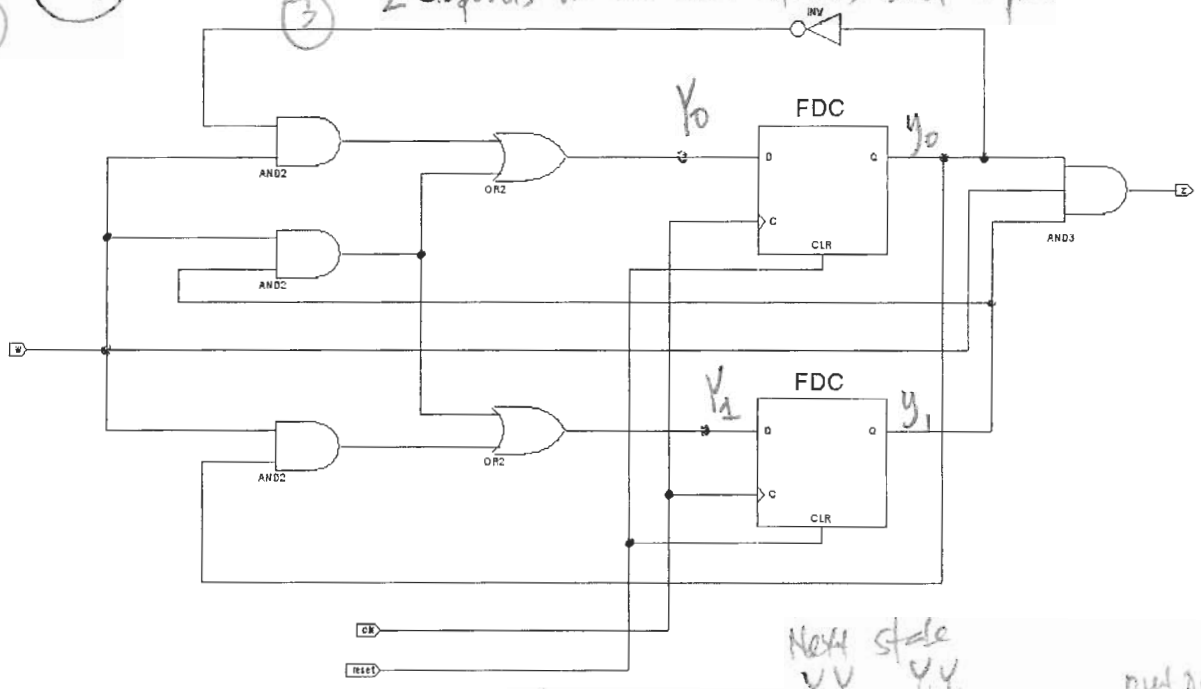
1. (5 points) Explain the basic differences between a latch and a flip-flop.

latch: level Sensitive
flip-flop: edge Sensitive

2. (5 points) Explain the basic differences between combination and sequential digital circuits.

memory

3. (15 points) Derive the state and output equations, and state-assignment table for the circuit shown. Is this a Moore or Mealy state machine? Why? Z depends on current states and input



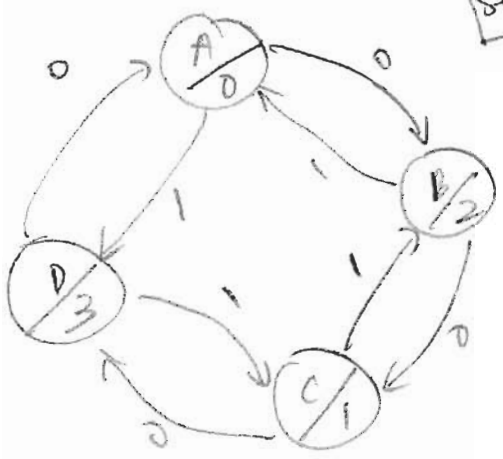
$Z = W y_0 y_1$

$Y_0 = \bar{y}_0 W + y_1 W$

$Y_1 = y_1 W + y_0 W$

Present state $y_1 y_0$	Next state $Y_1 Y_0$ $W=0$	Next state $Y_1 Y_0$ $W=1$	Output $W=0$	Output $W=1$
00	01	01	0	0
01	00	10	0	0
10	00	11	0	0
11	00	11	0	1

4. (30 points) Design (*includes the state diagram, state table, state-assigned table, and logic circuit*) a counter that counts in the sequence 0, 2, 1, 3 when $w = 0$. If $w = 1$, the count sequence is reverse which is 3,1,2,0. Use D flip-flops for your design. Use Moore state machine design method.



State table

Present State	Next State $w=0$	Next State $w=1$	output
A	B	D	0
B	C	A	2
C	D	B	1
D	A	C	3

State-assigned table

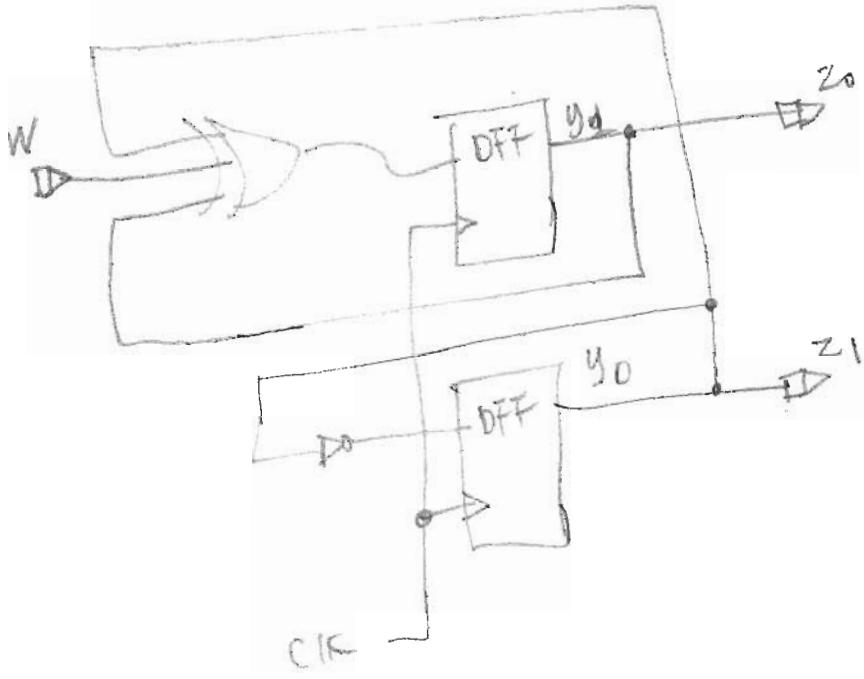
Present state $Y_1 Y_0$	Next state $w=0$ $Y_1 Y_0$	Next state $w=1$ $Y_1 Y_0$	output $Z_1 Z_0$
00	01	11	00
01	10	00	10
10	11	01	01
11	00	10	11

Y_1

w \ $y_1 y_0$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Y_0

w \ $y_1 y_0$	00	01	11	10
0	1	0	0	1
1	1	0	0	1



$Y_1 = w \oplus y_1 \oplus y_0$

$Y_0 = \bar{y}_0$

Z_1

y_1 \ y_0	0	1
0	0	1
1	0	1

$Z_1 = y_0$

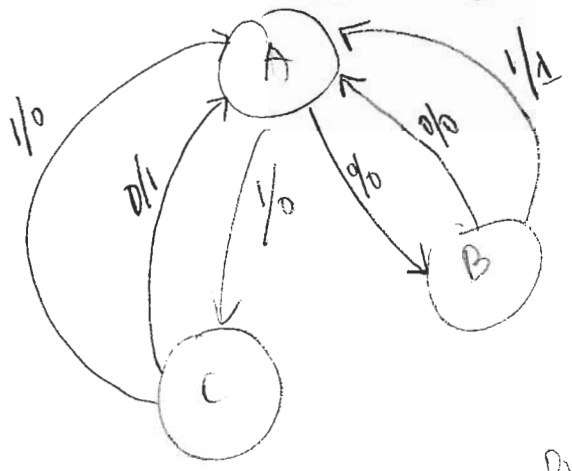
Z_0

y_1 \ y_0	0	1
0	0	0
1	1	1

$Z_0 = y_1$

5. (45 points) A given finite state machine has an input, w, and an output, z. During two consecutive clock pulses, a sequence of two values of the w signal is applied. Design a finite state machine that produces $z = 1$ when it detects that either the sequence w : 01 or w : 10 has been applied; otherwise, $z = 0$. After the second clock pulse, the machine has to be again in the reset state (or initial state), ready for the next sequence. Use one-hot encoding. You should show the state **diagram, state table,** state-assigned table (one-hot encoding), and the logic equations.

(15) (10) (10)



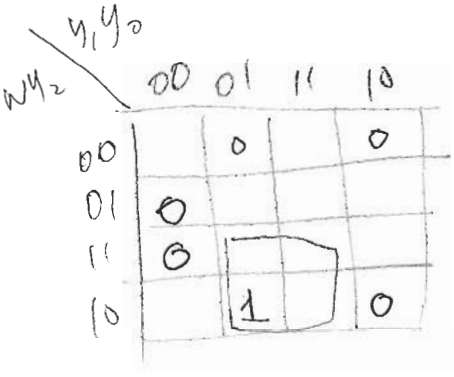
(10) State table

Present State	Next State w=0	Next State w=1	output w=0	output w=1
	B	C	0	0
A	A	A	0	1
B	A	A	1	0
C				

State-assigned table (one-hot encoding)

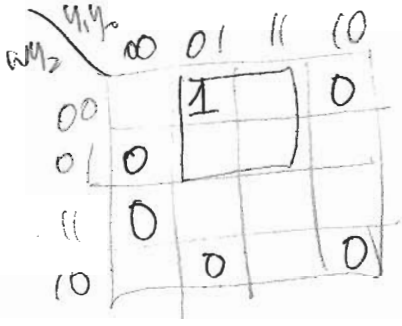
Present State $Y_2 Y_1 Y_0$	Next State w=0 $Y_2 Y_1 Y_0$	Next State w=1 $Y_2 Y_1 Y_0$	output w=0	output w=1 (z)
001	010	100	0	0
010	001	001	0	1
100	001	001	1	0

Y_2



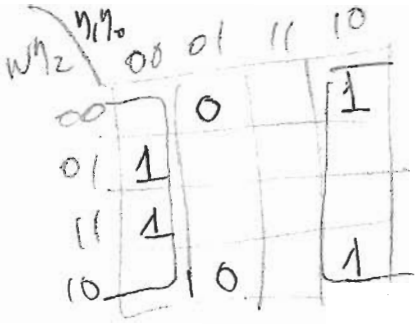
$Y_2 = wY_0$

Y_1



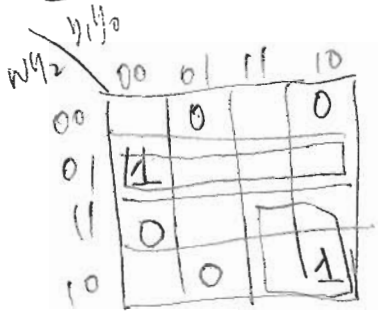
$Y_1 = w'Y_0$

Y_0



$Y_0 = Y_1' Y_0'$

Z



$Z = w'Y_2 + wY_1$