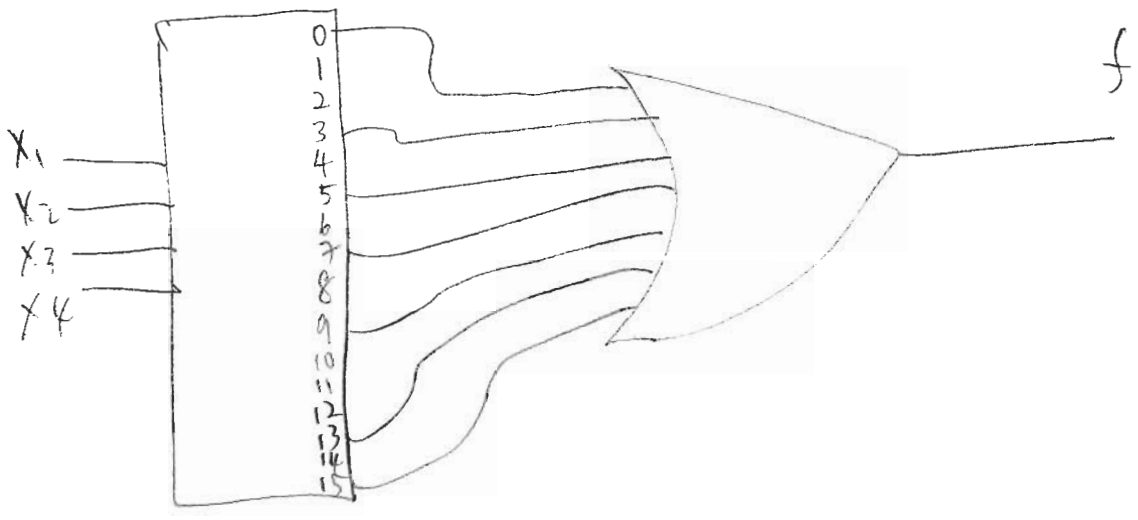
Boise State University
Department of Electrical and Computer Engineering
EE 230 Digital Systems
Test 2 – March 17, 2005

Name: Key

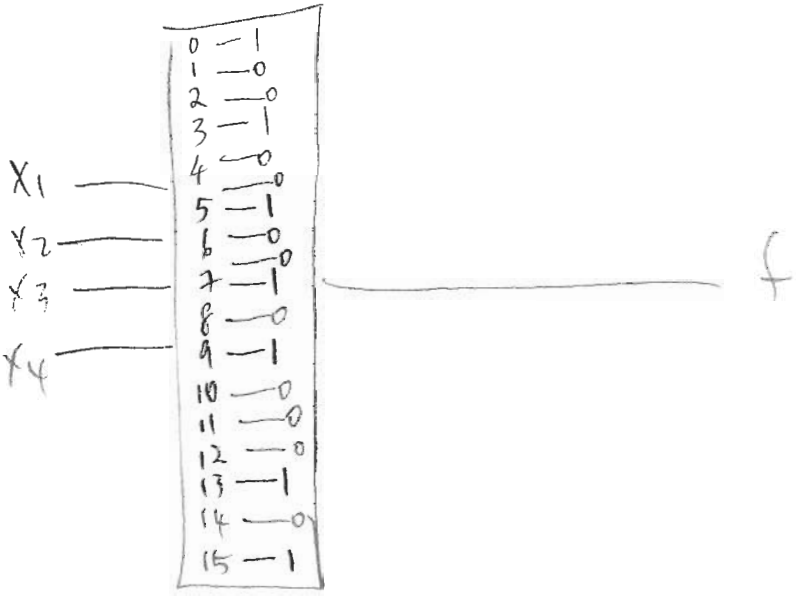
Instructions: Show all steps and logic circuits for full or partial credits. It is very important that you write clearly, so that your test can be graded appropriately and fairly. This is a closed book and closed notes test.

1. (10 points) Show how the function $f(x_4, x_3, x_2, x_1) = \Sigma m(0,3,5,7,9,13,15)$, where x_4 is MSB and x_1 is LSB, can be implemented using

a. one 4-to-16 decoder and an OR gate, and



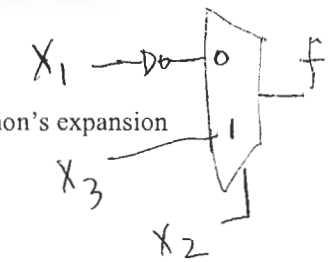
b. one 4-input LUT.



or using X_2

$f = X_2'(X_3'X_1' + X_3X_1') + X_2(X_3X_1' + X_3X_1)$

$= X_2'(X_1') + X_2(X_3)$



2. (15 points) For the function $f(x_3, x_2, x_1) = \Sigma m(0,4,6,7)$, where x_3 is MSB and x_1 is LSB, use Shannon's expansion to derive an implementation using a 2-to-1 multiplexer and any other necessary gates.

using X_3

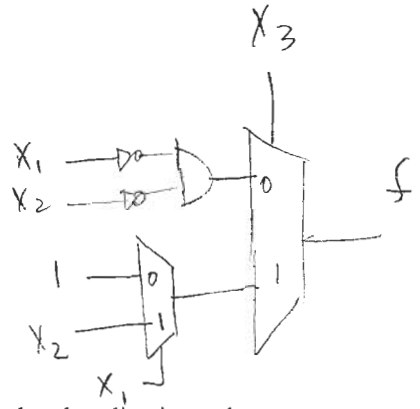
$f = X_3'X_2'X_1' + X_3X_2'X_1' + X_3X_2X_1' + X_3X_2X_1$

$= X_3' f_{X_3'} + X_3 f_{X_3}$

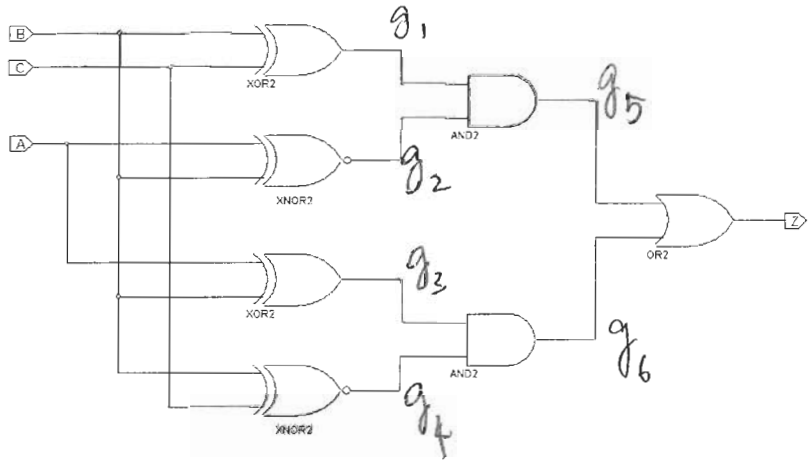
$= X_3'(X_2'X_1') + X_3(X_2'X_1' + X_2X_1' + X_2X_1)$

$= X_3'(X_2'X_1') + X_3(X_1'(X_2' + X_2) + X_1X_2)$

$= X_3'(X_2'X_1') + X_3(X_1' + X_1X_2)$



3. (25 points) Reverse engineer the circuit shown in the schematic in order to derive a two-level realization, where A is MSB and C is LSB.



a. Find the Boolean expression that describes the circuit (*Label and find the intermediate expressions, and the final expression, Z*).

$g_1 = BC' + B'C$

$g_2 = A'B' + AB$

$g_3 = A'B + AB'$

$g_4 = B'C' + BC$

$g_5 = g_1g_2 = A'B'C + ABC'$

$g_6 = g_3g_4 = A'BC + AB'C'$

$Z = g_5 + g_6 = A'C + AC' = A \oplus C$

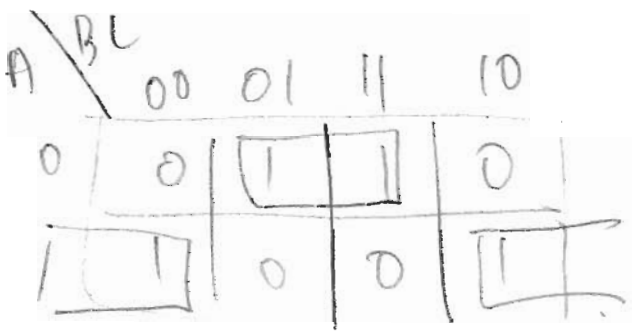
b. Construct the truth table for the function, Z.

A	B	C	g_1	g_2	g_3	g_4	g_5	g_6	Z
0	0	0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	1	0	1
0	1	0	1	0	1	0	0	0	0
0	1	1	0	0	1	1	0	1	1
1	0	0	0	0	1	1	0	1	1
1	0	1	1	0	1	0	0	0	0
1	1	0	1	1	0	0	1	0	1
1	1	1	0	1	0	1	0	0	0

c. Write the function in canonical sum-of-products form (*The function, Z, from truth table without simplification.*).

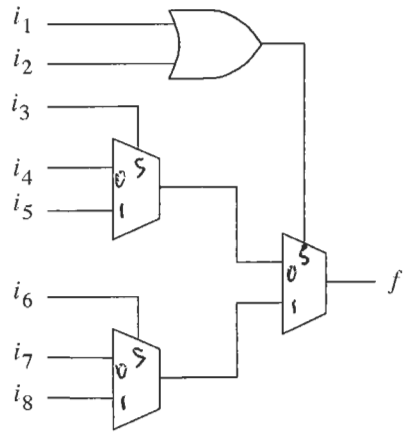
$$Z = A'B'C + A'BC + AB'C' + ABC$$

d. Simplify the function, Z, using K-maps.



$$Z = A'C + AC'$$
$$= A \oplus C$$

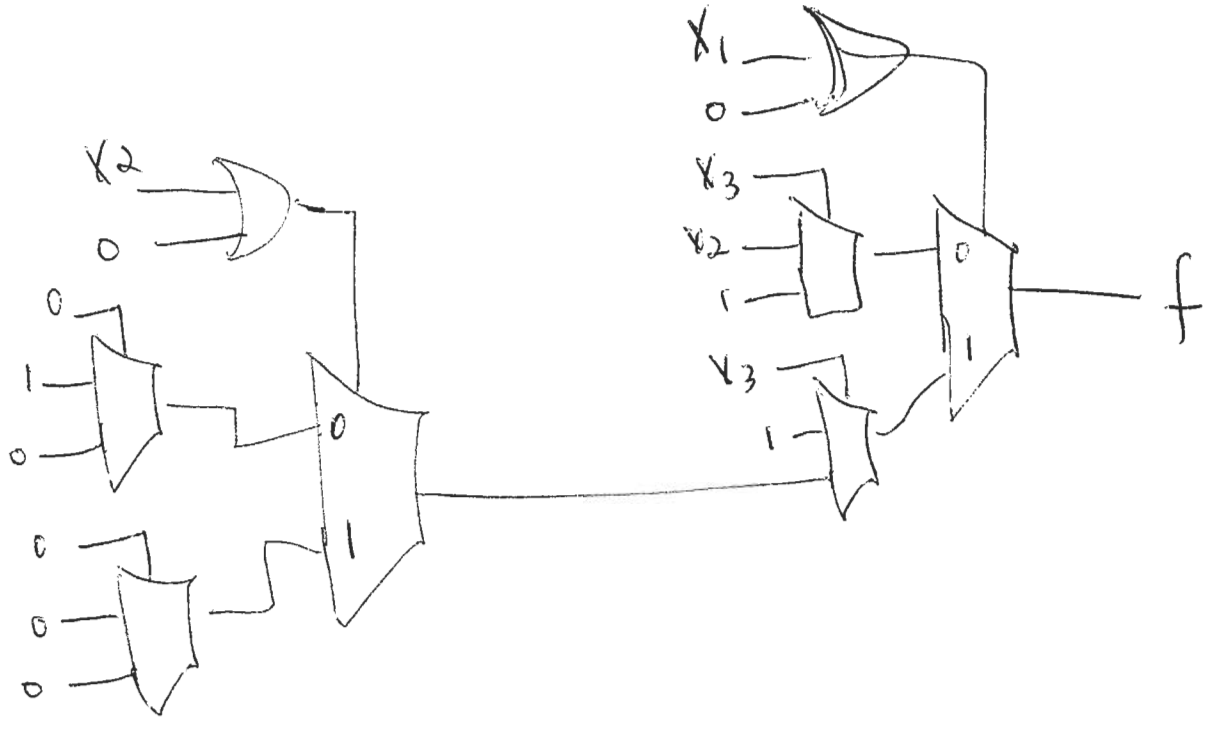
5. (10 points) Show how the function $f = x_1x_3' + x_1'x_3 + x_1x_2x_3' + x_1x_2' + x_1'x_2x_3'$ can be realized using Act 1 logic blocks (Act 1 logic block is shown). Note that there are no NOT gates in the chip; hence complements of signals have to be generated using the multiplexers in the logic block.



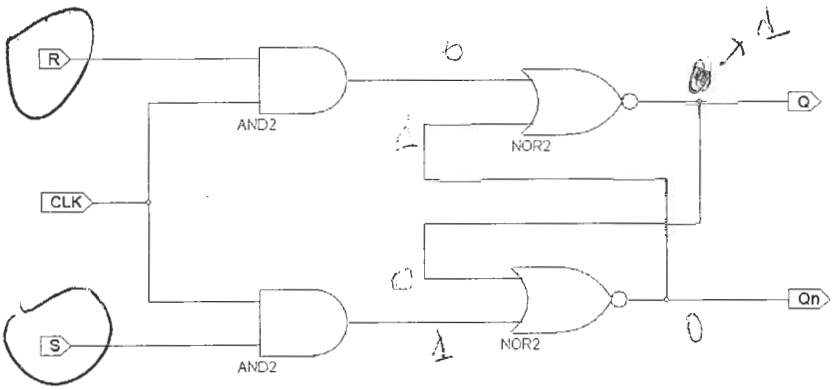
$$f = x_1'(x_3 + x_2x_3') + x_1(x_3' + x_2x_3' + x_2')$$

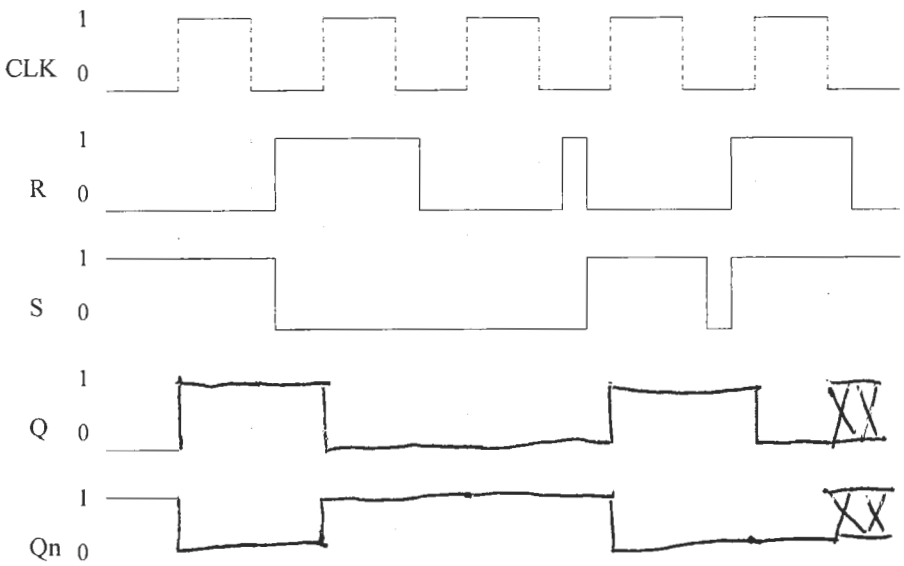
$$= x_1'[x_3'(x_2) + x_3(1)] + x_1[x_3'(1 + x_2 + x_2') + x_3(x_2')]$$

$$= x_1'[x_3'(x_2) + x_3(1)] + x_1[x_3'(1) + x_3(x_2')]$$



6. (15 points) Complete the following timing diagram.





6. (20 points) Design a shifter circuit, which can shift a four-bit input vector, $\mathbf{W}=w_3w_2w_1w_0$, one bit-position to the right when the control signals are *S1=0 and S0=1*, and one bit-position to the left when the control signals are *S1=1 and S0=0*. When *S1=0 and S0=0* the output of the circuit should be the same as the input vector. When the condition *S1=1 and S0=1* occurs, the shifter will carry out a right rotate. [Hint: Use four 4-to-1 multiplexers]

S_1	S_0	Shift operation
0	0	flow through
0	1	right
1	0	left
1	1	rotate right