Average 45 which 69% | 90% 58.5 | 80% 52 | 70% 45.5

/65

Boise State University
Department of Electrical and Computer Engineering
ECE 230 Digital Systems
Test 2, Date: April 6, 2009, Location: ET 110, Time: 1:40pm to 2:30pm

Name: key

Instructions: *Show all steps and logic circuits for full or partial credits. It is very important that you write clearly, so that your test can be graded appropriately and fairly. This is a closed book and closed notes test.* ***ABSOLUTELY NO calculator.***

range −128 to 127

1. (15 points) Complete the following using 8-bit signed number (using 2's complement) representation. You need to indicate whether arithmetic overflow occurs. What is the range of 8-bit signed number using 2's complement number representation? (2)

128 64 32 16 8 4 2 1

5 (a)

98_{10}
$-(-33_{10})$

131

0 1 1 0 0 0 1 0 — 98
0 0 1 0 0 0 0 1 — 33

01100010
+00100001
01000011

overflow! 137 > 127

convert (2), Addition (2), (1) overflow

4 (b) 32 16 8 4 2 = 62

00111110
− 01000111 — 71

−9

00111110
+10111001
11110111

no overflow

4 (c) −128 64 4 2 1

11000111
−11010010

−128 + 71 = −57
−128 + 82 = −46

−57
+46
−11

11000111
+00101110
11110101

no overflow

2. (10 points) Short answers and fill in the blanks.
a. What is the key difference between a half-adder and full-adder? carry in
b. Latch is ___level___ sensitive.
c. Flip-flop is ___edge___ sensitive.
d. A multiplexer circuit has a number of ___data___ inputs, one or more select inputs, and ___one___ output.
e. Why is 2's complement better for implementing arithmetic logics than 1's complement?
no conversion needed, with 1's complement and sign-magnitude, adjust is required

total 25

$A = A_3 A_2 A_1 A_0$

$B = B_3 B_2 B_1 B_0$

$A < B$

$A \Rightarrow 0 \times \times \times$

$B \Rightarrow 1 \times \times \times$

$f = \bar{A}_3 B_3$

$A \Rightarrow \%_1\ 0 \times \times$

$B \Rightarrow \%_0\ 1 \times \times$

$f = \bar{A}_3 B_3 + (A_3 \odot B_3)\bar{A}_2 B_2$

$A \Rightarrow \%_1\ \%_1\ 0 \times$

$B \Rightarrow \%_1\ \%_1\ 1 \times$

$f = \bar{A}_3 B_3 + (A_3 \odot B_3)\bar{A}_2 B_2 + (A_3 \odot B_3)(A_2 \odot B_2)\bar{A}_1 B_1$

$A \Rightarrow \%_1\ \%_1\ \%_1\ 0$

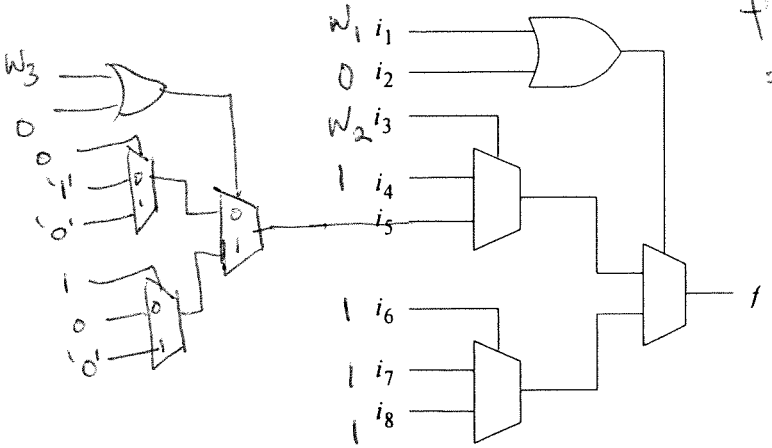
$B \Rightarrow \%_1\ \%_1\ \%_1\ 1$

$f = \bar{A}_3 B_3 + (A_3 \odot B_3)\bar{A}_2 B_2 + (A_3 \odot B_3)(A_2 \odot B_2)\bar{A}_1 B_1 +$

$(A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)\bar{A}_0 B_0$

$(\bar{w}_1 + w_1)\bar{w}_2$

3. (10 points) Show how the function $f = \bar{w}_2 + \bar{w}_1\bar{w}_3 + w_1w_2$ can be realized using Act 1 logic blocks (Act 1 logic block is shown). Note that there are no NOT gates in the chip; hence complements of signals have to be generated using the multiplexers in the logic block.



$f = \bar{w}_1[\bar{w}_2 + \bar{w}_3] + w_1[\bar{w}_2 + w_2]$

$= \bar{w}_1[\bar{w}_2(1+\bar{w}_3) + w_2(\bar{w}_3)] + w_1[1]$

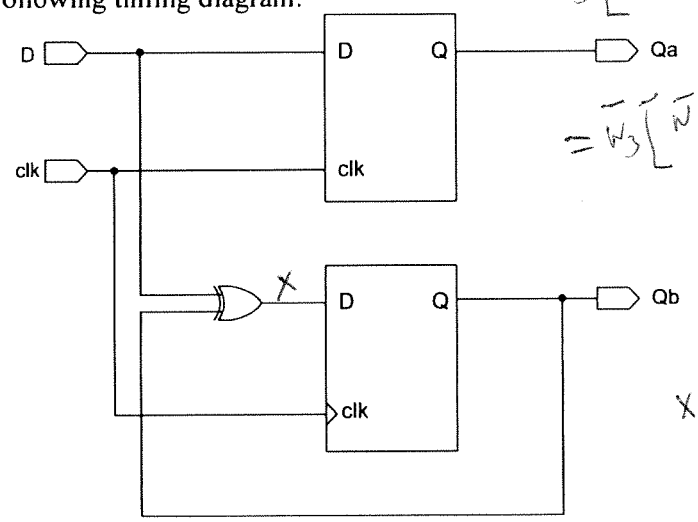
$= \bar{w}_1[\bar{w}_2(1) + w_2(\bar{w}_3)] + w_1[1]$

$f = \bar{w}_2\bar{w}_3 + \bar{w}_2w_3 + \bar{w}_1\bar{w}_3 + w_1w_2w_3 + w_1w_2w_3$

$= \bar{w}_3[\bar{w}_2 + \bar{w}_1 + w_1w_2] + w_3[\bar{w}_2 + w_1w_2]$

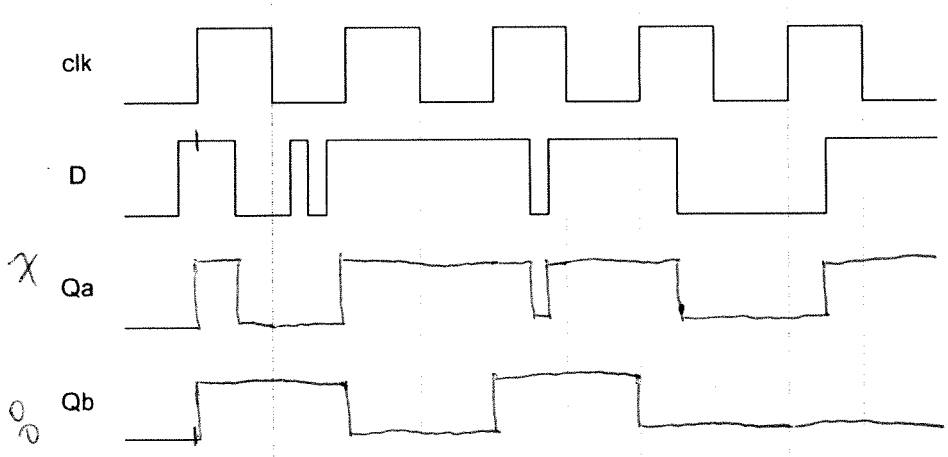
$= \bar{w}_3[\bar{w}_1(1+\bar{w}_2) + w_1(w_2+\bar{w}_2)] + w_3[\bar{w}_2(1) + w_2(w_1)]$

4. (15 points) Complete the following timing diagram.



$X = D \oplus Q_b$

$= D'Q_b + DQ_b'$



5. (15 points) Design a comparator logic circuit that compares two 4-bit binary numbers (A and B). This comparator logic only has 1-bit output (called `AltB`, A less than B). When A < B, `AltB = 1`. Otherwise, `AltB = 0`.

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