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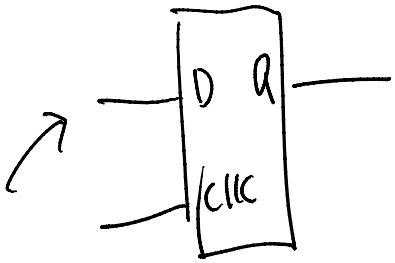
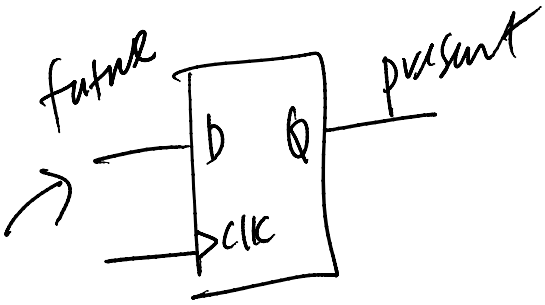
D-latch Vs D-flip-flop

level sensitive

edge sensitive





D latch

D flip-flop

CLK	D	Q(t+1)
0	X	Q(t)
1	0	0
1	1	1

CLK	D	Q(t+1)
↓	D	D
↑		
⌐		

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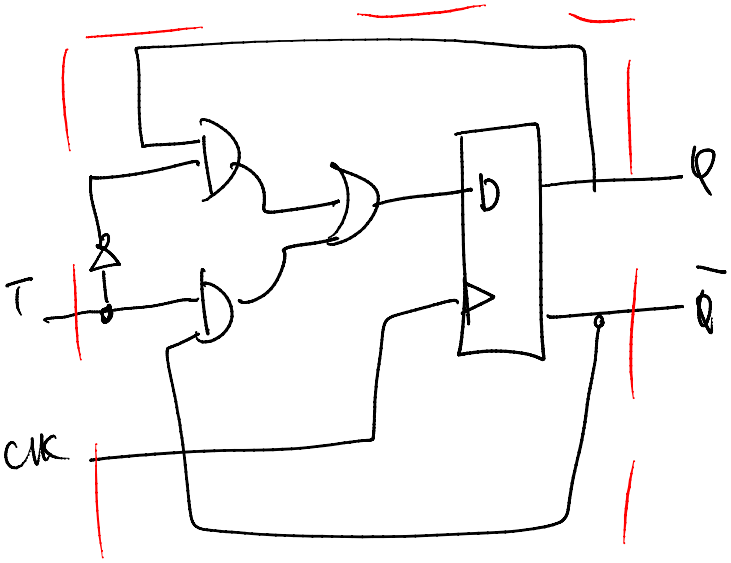
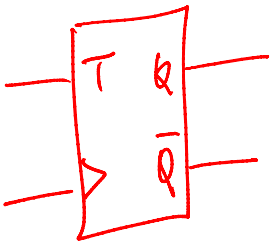
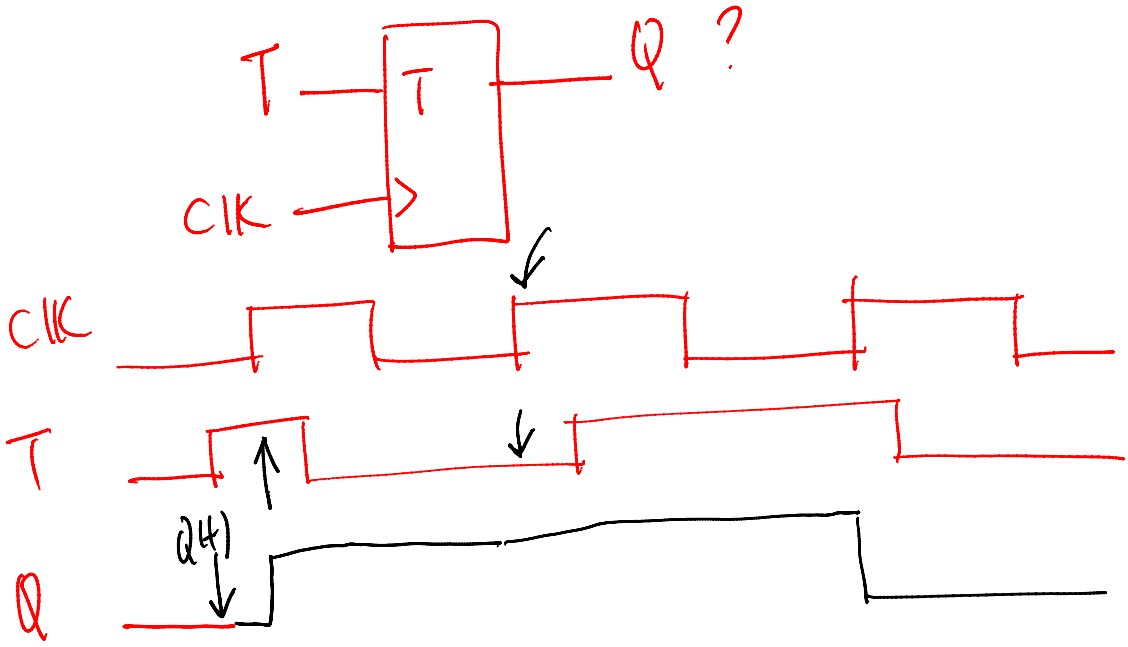
T -flip-flop



T	Q(t+1)
0	Q(t) ←
1	$\bar{Q}(t)$



T flip-flop



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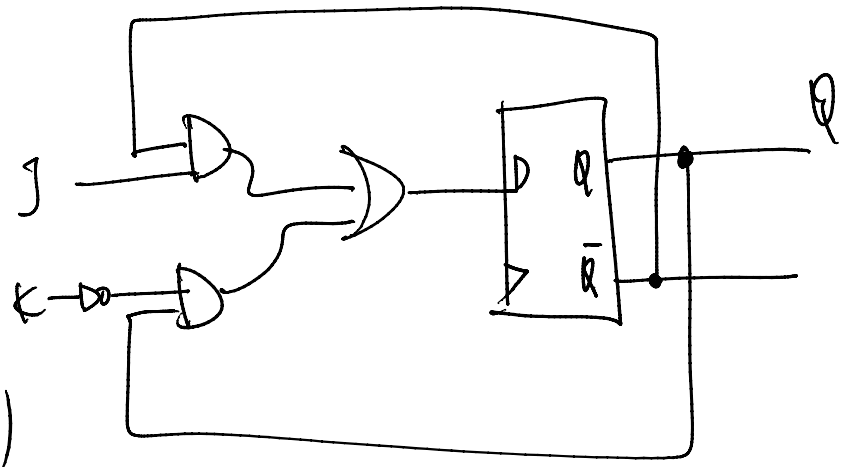
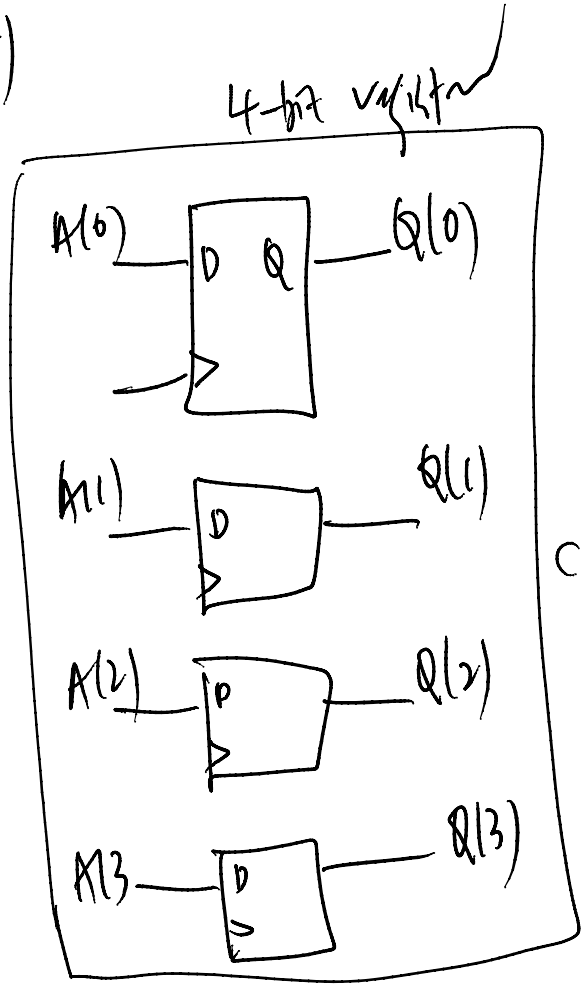
JK flip-flop

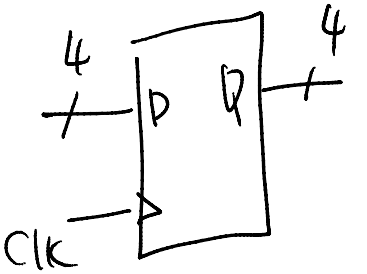


J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q̄(t)

D flip-flop



4-bit register



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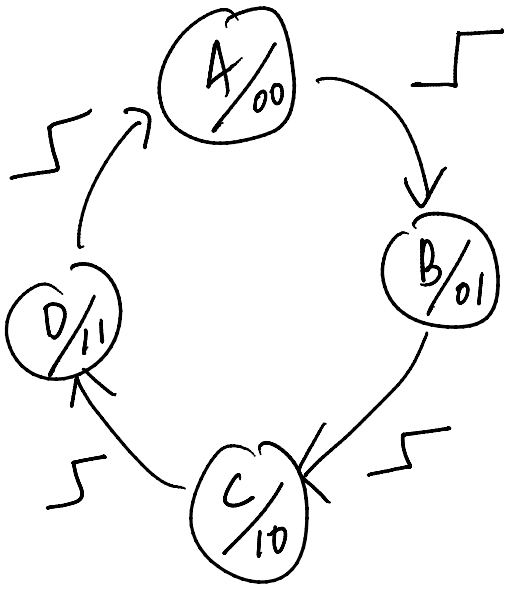
State diagram

design a 2-bit up counter

"11" wrap around "00"



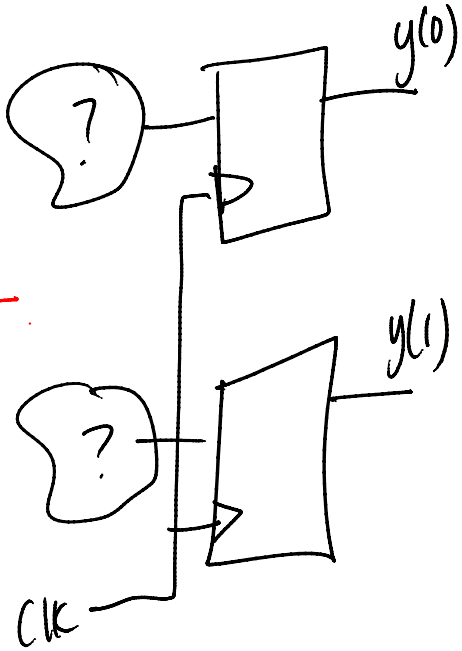
state table

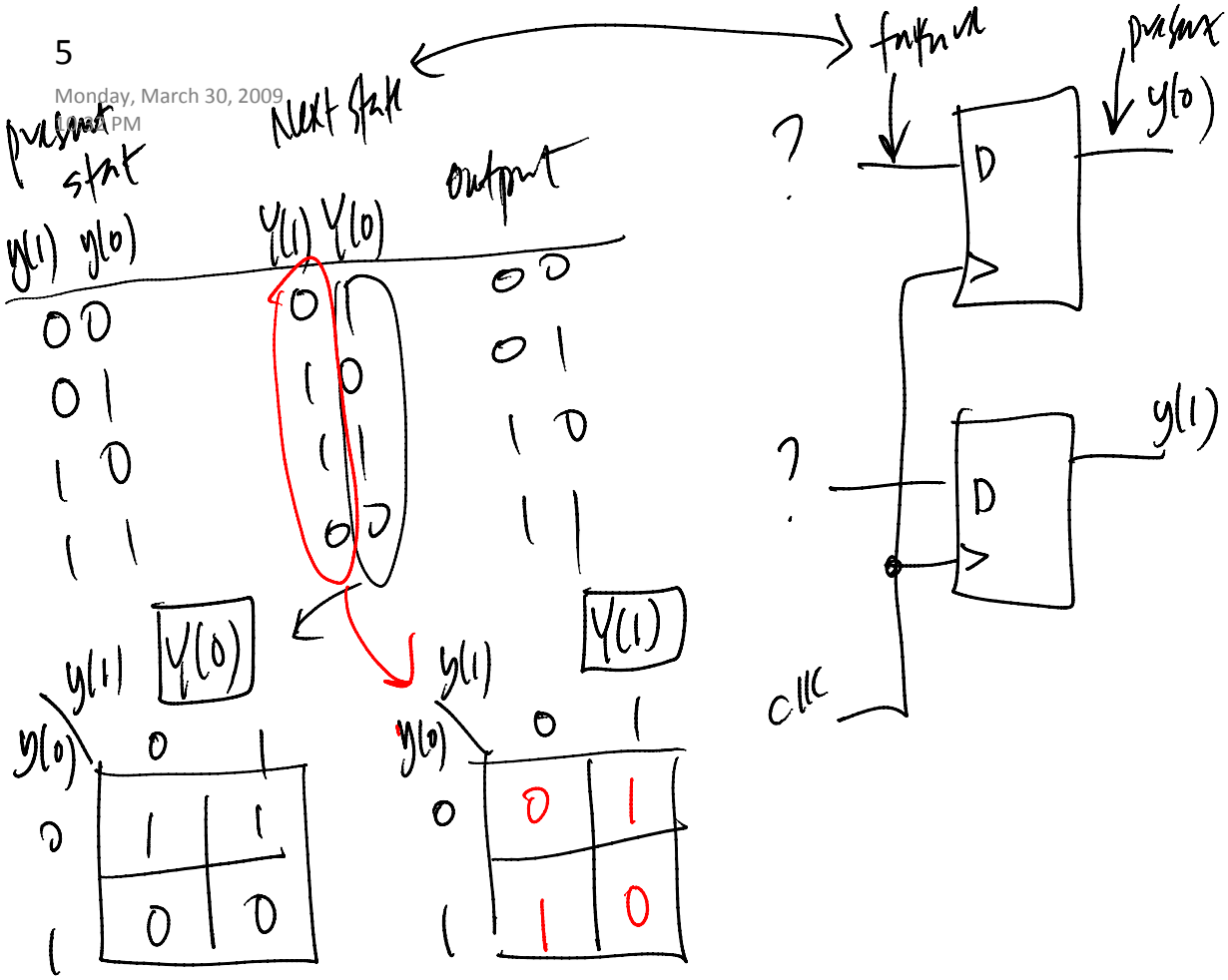
Present State	Next State	Output
A	B	00
B	C	01
C	D	10
D	A	11

A = "00" C = "10"

B = "01" D = "11"

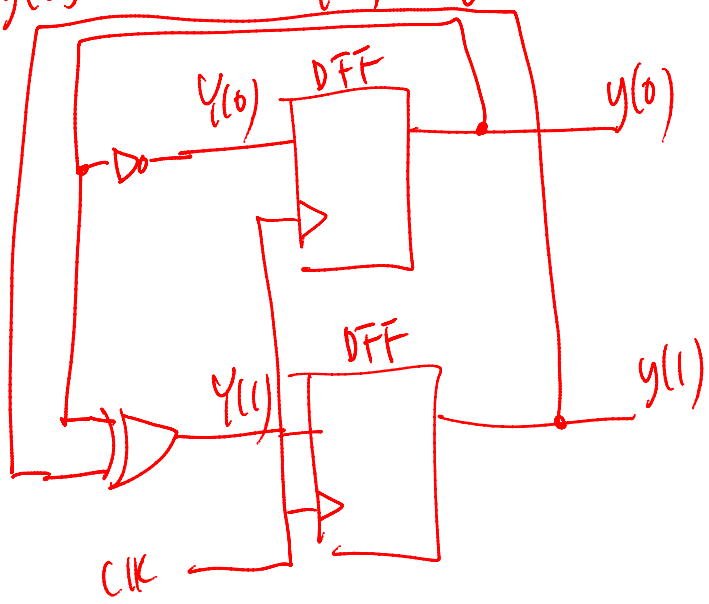
Present State	Next State	Output
00	01	00
01	10	01
10	11	10
11	00	11





$Y(0) = \overline{y(0)}$

$Y(1) = y(0) \oplus y(1)$



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