CMOS - Complementary

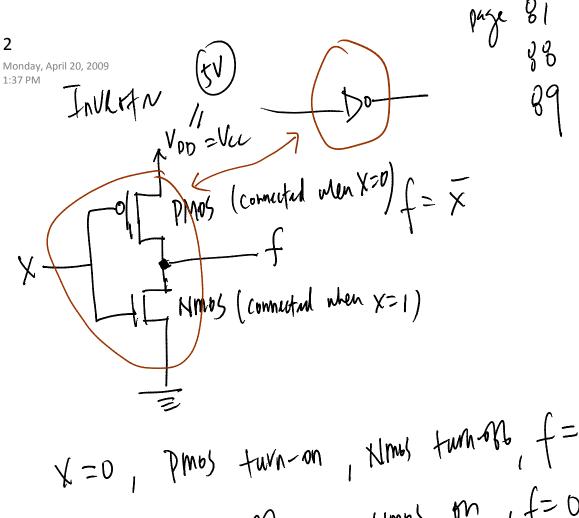
Metal atided Surivortation

NMbs

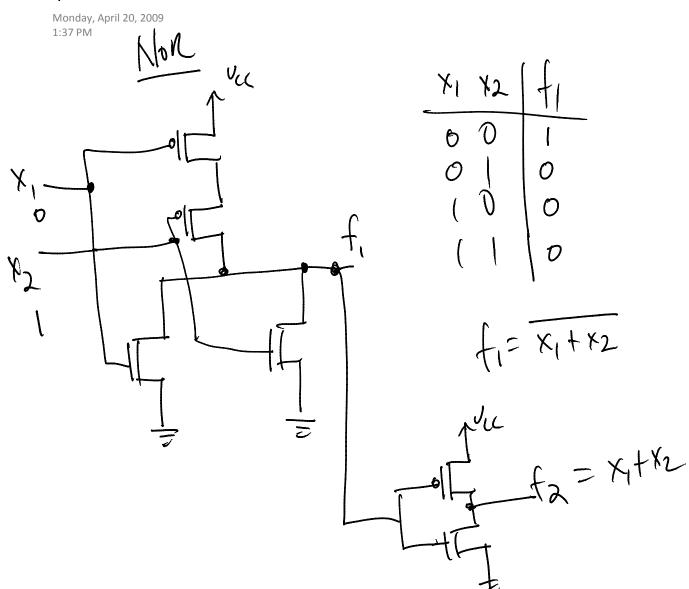
VG=1, A and B is

connected

PMOS VG=0, A and B is connected.



$$\chi=0$$
, Pmos turn-on, $\chi=0$, $\chi=1$, $\chi=0$, $\chi=1$, $\chi=0$, $\chi=1$, $\chi=0$, $\chi=1$,



110 no overlap 0 d% O dy Next X output 0 prenent ABC Ddd ට

Monday, April 20, 2009 1:38 PM

