SEMICONDUCTORS & IT HARDWARE

Samsung Memory Tech Day Takeaways

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We had the privilege of attending Samsung's Memory Day in San Jose, an invite-only event that showcased Samsung's technology roadmaps and vision to support AI workloads. Overcoming the "memory wall" will require the use of CXL, greater use of high-bandwidth memory (HBM), and new memory technologies such as LHM (low power, high bandwidth memory) and PIM (processing in memory). There is a battle brewing in HBM, and Samsung (NR) appears well positioned.

DRAM is the primary beneficiary of AI, supported by CXL memory pooling

Samsung and Microsoft both spoke about how we are in the early days of the AI revolution, which will drive significant demand for HBM and high-capacity DDR5 DRAM but only modest demand for SSDs and HDDs. CXL is aimed to address the "memory wall" or the widening gap between LLM computational needs and the memory infrastructure it relies on. Samsung noted that memory demand for AI/ML accelerators will grow at a 50%+ CAGR to reach 11% of total DRAM demand by 2028. Similarly, CXL should grow at a 275% CAGR from '24 to '28 to reach 11% of the DRAM market.

Here comes Samsung in HBM (High-bandwidth memory)

Hynix remains in the lead on HBM, which is used in compute accelerators and GPUs. Samsung is shipping HBM3 now and in quals with HBM3E. Samsung's HBM3E is on par with Micron's and above Hynix's. Samsung's HBM4 is very competitive supporting 48GB at 2.0TB/s bandwidth w/ 2.6pJ/bit.

DRAM roadmap indicates high-NA EUV in mid 2025

1-beta (12nm) is ramping today, and 1-c (11nm) could ramp in mid-2024. High-NA EUV patterning appears to ramp with 1-d in late '25/early '26. Samsung will introduce a 3D structure for sub-10nm DRAM capable of a 100Gb die, which may occur as HKMG transitions to FinFET for 0bnm (2029?).

NAND roadmap showcases wafer bonding in V10 (2026?)

V8 (238L 3D NAND) was Samsung's second node to use logic under the array; V9 will ramp mid '24, and V10 will use wafer bonding as Samsung takes a page from YMTC, Kioxia and WDC's play book.

Key valuation metrics

	Stock Rating	Price (LC)	TP / Upside		Mkt cap (USDm)	P/E (x) CY23e	P/E (x) CY24e	EV/EBITA (x) CY23e	EV/EBITA (x) CY24e	ESG Rating
AMD	(+)	100.0	150	50%	161,766	85.2	37.4	63.3	28.5	Average
Applied Mat.	(=)	134.2	140	4%	112,867	17.3	16.5	14.5	13.9	Leader
ASML	(+)	552.6	810	47%	230,423	28.5	27.9	24.2	23.3	Leader
Intel	(-)	33.9	28	-17%	141,324	NC	51.4	NC	52.3	Average
KLA	(=)	462.6	550	19%	62,165	20.6	20.2	16.9	16.5	Average
Lam Research	(=)	599.6	570	-5%	79,495	20.3	21.4	17.3	18.0	Average
Micron Tech.	(+)	66.9	75	12%	65,318	0.0	NC	NC	NC	
Nvidia	(+)	429.8	745	73%	1,059,212	44.1	26.6	37.7	21.4	Average
Seagate	(=)	65.3	58	-11%	13,624	NC	24.2	42.7	18.7	
Western Digital	(+)	41.8	58	39%	13,765	0.0	0.0	NC	37.4	

Prices at 23 October 2023

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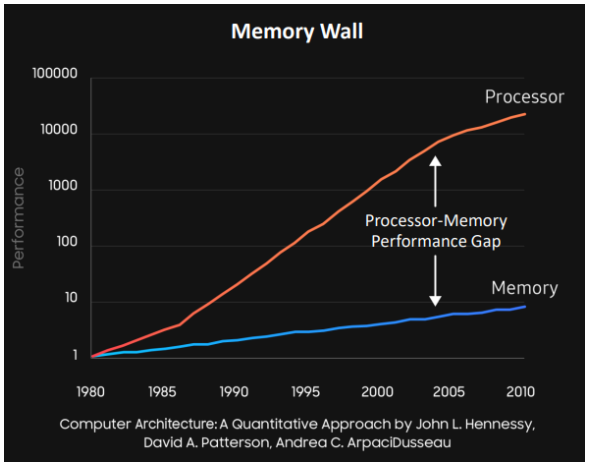
New DRAM technologies are being developed to support AI workloads

It is no surprise that inference and training workloads are memory intensive. As model parameters continue to grow at 10x a year and should exceed 1T parameters for GPT-4, AI accelerator performance is increasingly bottlenecked by the ability to store and retrieve training and inference data from memory. At the Open Compute Project Summit earlier last week, Microsoft highlighted how computational demand of transformer models has grown at 750x every 2 years while memory bandwidth has been just 1.6x/2yrs and interconnect bandwidth has been just 1.4x/2yrs.

This "memory wall" problem arises when processors must wait clock cycles to retrieve data from memory. Essentially, while the computing power of processors has advanced exponentially over the past 30 years as Moore's Law predicted, the performance of memory chips – although much faster than ever before – has advanced in a more linear way. This creates infrastructure scaling problems and underutilization of system resources.

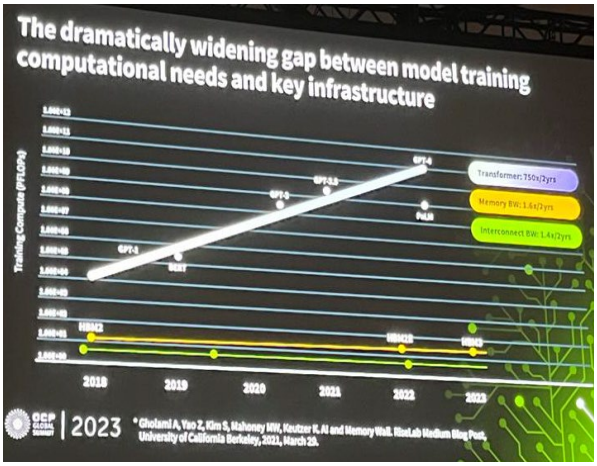
Figure 1: Model parameters of AI training systems are growing faster than improvements in infrastructure

Memory I/O has not been able to scale at the same rate as processor performance



Source: Samsung

AI models depend on advancements in networking, compute, and memory



Source: Open Compute Summit presentations

DRAM will be the primary beneficiary of AI/ML adoption

To overcome this "memory wall" problem, new forms of memory need to be developed. Samsung and Microsoft both spoke about how we are in the early days of the AI revolution, which will drive significant demand for high-bandwidth memory (HBM) and high-capacity DDR5 DRAM but only modest demand for SSDs and HDDs. This is relatively consistent with what semicap and memory IC providers have indicated earlier this year: an AI server is supposed to drive 8x higher DRAM content and 3x higher NAND content than a "traditional" server.

3D XPoint "died" in 2021 when Intel and Micron abandoned their efforts, which has left a gap between CPU cache (SRAM) and HBM. At the conference, Samsung introduced LHM, or low power high bandwidth memory. They also discussed upcoming HBM products such as PIM (process in-memory) and several products that support the CXL transport protocol.

LHM for AI Inferencing

Similar to Samsung's introduction of Wide IO in circa 2015, LHM offers high bandwidth and low-density cache memory. Essentially, the first chip on LHM (in 2026?) will run at the same speed of Samsung's HBM3 (820GB/s) but will be just 2GB in size (vs. 16GB) and can run at only 1.4 picojoule (pJ/Bit) that's roughly 4x lower power than HBM!

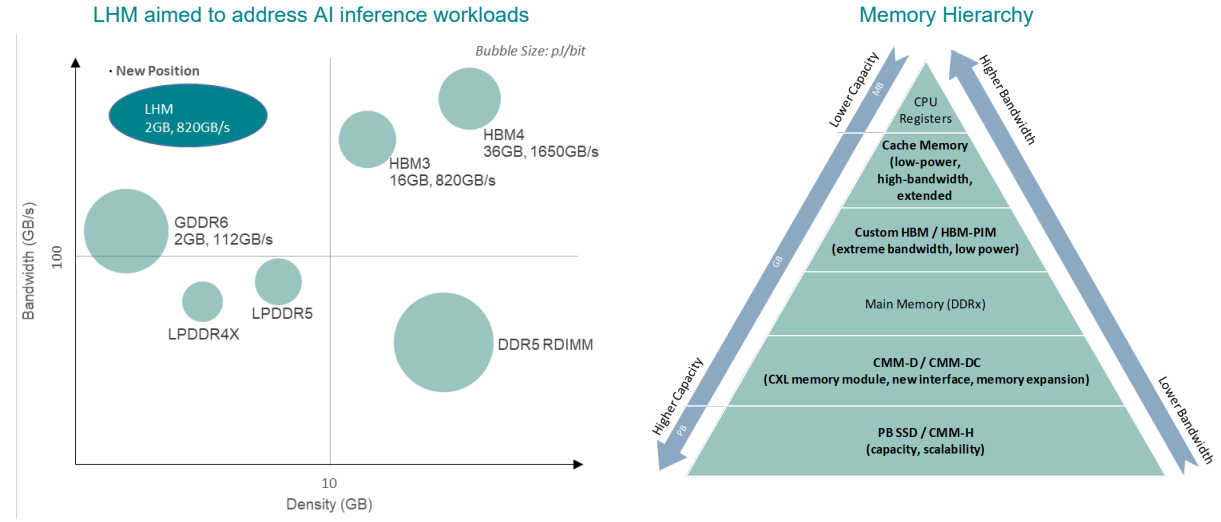
Samsung will be able to achieve this using hybrid bonded and 2.5D packaging technology. In other words, LHM is being pitched for AI inference given its low power and higher bandwidth capabilities vs. GDDR and LPDDR DRAM offerings.

PIM (Processing In Memory) for AI applications

Samsung also discussed the use of PIM in its future DRAM roadmap. The idea is that the IO counts and thermal constraints are becoming a limitation for higher memory bandwidth of AI applications. PIM overcomes these constraints by calculating target operations in parallel inside DRAM. This results in improved energy efficiency and higher bandwidth since the AI processor will receive only final data from the LPDDR DIMM or HBM-PIM rather than sending all data to the processor host for AI model calculations. Samsung indicated that LPDDR-PIM could be commercialized in 2026.

Similarly, Samsung noted that the use of HBM-PIM can drive a 2.25x increase in energy efficiency and 2.3x gain in bandwidth over "regular" HBM. This technology is expected to be commercialized in 2027.

Figure 2: New forms of memory needed to address the "memory wall"



Source: BNP Paribas Exane estimates

Understanding the need for CXL

CXL will add another tier in the memory hierarchy below the main system memory (DRAM found in a server) to address growing demand for different tiers of memory capacity and bandwidth. CXL is needed to support the planned increase in I/O traffic by adding DRAM capacity and bandwidth data-intensive, high performance computing applications.

Samsung's CXL solutions have a naming convention of "CMM" or CXL Memory Modules. Samsung believes CMM can be used for capacity expansion, bandwidth expansion, tiered memory, and memory pooling/sharing for in-memory databases, HPC, AI training and inference, and general purpose virtualization applications.

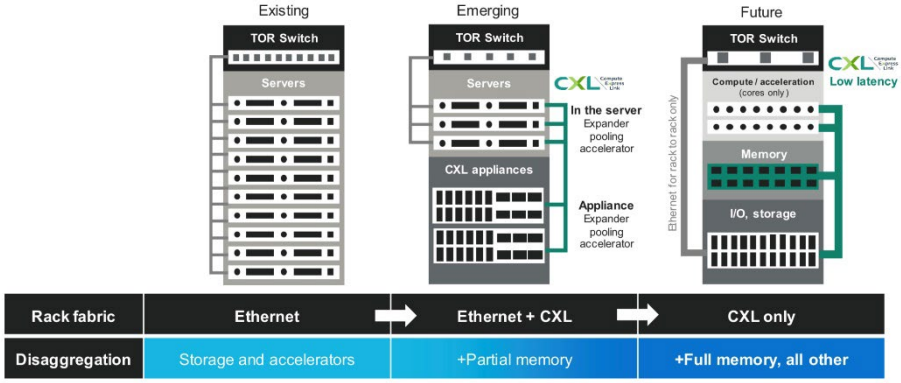
Compute express link (CXL) allows low-latency high-bandwidth interconnects

Compute Express Link (CXL) is a new open standard communication design based on PCIe PHY that allows low-latency and high-bandwidth interconnects between CPUs, GPUs, FPGAs, and other devices. It enables devices to share memory and cache resources directly with each other and eliminates the need for data to be transferred over the interconnect.

CXL 1.0 was first introduced in 2019 and upgraded to CXL 2.0 in 2020, both based on PCIe 5.0 physical layers. The latest version CXL 3.0 was released in Aug 2022 and is based on PCIe 6.0 PHY and PAM-4 coding, supporting up to 128GB/s bi-directional communication over a 16-lane link. It's worth noting that most products out today by vendors are for CXL 1.0 and 2.0 and that product supporting CXL 3.0 will likely not be out until PCIe 6.0 in 2026.

AI and HPC will drive the need for higher-performance accelerators and low-latency memory solutions, and it will be the test bed for CXL solutions. What's interesting to us is that the CXL technology could potentially allow multiple devices to coherently share memory spaces and make it possible to create a scalable disaggregate memory pool for GPU devices. This could essentially change the architecture of integrated system designs and significantly improve the efficiency of processing workloads.

Figure 3: CXL allows the creation of a disaggregate memory pool



Source: Marvell

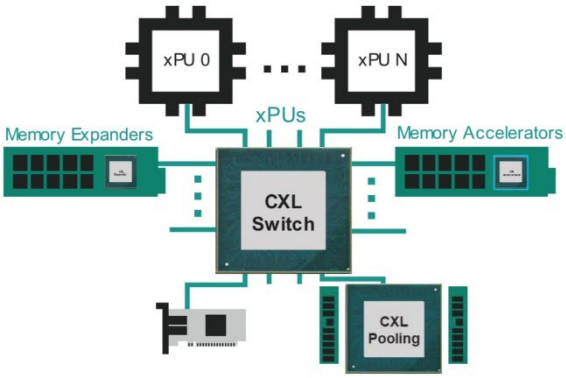
The implementation of CXL is still at very early stage, but the industry has coalesced to push for the next generation interconnects. The CXL Consortium was formed with all major technology companies, including AMD, Broadcom, Cisco, Google, Intel, Marvell Meta, Microsoft, Micron, Samsung, SK Hynix, Nvidia, Western Digital and many others.

In 2021, CXL 1.1 support was announced for the latest Intel Sapphire Rapids and AMD Zen 4 EPYC Genoa and Bergamo CPUs, and deployments have already occurred in 2023. Micron anticipates CXL 2.0 will be rolled out in late 2024, and the market will accelerate further when CXL 3.0 rolls out afterwards – perhaps late 2025/early 2026 – which enables memory pooling.

At Samsung's Memory Tech Day, the company noted that memory demand for AI/ML accelerators will grow at a 50%+ CAGR to reach 11% of total DRAM demand by 2028. Similarly, CXL should grow at a 275% CAGR from '24 to '28 to reach 11% of the DRAM market. At Micron's last analyst day, the company suggested CXL could exceed $20B+ by 2030.

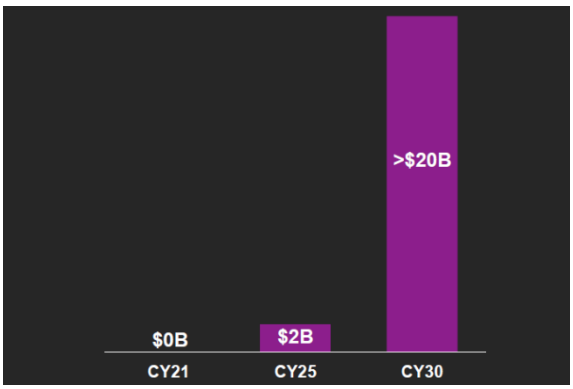
Figure 4: CXL is the next generation of interconnects

CXL allows cache-coherent interconnects across device memory



Source: Marvell

CXL TAM could grow to over $20B by 2030



Source: Micron

DRAM Roadmap

We believe Samsung will remain the #1 provider of DRAM globally, and we think Samsung is making good progress on 1-beta (12nm) node today. We estimate that Samsung could be shipping 1-c (11nm) in mid-2024. We think that High-NA EUV patterning should ramp with 1-d in late '25/early '26. In our view, the use of high-NA and no mention of 3D DRAM on the roadmap should be viewed positively for ASML.

Figure 5: Our estimate of Samsung's DRAM roadmap

	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Tech node	2znm		1xnm		1ynm		1znm		1anm	1bnm		1cnm	1dnm		0anm	0dnm	
Capacity Speed	8Gb		2.4Gbps	2.6Gbps			3.2Gbps		4.8Gbps	24Gb 6.4Gbps	32Gb	7.2Gbps	9.6Gbps		48Gb 10.8Gbps		
Products	DDR4		LPDDR4x		GDDR6 HBM2		DDR5 LPDDR5 HBM2E			LPDDR5x GDDR6+ HBM3	GDDR7 HBM3E CXL-MXP	HBM3-PIM AX DIMM	HBM4	CXL-PNM	DDR6		
Patterning	Double Patterning		Quadruple Patterning				EUV					Advanced EUV					

Source: BNP Paribas Exane estimates

New sever server platforms from Intel and AMD support more memory channels and DIMM slots per server CPU. The largest benefit of Sapphire Rapids launching will be the support of DDR5 DRAM, PCIe 5.0 SSDs, CXL 1.1, and up to 64GB of HMB2.

Figure 6: Our estimate of Samsung's DDR5 Roadmap

		2022	2023	2024	2025	2026	2027	2028
Compute Needs	x86 CPU Core	40 - 64 cores	56 - 128 cores		128 - 192 cores		192+ cores	
	CPU Mem. Ch.	8 Channels	8/12/16 Channels				12/16 Channels	
	CPU TDP (max.)	280W	350W+		400W+		Beyond	
	Rack Power (Volume.)	4.4 - 8.8 kW	8.8 - 15+ kW					
	DIMM Config	2SPC /	1SPC or mixed 1&2SPC / 7+mm				1SPC	
System Requirement & DRAM Solution	Process	1anm		1bnm	1cnm	1dnm	0anm	
	DRAM Generation	DDR5					DDR6 (TBD)	
	Bandwidth	4800Mbps	5600Mbps	6400Mbps	7200/8000Mbps	8000Mbps+	9600Mbps+	TBD
	Capacity comp.	16/24Gb		16/24/32Gb				
	Capacity DIMM	Max. 512GB		Max 1TB				

Source: BNP Paribas Exane estimates

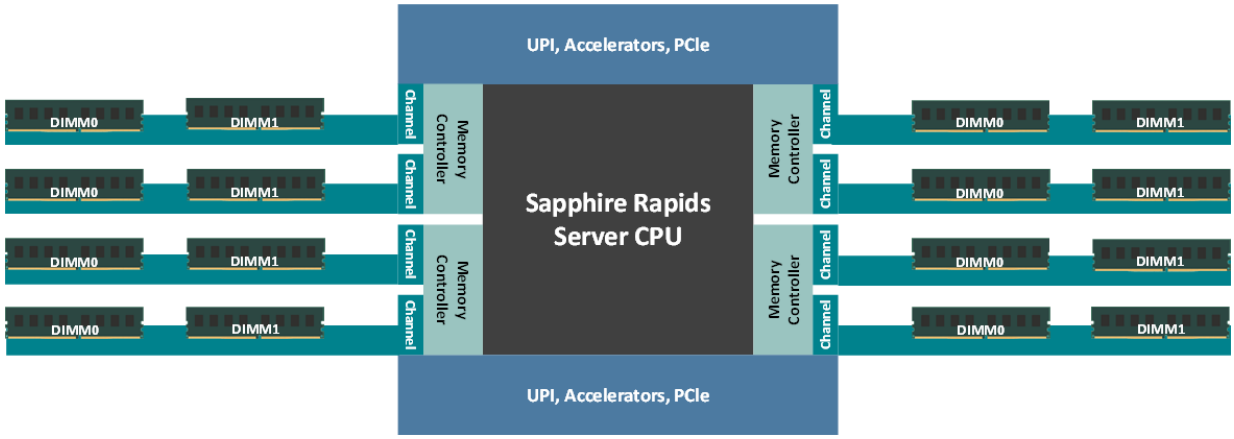
Understanding The Benefits Of DDR5

Historically, server system performance has been bottlenecked by different components of the system architecture. Over the last decade, MPU vendors have increased overall processing performance via process node transitions, enhanced instruction set architecture (ISA) compilation, and utilization of multi-core architectures. The problem, though, is that there is a widening gap between the performance of CPU cores and the DRAM DIMMs ("dual in-line memory modules", the primary form factor for server memory) that 'feed' and transport data to them each clock cycle. Much of this can be explained by DRAM core clock rates falling behind improvements in CPU core clock rates. This creates infrastructure scaling problems and underutilization of system resources.

There are two ways to remedy system performance gated by memory: increase the total system memory capacity via volume, and/or increase the transmission speed via bandwidth of the memory itself commensurate with the processor it supports. The former is done by optimally allocating server DRAM DIMMs across a server's memory channels. Increasing the bandwidth is done by upgrading the clock speed of the DRAM, such as increasing from DDR4 (3.2Gb/s) to DDR5 (initial speed of 4.8Gb/s with a path to 6.4Gb/s). Thus, DDR5 provides 50% better performance out of the gate with capacity to run at twice the effective bandwidth of DDR4. Of course, DDR5 offers reduced power consumption vs. DDR4 making it more suitable for all applications as a system's main memory configuration.

DRAM speeds and densities should continue to expand as memory requirements in servers grow to help serve a growing number of CPU cores. Higher compute capacity and bandwidth arises from user-generated content of video (Youtube, Netflix), gaming, big data analytics, high performance computing and virtualization. Similarly, future server platforms such as INTC's Granite Rapids (3nm) will support even more DIMM channels (12 vs. 8). Combined, improved DRAM speed and capacity per server will allow DRAM to continue to grow within server architectures and provide Micron, Samsung and Hynix ample opportunity to grow over the next few years.

Figure 7: Server DRAM "Feeds" The CPU

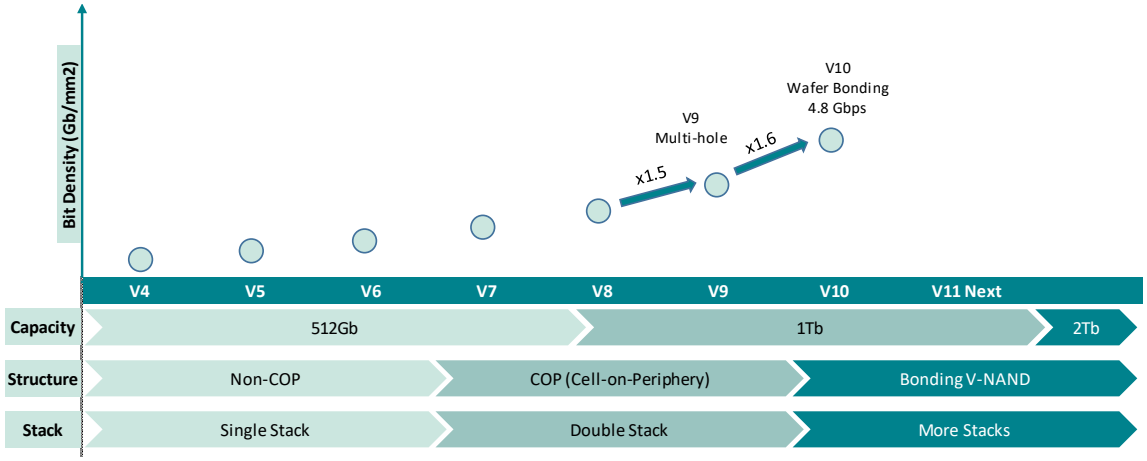


Source: BNP Paribas Exane

NAND Roadmap

Samsung's V7 node, or its 176-layer 3D NAND die, was Samsung's first node to use logic under the array. Samsung's 238L die (V8) continues to drive bit density, though the use of multi-hole technology in the upcoming V9 node is expected to drive a 50% improvement in bit density. For V10, we expect Samsung to introduce wafer bonding that will drive another 60% improvement in bit density vs. V9. YMTC, Kioxia and WDC have all since adopted wafer bonding to drive improvements in bit density and cost across their NAND roadmaps.

Figure 8: Our estimate of Samsung's NAND roadmap



Source: BNP Paribas Exane estimates

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