	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	ΧA	хB	хC	хD	хE	хF
	RLC B	RLC C	RLC D	RLC E	RLC H	RLC L	RLC (HL)	RLC A	RRC B	RRC C	RRC D	RRC E	RRC H	RRC L	RRC (HL)	RRC A
0x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z Ø Ø C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z Ø Ø C	Z Ø Ø C	Z 0 0 C	Z Ø Ø C	Z 0 0 C	Z 0 0 C
	RL B	RL C	RL D	RL E	RL H	RL L	RL (HL)	RL A	RR B	RR C	RR D	RR E	RR H	RR L	RR (HL)	RR A
1x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C	Z 0 0 C
	SLA B	SLA C	SLA D	SLA E	SLA H	SLA L	SLA (HL)	SLA A	SRA B	SRA C	SRA D	SRA E	SRA H	SRA L	SRA (HL)	SRA A
2x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
-^	z ø ø c	z o o c	z ø ø c	z o o c	zøøc	zooc	Z 0 0 C	z o o c	z 0 0 0	Z 0 0 0	Z 0 0 0	Z 0 0 0	Z 0 0 0	z 0 0 0	Z 0 0 0	Z 0 0 0
	SWAP B	SWAP C	SWAP D	SWAP E	SWAP H	SWAP L	SWAP (HL)	SWAP A	SRL B	SRL C	SRL D	SRL E	SRL H	SRL L	SRL (HL)	SRL A
3.4	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
J ^	Z 0 0 0	Z 0 0 0	Z 0 0 0	Z 0 0 0	Z 0 0 0	z 0 0 0	Z 0 0 0	Z 0 0 0	z o o c	z o o c	z 0 0 c	z o o c	Z 0 0 C	zooc	Z O O C	z o o c
	BIT 0,B	BIT 0,C	BIT Ø,D	BIT 0,E	BIT 0,H	BIT 0,L	BIT 0,(HL)	BIT 0,A	BIT 1,B	BIT 1,C	BIT 1,D	BIT 1,E	BIT 1,H	BIT 1,L	BIT 1,(HL)	BIT 1,A
4x	2 8	2 8	2 8	2 8	2 0	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 0	2 8	2 16	2 8
7^	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -
5x	BIT 2,B	BIT 2,C 2 8	BIT 2,D 2 8	BIT 2,E 2 8	BIT 2,H	BIT 2,L 2 8	BIT 2,(HL) 2 16	BIT 2,A 2 8	BIT 3,B 2 8	BIT 3,C 2 8	BIT 3,D 2 8	BIT 3,E 2 8	BIT 3,H 2 8	BIT 3,L 2 8	BIT 3,(HL) 2 16	BIT 3,A 2 8
ox	28				7 0 1											
	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -
6	BIT 4,B	BIT 4,C	BIT 4,D	BIT 4,E	BIT 4,H	BIT 4,L	BIT 4,(HL)	BIT 4,A	BIT 5,B	BIT 5,C	BIT 5,D	BIT 5,E	BIT 5,H	BIT 5,L	BIT 5,(HL)	BIT 5,A
ox	2 0 7 0 1	2 ŏ	28	2 8	7 0 1	7 0 1	2 16	2 8	2 8	2 8	7 0 1	2 8	2 8	2 8	2 16	2 8
	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -
7x	BIT 6,B	BIT 6,C	BIT 6,D	BIT 6,E	BIT 6,H	BIT 6,L	BIT 6,(HL)	BIT 6,A	BIT 7,B	BIT 7,C	BIT 7,D	BIT 7,E	BIT 7,H	BIT 7,L	BIT 7,(HL)	BIT 7,A
/x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -	Z 0 1 -
	RES 0,B	RES 0,C	RES Ø,D	RES 0,E	RES 0,H	RES 0,L	RES 0,(HL)	RES 0,A	RES 1,B	RES 1,C	RES 1,D	RES 1,E	RES 1,H	RES 1,L	RES 1,(HL)	RES 1,A
8x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
0	RES 2,B	RES 2,C	RES 2,D	RES 2,E	RES 2,H	RES 2,L	RES 2,(HL)	RES 2,A	RES 3,B	RES 3,C	RES 3,D	RES 3,E	RES 3,H	RES 3,L	RES 3,(HL)	RES 3,A
9x	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	RES 4,B	RES 4,C	RES 4,D	RES 4,E	RES 4,H	RES 4,L	RES 4,(HL)	RES 4,A	RES 5,B	RES 5,C	RES 5,D	RES 5,E	RES 5,H	RES 5,L	RES 5,(HL)	RES 5,A
AX	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
D	RES 6,B	RES 6,C	RES 6,D	RES 6,E	RES 6,H	RES 6,L	RES 6,(HL)	RES 6,A	RES 7,B	RES 7,C	RES 7,D	RES 7,E	RES 7,H	RES 7,L	RES 7,(HL)	RES 7,A
Bx	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
						CET O I										
	SET 0,B	SET 0,C	SET 0,D	SET 0,E	SET 0,H	SET 0,L	SET 0,(HL)	SET 0,A	SET 1,B	SET 1,C	SET 1,D	SET 1,E	SET 1,H	SET 1,L	SET 1,(HL)	SET 1,A
Cx	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	CET 2 C				CET 2 "	CET 2 :	CET 2 (111)			CET 2.6		CET 3 5		CET 2 :		CET 2 4
D.,	SET 2,B	SET 2,C	SET 2,D	SET 2,E	SET 2,H	SET 2,L	SET 2,(HL)	SET 2,A	SET 3,B	SET 3,C	SET 3,D	SET 3,E	SET 3,H	SET 3,L	SET 3,(HL)	SET 3,A
Dx	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	CFT 4.0				CET 4 ''	CET 4	CET 4 (111 )			CET 5 C			CET 5 ''	CET 5 :		CET 5 A
F.,	SET 4,B	SET 4,C	SET 4,D	SET 4,E	SET 4,H	SET 4,L	SET 4,(HL)	SET 4,A	SET 5,B	SET 5,C	SET 5,D	SET 5,E	SET 5,H	SET 5,L	SET 5,(HL)	SET 5,A
Ex	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8
	SET 6,B	SET 6,C	SET 6,D	SET 6,E	SET 6,H	SET 6,L	SET 6,(HL)	SET 6,A	SET 7,B	SET 7,C	SET 7,D	SET 7,E	SET 7,H	SET 7,L	SET 7,(HL)	SET 7,A
FX	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8	2 8	2 8	2 8	2 8	2 8	2 8	2 16	2 8

	x0	x1	
	NOP	LD BC,d16	LD (
0 x	1 4	3 12	1
	STOP 0	LD DE,d16	LD
1 v	2 4	3 12	1

```
0×00 ⇒ 1,
0×01 ⇒ {
    let value = self.memory.read_word(self.registers.pc);
    self.registers.pc = self.registers.pc.wrapping_add(2);
    cpu.registers.b = (value >> 8) as u8;
    cpu.registers.c = (value & 0×00FF) as u8;
3
}
```