

RAPIDO 2025: Workshop on Rapid Simulation and Performance Evaluation for Design Optimization: Methods and Tools

- Workshop of HiPEAC Conference
- **Barcelona, Spain, January 21, 2025**

17th Workshop on Rapid Simulation and Performance Evaluation for Design Optimization: Methods and Tools - in Barcelona, Spain, 21th January 2025

Held in conjunction with the HiPEAC Conference (<https://www.hipeac.net/2025/barcelona/#/>)

!!! Accepted papers will be published in the ACM digital library !!!

Goal of the Workshop

The focus of the RAPIDO workshop is on methods and tools for rapid simulation and performance evaluation in embedded and high-performance system design. Considering continuous advances in chip design technology, it is expected that future-generation systems on chip will integrate numerous units on a single die, including multiple (heterogeneous) processor cores, multiple levels of (shared/private) caches or memories, and dedicated accelerators (in particular for AI), which will be glued together through a network on-chip (NoC). The design space is huge though and several design metrics should be considered as well for selecting the optimal system configuration. Despite several years of research, the early stage of design phase still requires to be supported by innovative design methodologies and tools for simulation, exploration and performance evaluation. RAPIDO seeks for original research papers that face this challenge for high performance embedded computing systems, in particular for system supporting Artificial Intelligence or using Artificial Intelligence based techniques for design space explorations and to satisfy design constraints (performance, power, security, etc).

Topics of Interest include, but are not limited to

- Rapid simulation techniques especially for new architectures: Multicores, 3D Architectures, FPGA and GPU based heterogeneous Multicores/MPSoC, ...
- Variability, reliability and power/energy consumption in simulation techniques.
- High-level modeling and simulation techniques, Transactional Level Modeling (TLM), Analytical Modeling, Trace-Driven Simulation, ...
- Rapid design space exploration (DSE) for heterogeneous and embedded systems.
- Dynamic binary translation for fast simulation and DSE.
- Verification and validation through simulation methods and tools.
- Simulation of complex systems, artificial intelligence, system of systems, ...
- Digital Twin simulations.
- Methods and tools for quantum computing simulation.
- Experience reports using existing simulators.

Submission Guidelines

- **Important dates:**
 - **Abstract Submission deadline: Oct 27th, 2024**
 - **Paper submission deadline: Nov 3rd, 2024**
 - Notification to authors: Dec 15th, 2024
 - Final version of accepted papers: Jan 10th, 2025
- All papers must be original and not simultaneously submitted to another journal or conference.
- Electronic paper submission requires a full paper, up to 6 double-column ACM format pages, including figures and references. Up to 2 extra-pages can be requested for free to the organizing committee (gianluca dot palermo at polimi dot it). Please use the following template when preparing your manuscript: <http://www.acm.org/sigs/publications/proceedings-templates>
- The paper submission will be conducted using the EasyChair conference manager. Papers should be submitted in PDF format on web site <https://easychair.org/conferences/?conf=rapido2025>
- *Accepted papers will be published in the ACM digital library.*

Organizing Committees

- | | |
|---|--|
| • Gianluca Palermo, Politecnico di Milano | • Morteza Biglari-Abhari, University of Auckland |
| • Reda Nouacer, CEA Saclay | • Matthias Jung, University of Würzburg, Fraunhofer IESE |
| • Daniel Chillet, University of Rennes, Irisa/inria | • Lilia Zaourar, CEA Saclay |
| • Daniel Gracia Pérez, Research and Technology | |