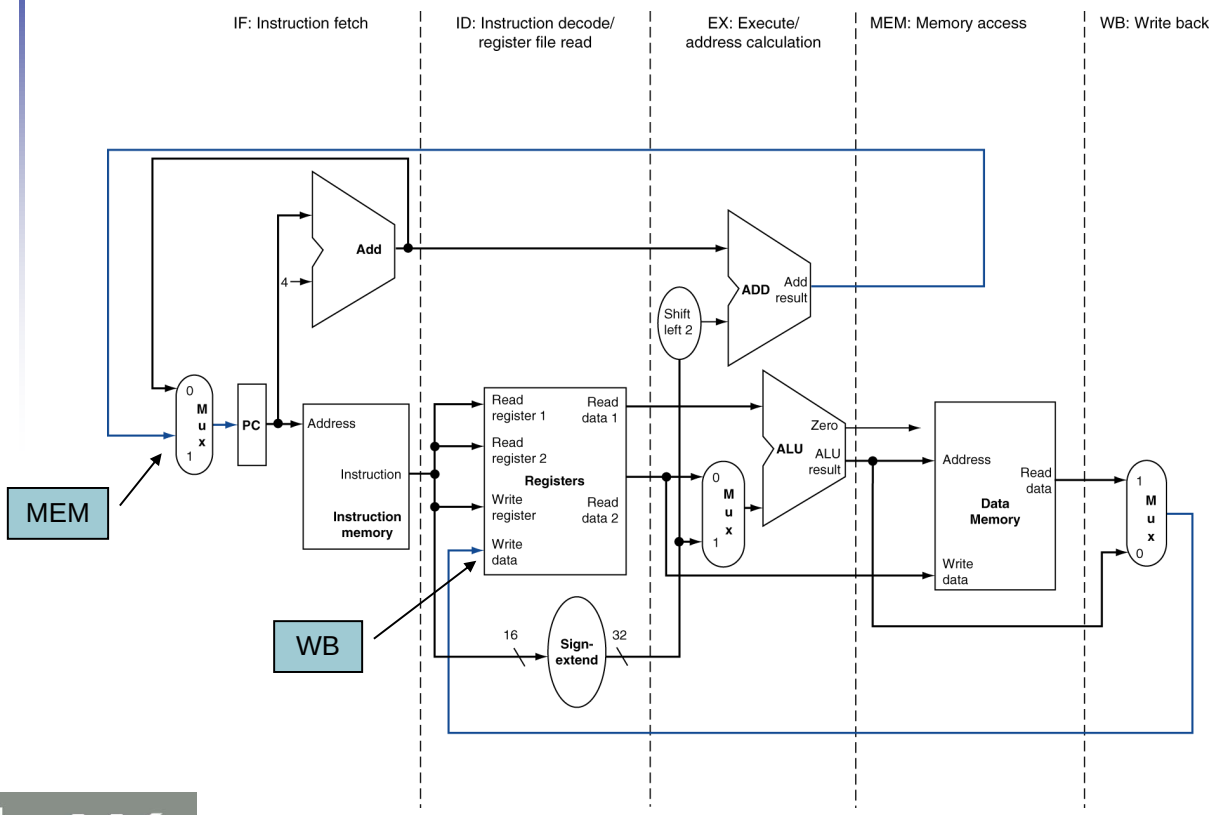
# Arquitetura de um processador

## 4. Pipeline: caminho de dados e controle

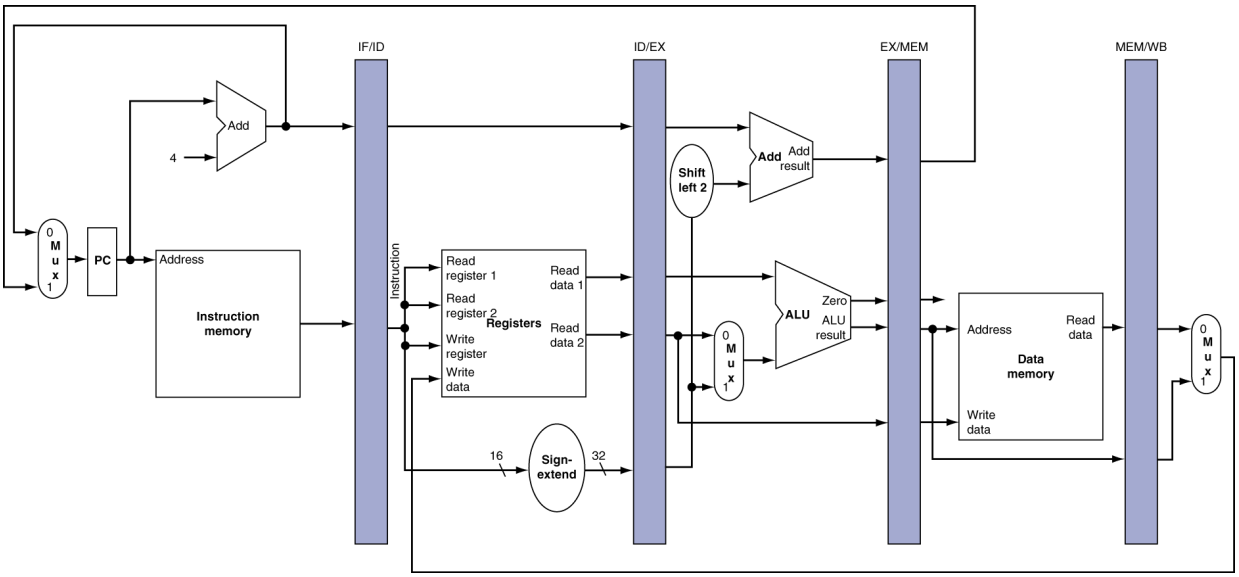
Prof. John L. Gardenghi
*Adaptado dos slides do livro*

## Caminho de dados com pipeline



# Registradores pipeline

- Há registradores entre os estados
  - Armazenam a informação do ciclo anterior

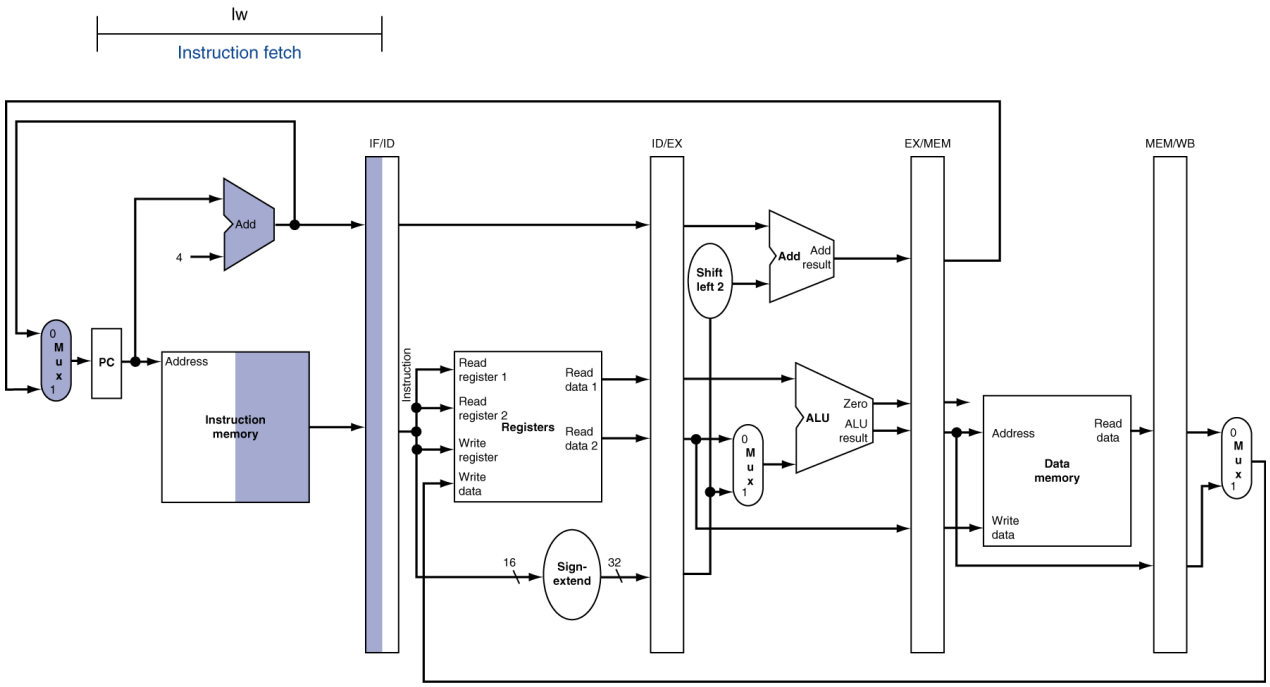





# Representação gráfica do pipeline

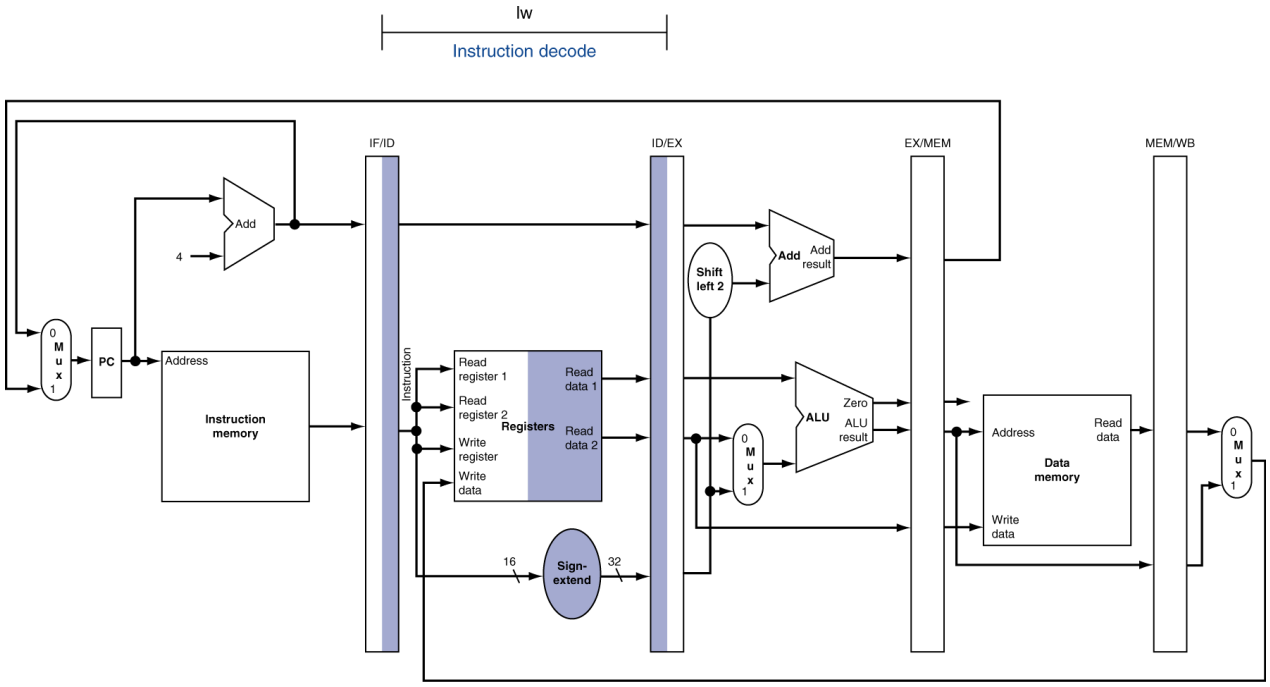
- Fluxo de uma instrução por ciclo de clock através do caminho de dados pipeline
  - Diagrama de pipeline “Single-clock-cycle”
    - Mostra o uso do pipeline num único ciclo de clock
    - Destaca os recursos utilizados
  - Diagrama “multi-clock-cycle”
    - Gráfico da operação através do tempo (com as fases do pipeline)
- Próximos slides: diagramas “single-clock-cycle” para load & store

# IF para Load, Store, …

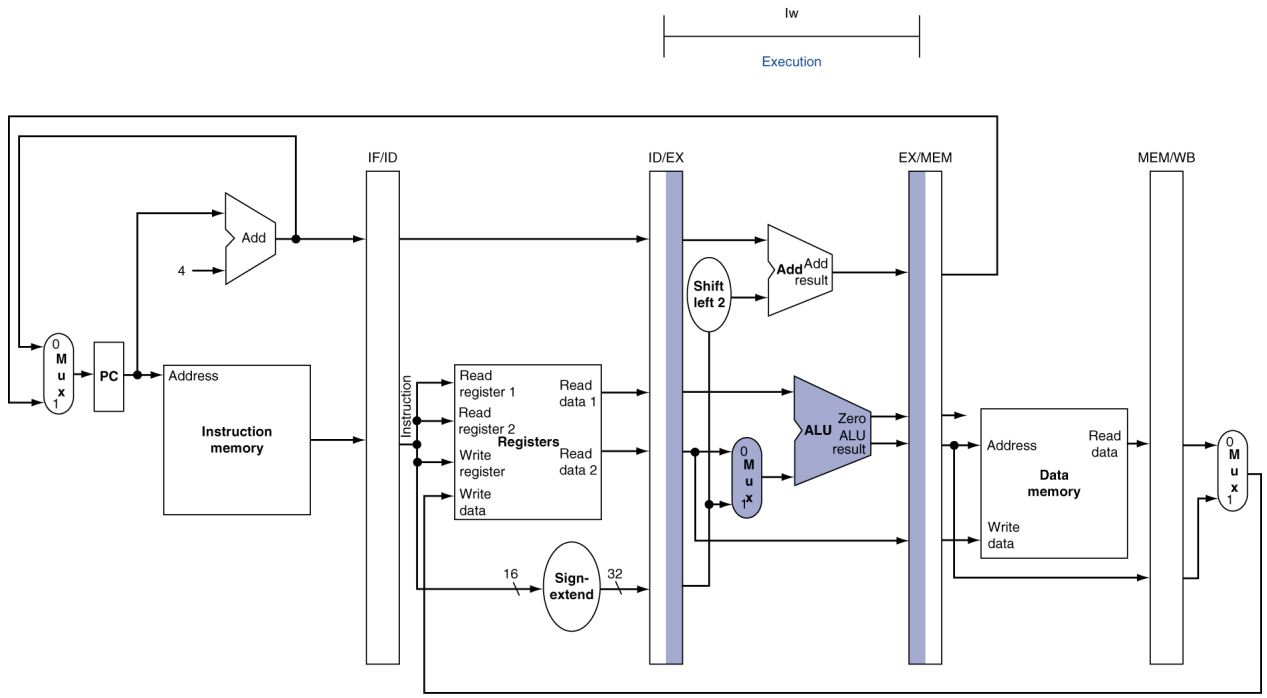





# ID para Load, Store, …

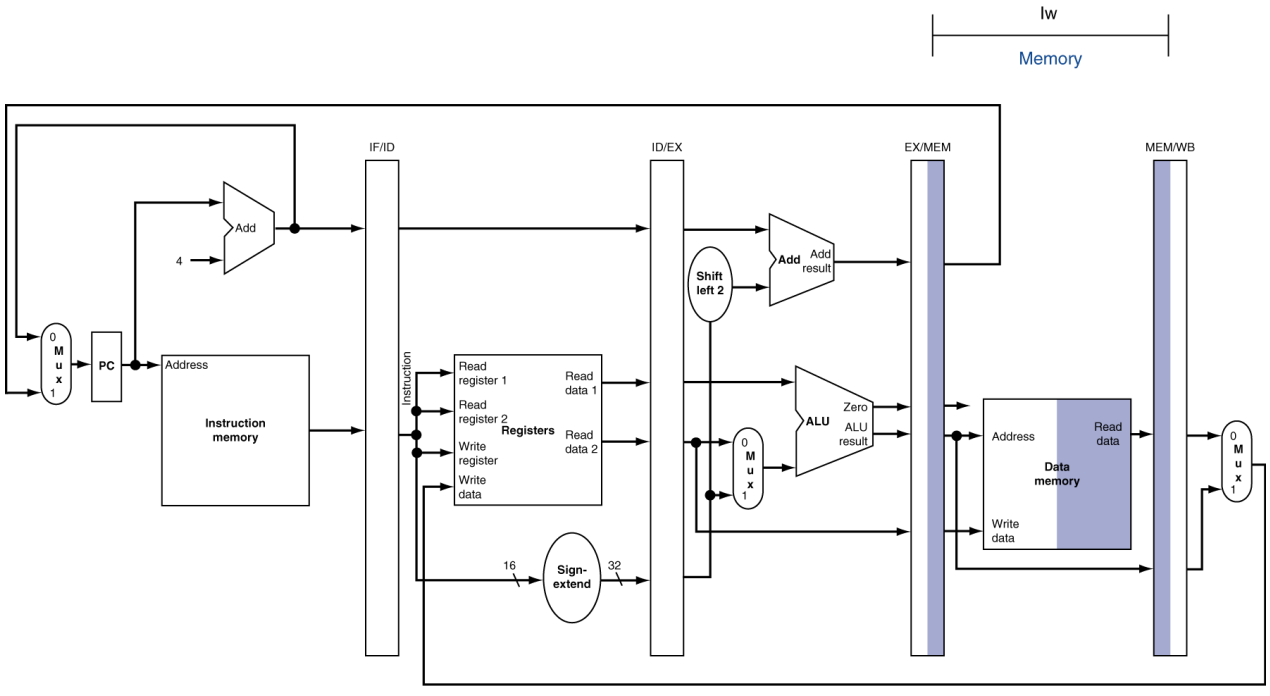


# EX para Load

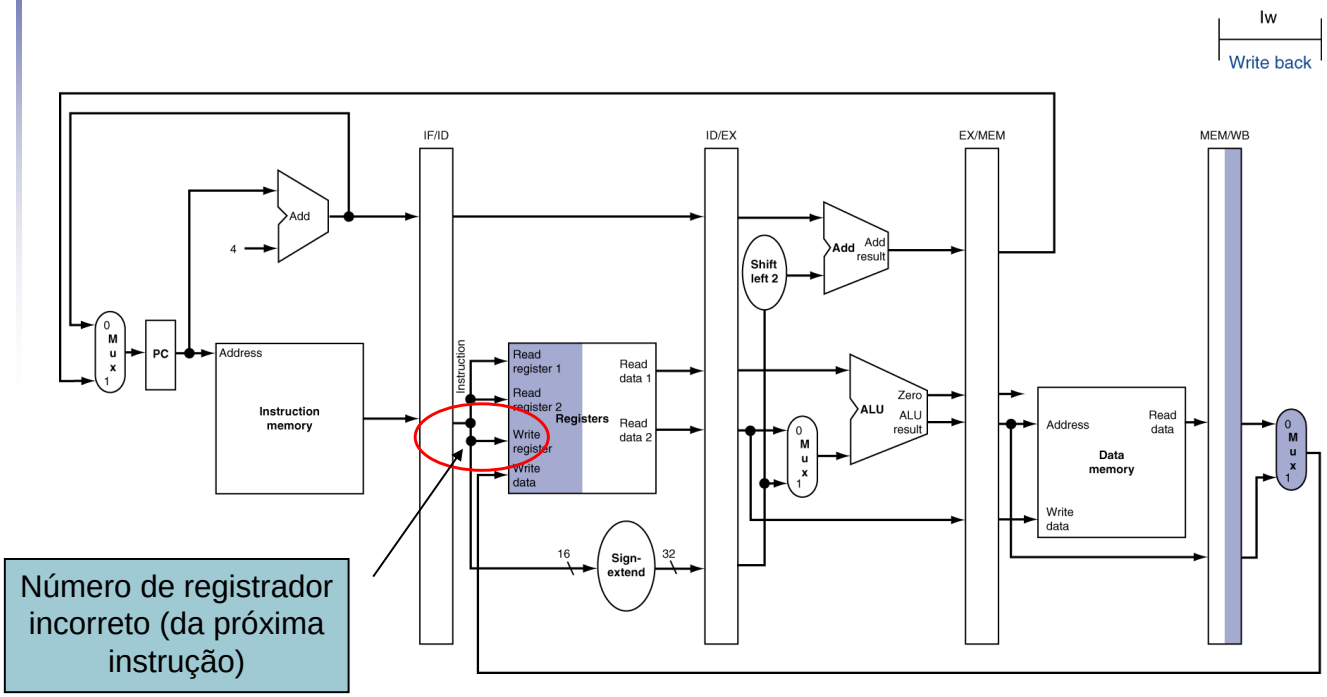





# MEM para Load



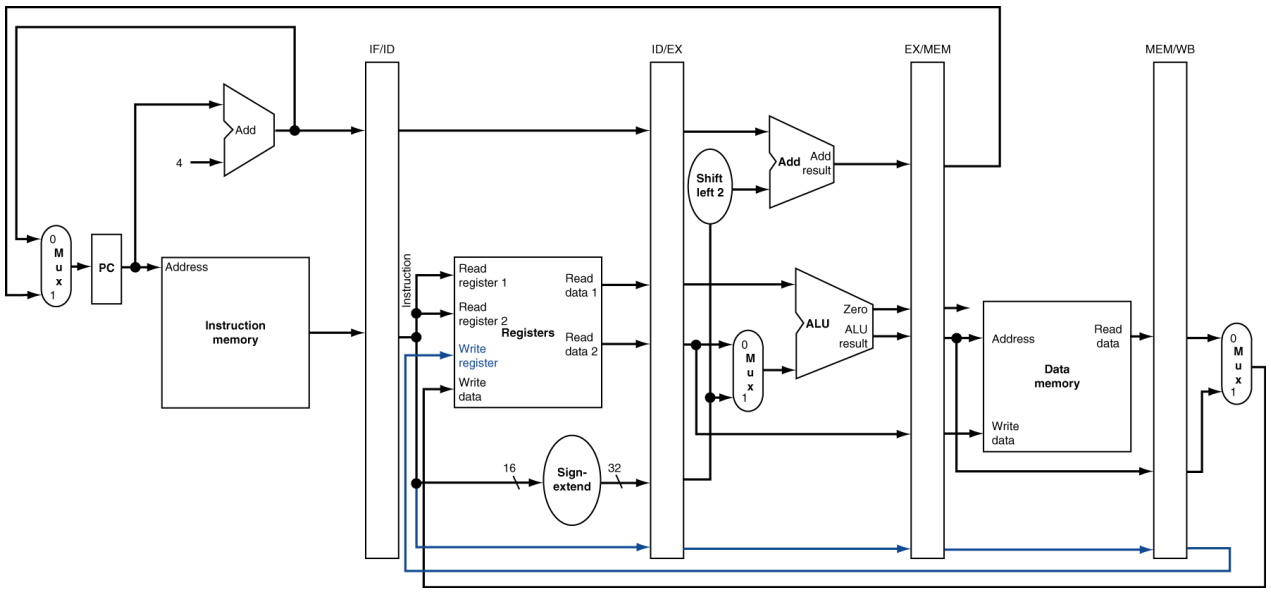
# WB para Load



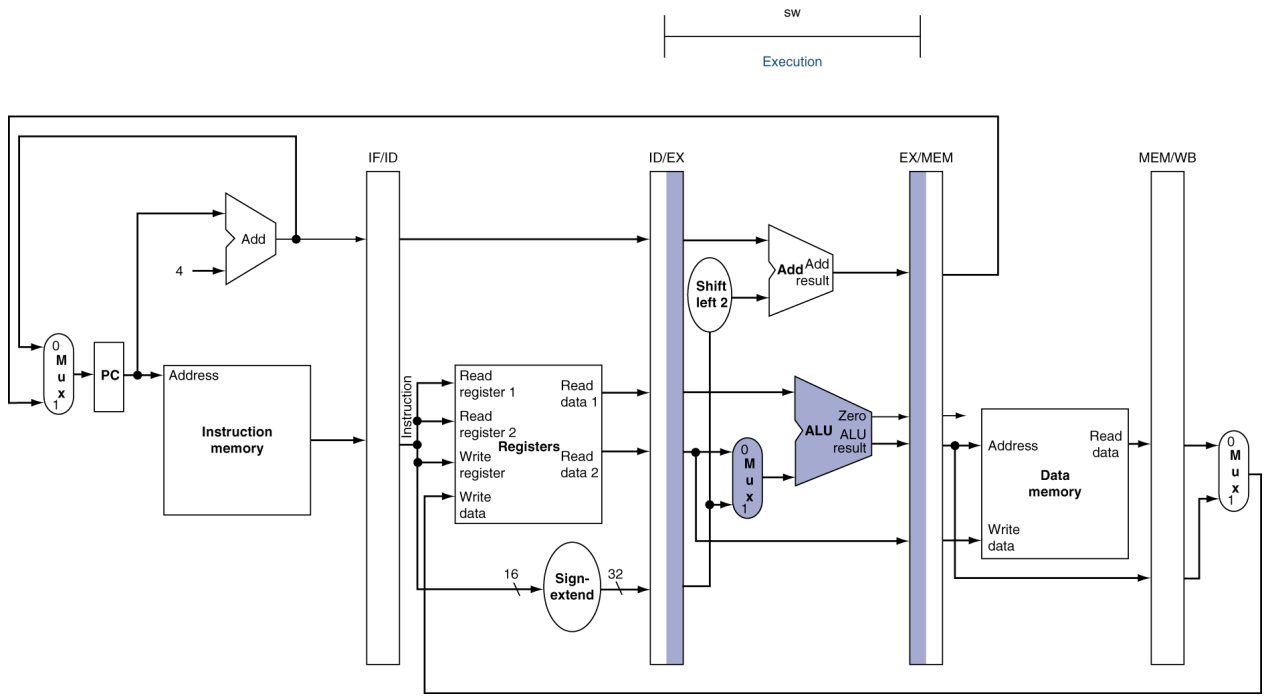

Número de registrador incorreto (da próxima instrução)



# Caminho correto para Load

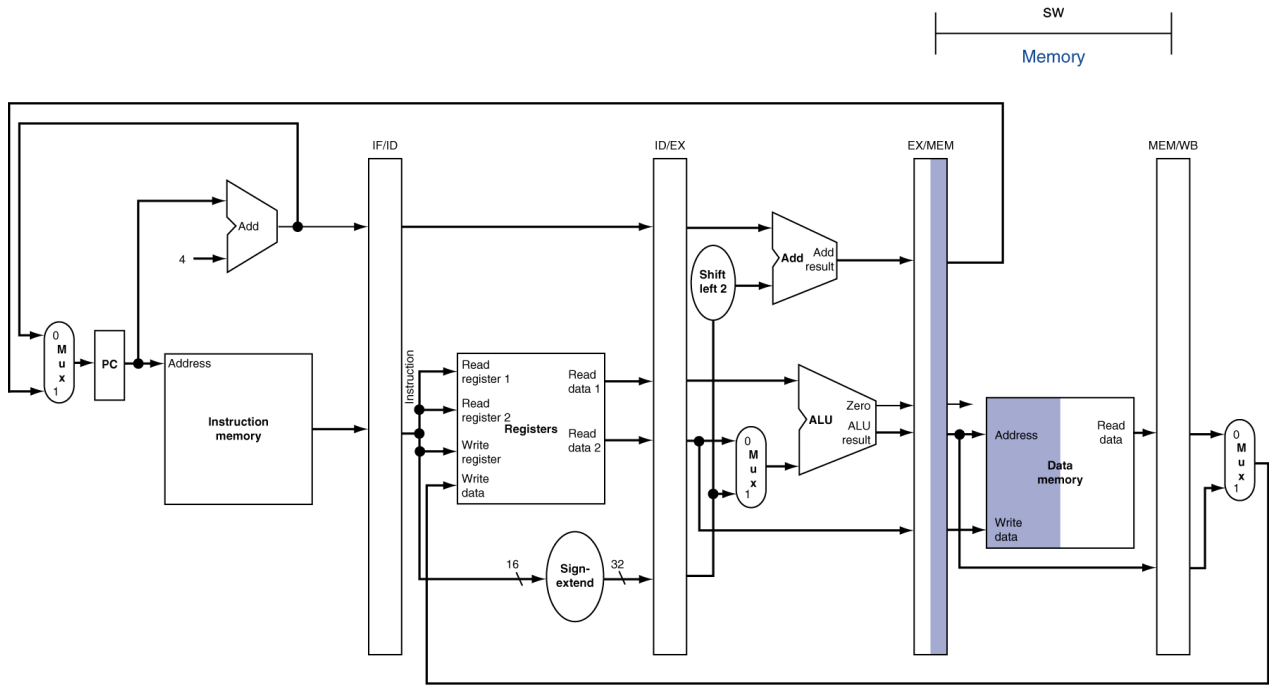


# EX para Store

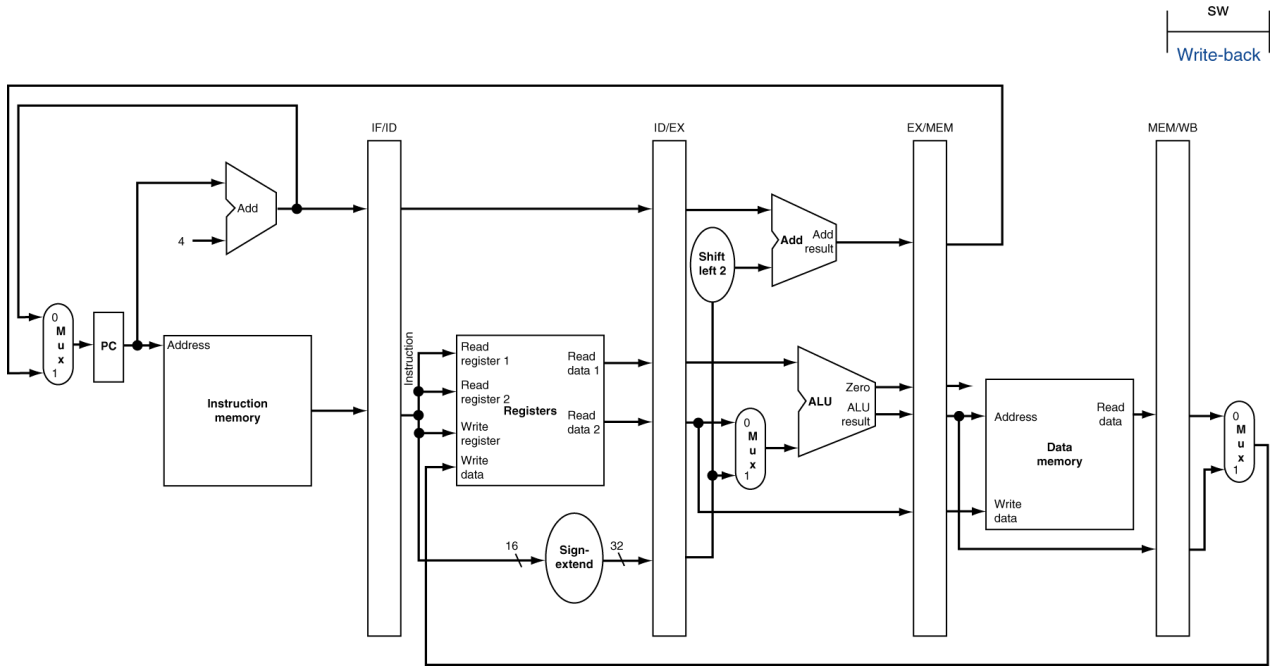





# MEM para Store



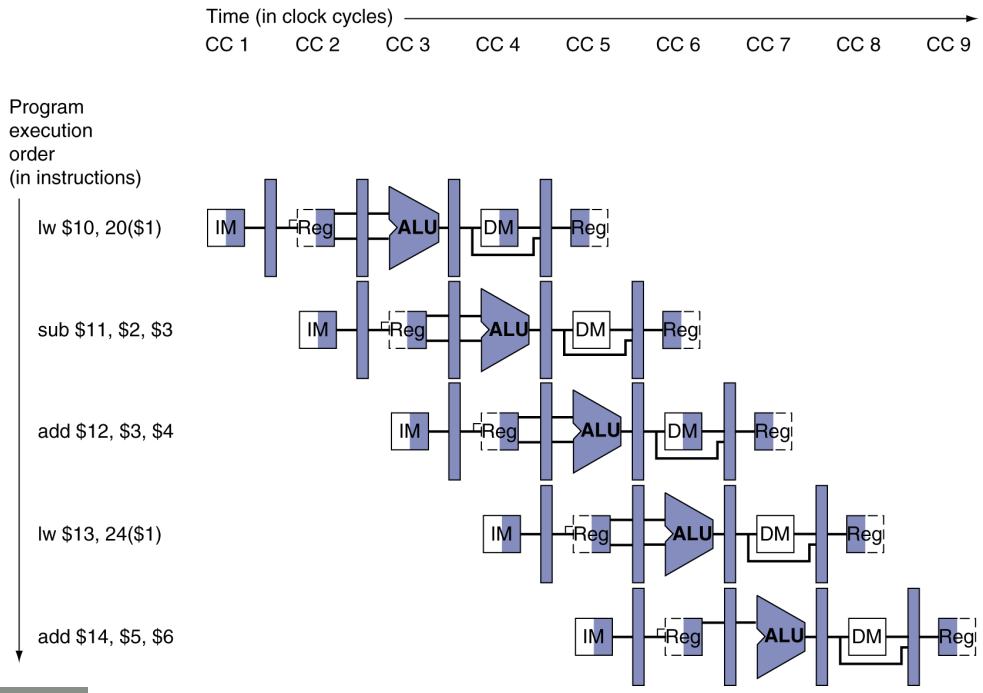
# WB para Store





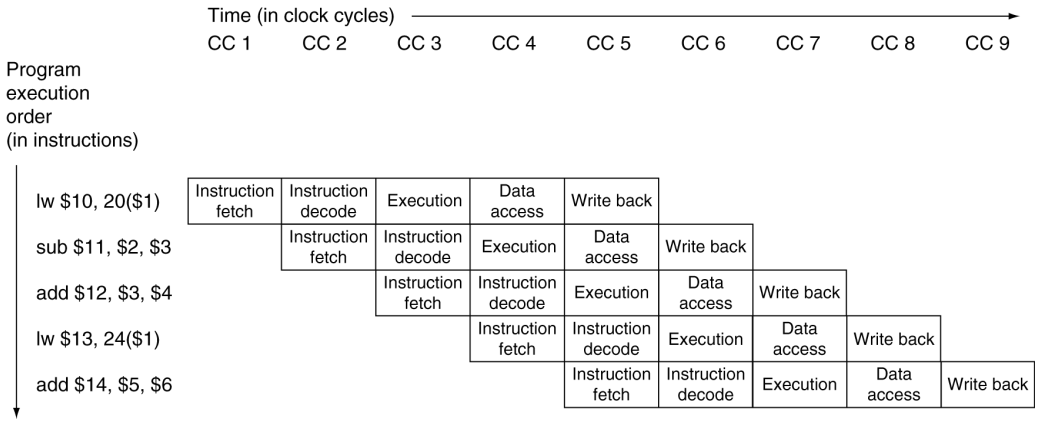

# Diagrama pipeline Multi-Cycle

- Formato que mostra o uso de recursos



# Diagrama pipeline Multi-Cycle

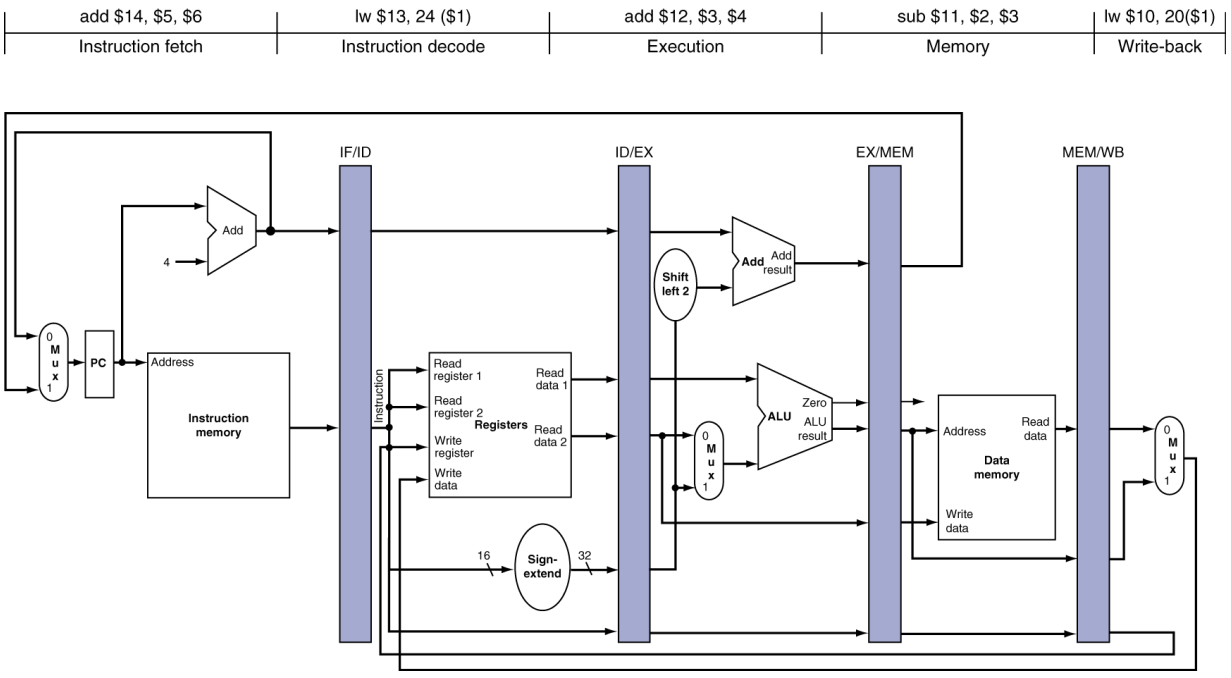
- Formato tradicional



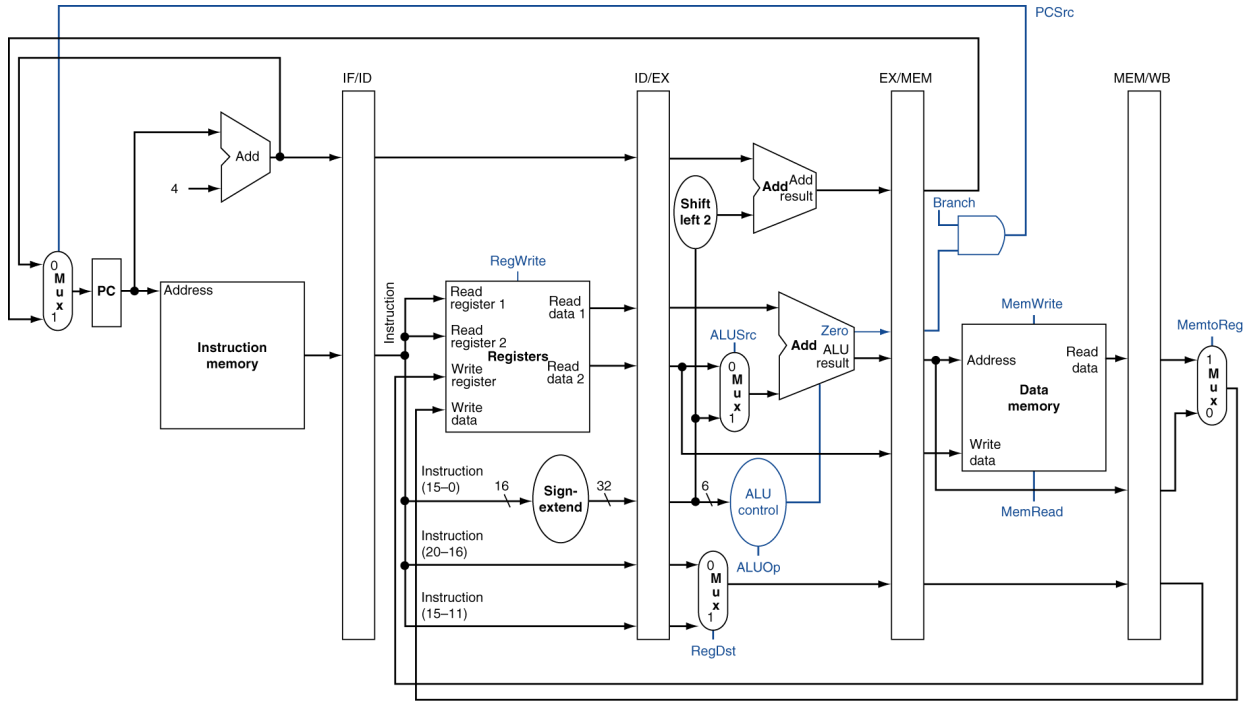



# Diagrama pipeline Single-Cycle

- Estado de um pipeline num dado ciclo



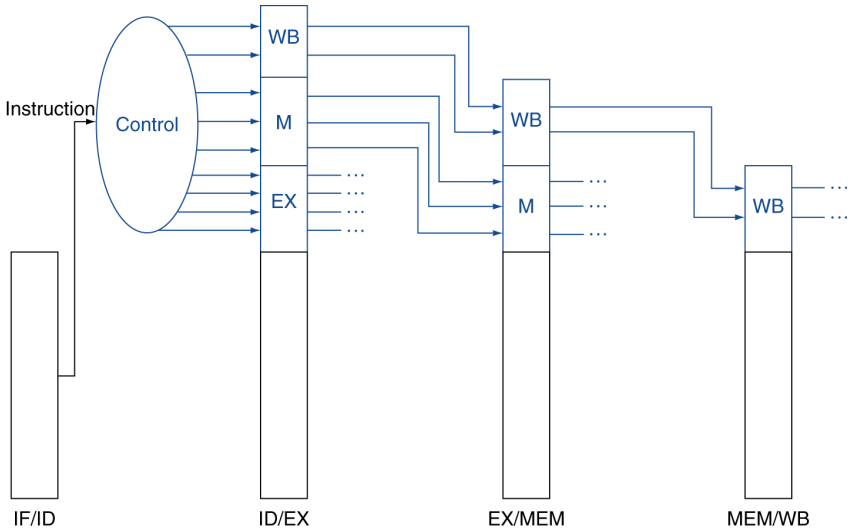
# Controle no Pipeline (simplif.)






# Controle no pipeline

- Os sinais são definidos a partir da instrução
  - Como na implementação monociclo



# Controle no Pipeline