

COMPUTER ORGANIZATION AND DESIGN

The Hardware/Software Interface

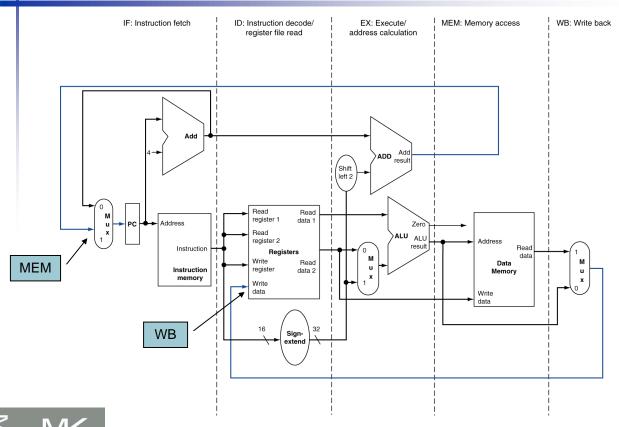


Arquitetura de um processador

4. Pipeline: caminho de dados e controle

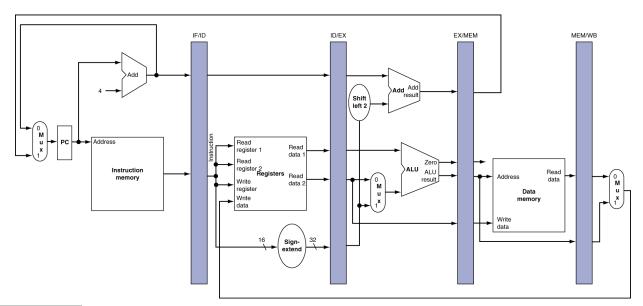
Prof. John L. Gardenghi Adaptado dos slides do livro

Caminho de dados com pipeline



Registradores pipeline

- Há registradores entre os estados
 - Armazenam a informação do ciclo anterior





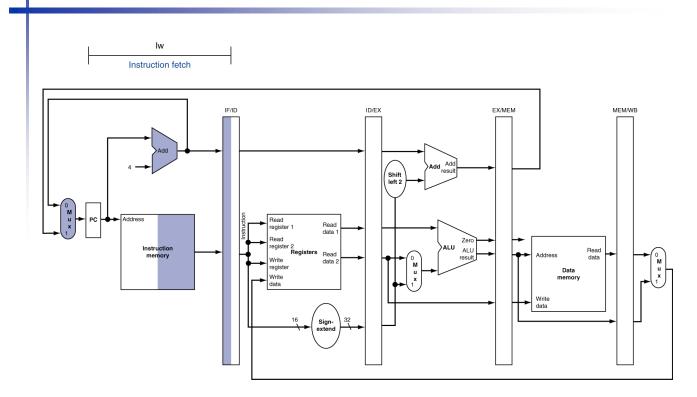
3

Representação gráfica do pipeline

- Fluxo de uma instrução por ciclo de clock através do caminho de dados pipeline
 - Diagrama de pipeline "Single-clock-cycle"
 - Mostra o uso do pipeline num único ciclo de clock
 - Destaca os recursos utilizados
 - Diagrama "multi-clock-cycle"
 - Gráfico da operação através do tempo (com as fases do pipeline)
- Próximos slides: diagramas "single-clockcycle" para load & store



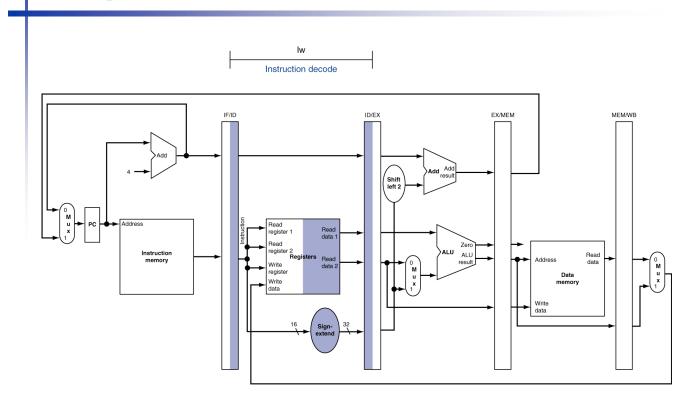
IF para Load, Store, ...



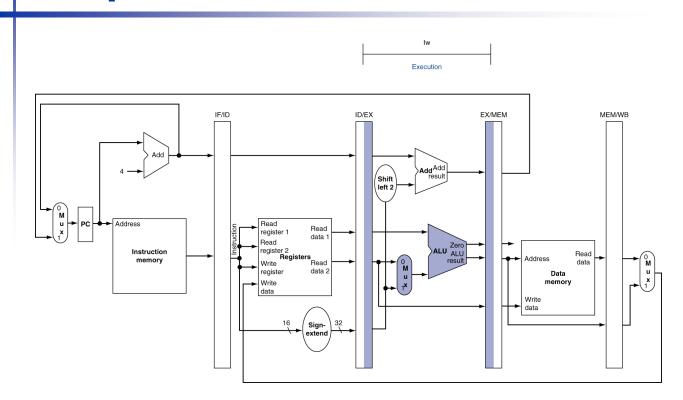
NORTH NAME AND PROPERTY OF THE PROPERTY OF THE

Chapter 4 — The Processor — 5

ID para Load, Store, ...



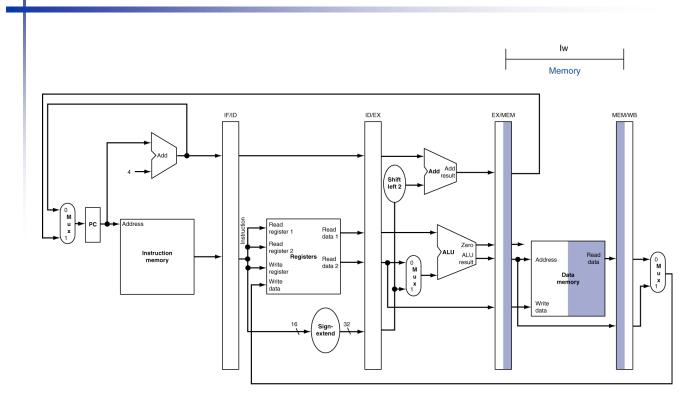
EX para Load



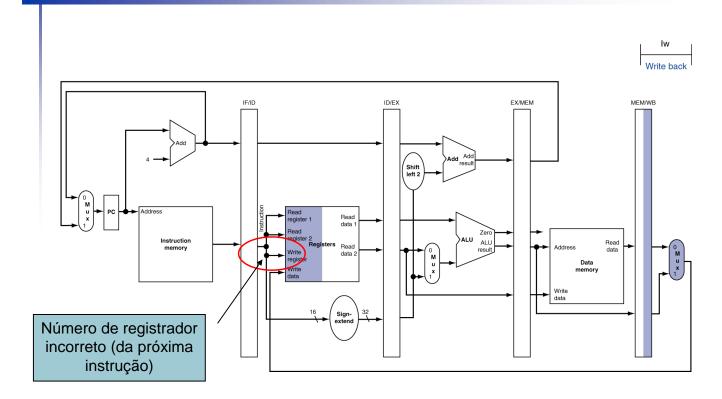
NO MORGAN KAUFHANN

7

MEM para Load



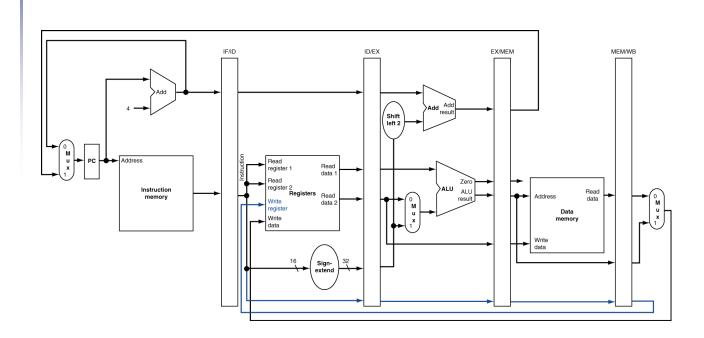
WB para Load



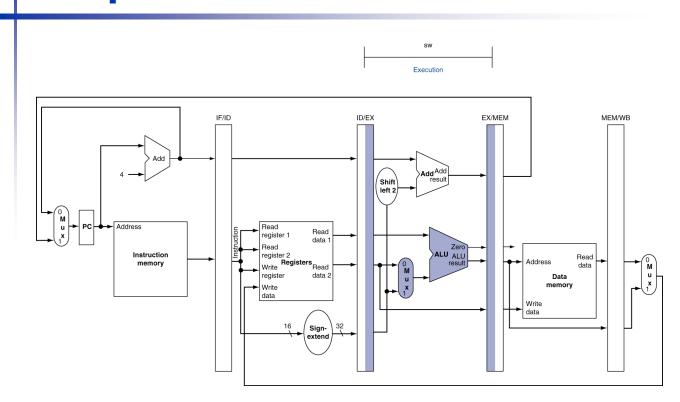
MORGAN KAUFHANN

9

Caminho correto para Load



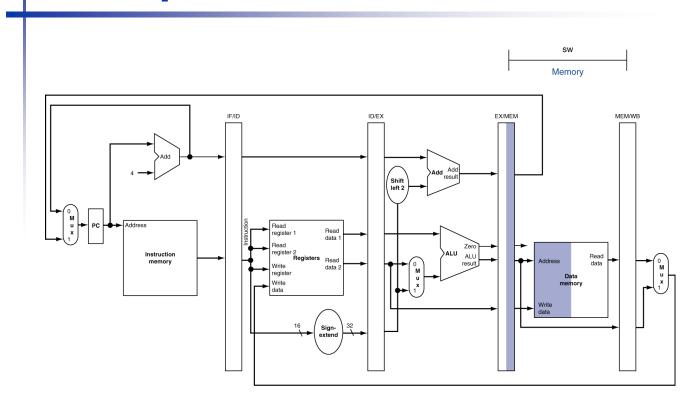
EX para Store



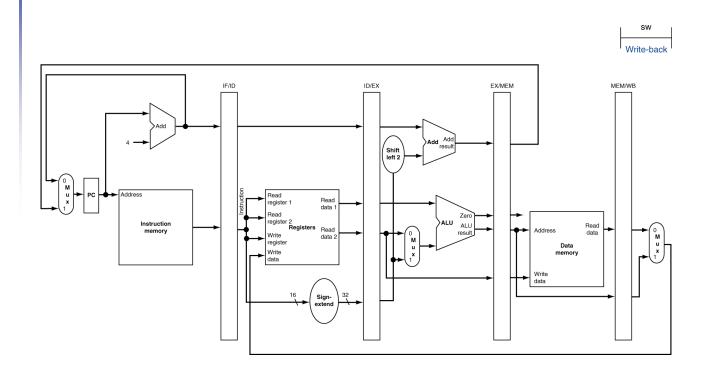
NO NO NA KAUFFAAN

11

MEM para Store



WB para Store





13

Diagrama pipeline Multi-Cycle

Formato que mostra o uso de recursos

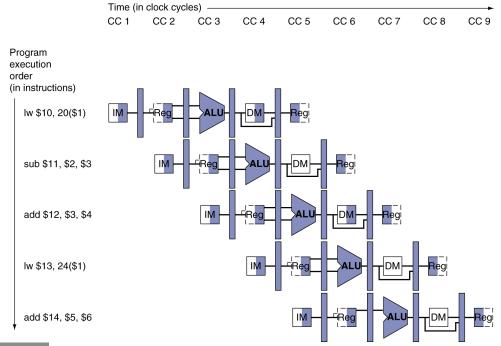


Diagrama pipeline Multi-Cycle

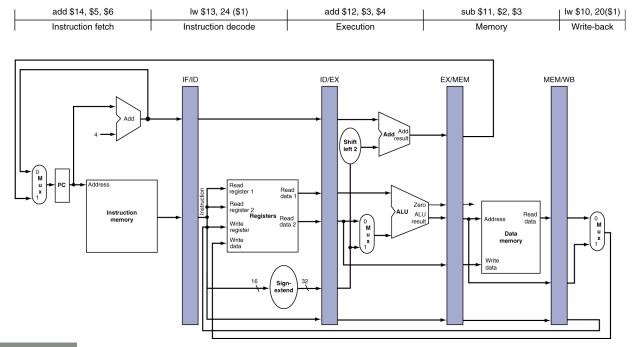
Formato tradicional

		es) ———								
		CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
Program execution order (in instructions)										
	lw \$10, 20(\$1)	Instruction fetch	Instruction decode	Execution	Data access	Write back				
	sub \$11, \$2, \$3		Instruction fetch	Instruction decode	Execution	Data access	Write back			
	add \$12, \$3, \$4			Instruction fetch	Instruction decode	Execution	Data access	Write back		
	lw \$13, 24(\$1)				Instruction fetch	Instruction decode	Execution	Data access	Write back	
	add \$14, \$5, \$6					Instruction fetch	Instruction decode	Execution	Data access	Write back



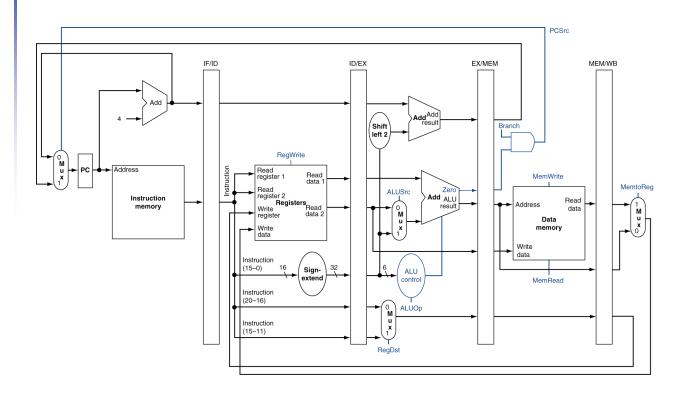
Diagrama pipeline Single-Cycle

Estado de um pipeline num dado ciclo



15

Controle no Pipeline (simplif.)

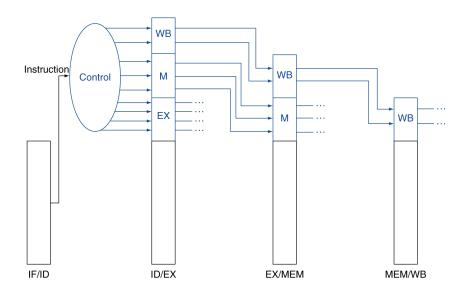




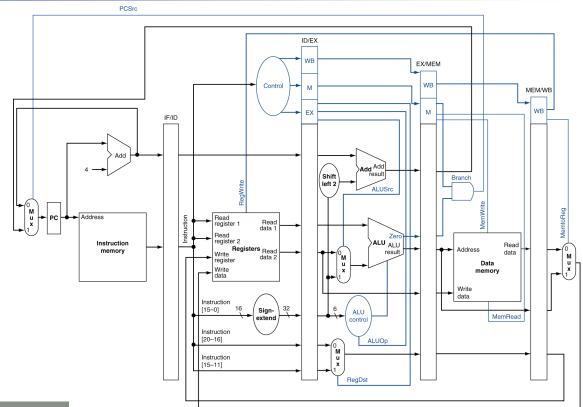
17

Controle no pipeline

- Os sinais são definidos a partir da instrução
 - Como na implementação monociclo



Controle no Pipeline



NORGAN KAUFHANN

19