M6MGB/T321S4TP

33,554,432-BIT (2,097,152 - WORD BY 16-BIT/4,194,304-WORD BY 8-BIT) CMOS 3.3V-ONLY FLASH MEMORY &
4,194,304-BIT (262,144-WORD BY 16-BIT/524,288-WORD BY 8-BIT) CMOS SRAM
Stacked - µ MCP (micro Multi Chip Package)

Description

The M6MGB/T321S4TP is a Stacked micro Multi Chip Package (S- µMCP) that contents 32M-bit Flash memory and 4M-bit Static RAM in a 52-pin TSOP.

32M-bit Flash memory is a 4,194,304 bytes / 2,097,152 words, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR (Divided bit-line NOR) architecture for the memory cell.

4M-bit SRAM is a 524,288 bytes / 262,144 words asynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MGB/T321S4TP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight.

M6MGB/T321S4TP provides for Software Lock Release function. Usually, all memory blocks are locked and can not be programmed or erased, when F-WP# is low. Using Software Lock Release function, program or erase operation can be executed.

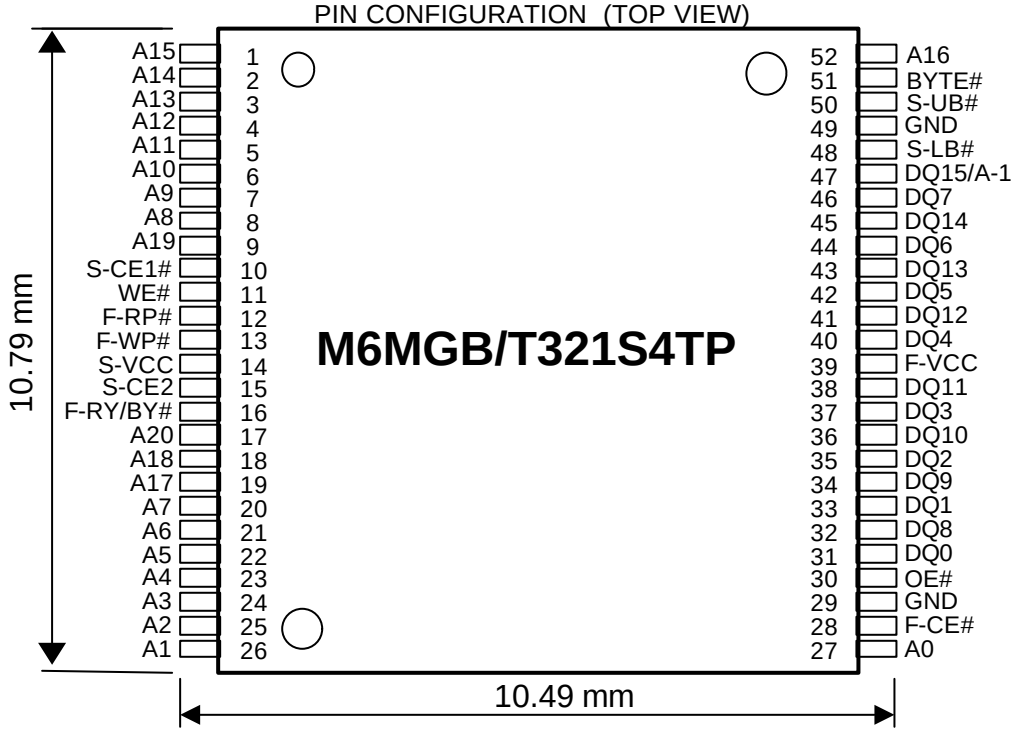
Features

Access Time	Flash	85ns (Max.)
	SRAM	85ns (Max.)
Supply Voltage		VCC=2.7 ~ 3.6V
Ambient Temperature		Ta=-20 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm

Application

Mobile communication products

PIN CONFIGURATION (TOP VIEW)



F-VCC	:Vcc for Flash
S-VCC	:Vcc for SRAM
GND	:GND for Flash/SRAM
A-1-A17	:Flash/SRAM common Address
A18-A20	:Address for Flash
DQ0-DQ15	:Data I/O
F-CE#	:Flash Chip Enable
S-CE#,S-CE2	:SRAM Chip Enable
OE#	:Flash/SRAM Output Enable
WE#	:Flash/SRAM Write Enable
F-WP#	:Flash Write Protect
F-RP#	:Flash Reset Power Down
F-RY/BY#	:Flash Ready/Busy
BYTE#	:Flash/SRAM Byte Enable
S-LB#	:SRAM Lower Byte
S-UB#	:SRAM Upper Byte

Outline 52PTC-A

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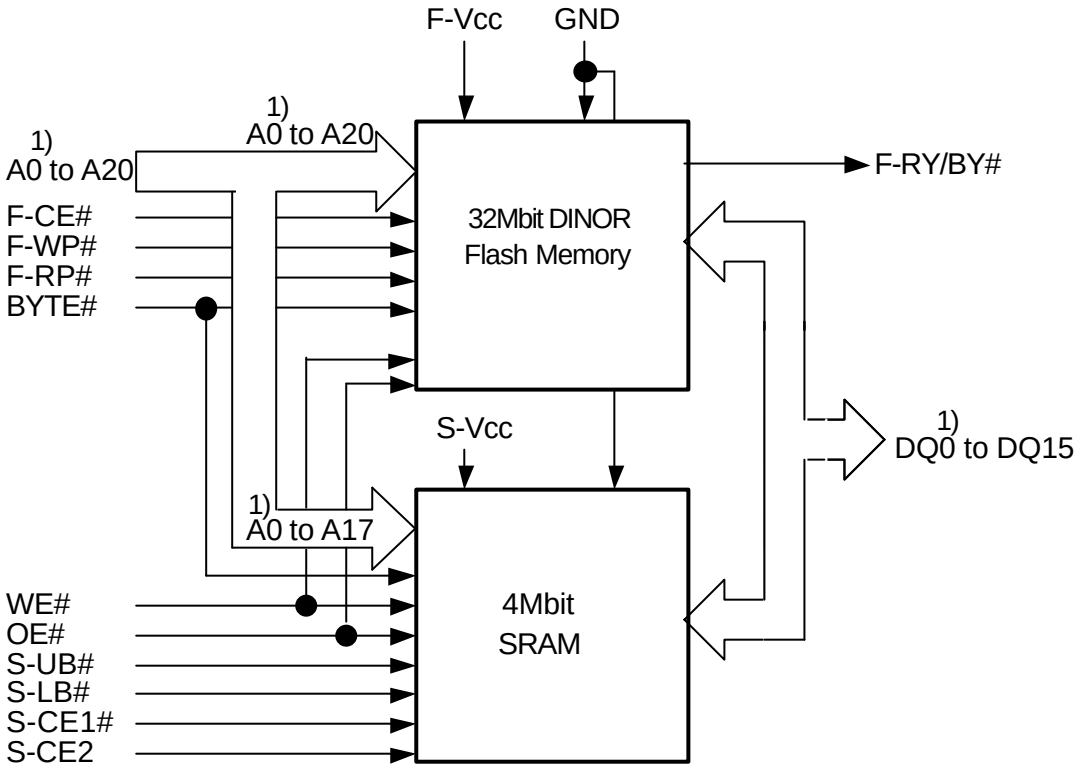
MCP Block Diagram



Note 1): In case of x8 organization, A-1 is added, and only Lower Byte data(DQ0 to DQ7) are assigned to I/O and Upper Byte data(DQ8 to DQ15) are High-Z.
Note 2): In the flash memory part there are "VCC"s which mean "F-VCC".
In the SRAM part there are "UB#" and "LB#" which mean "S-UB#" and "S-UB#", respectively.

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A20-A0, OE#, WE#, F-CE#, F-WP#, F-RP#, S-CE1#, S-CE2, BYTE#, S-LB#, S-UB#	Ta=25°C, f=1MHz, Vin=Vout=0V			18	pF
COUT	Output Capacitance	DQ15-DQ0,F-RY/BY#				22	pF

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