POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2005
Programme: BE | Full Marks: 100
Course: Logic Circuits | Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define Analog and Digital Signals. What are the advantages of digital systems over analog systems? 2+3

   b) Determine the value of base x if $(211)_x = (152)_8$. 5

   c) Convert the following numbers from the given base to the other three bases indicated. 5

      i) Octal 623 to decimal, binary and hexadecimal.

      ii) Hexadecimal 24C5 to decimal, octal, and binary.

2. a) "Excess-3 code is a self-complementing code". Justify it. 5

   b) Differentiate between 1's complement and 2's complement methods of subtraction. Perform the subtraction by using 2's complement method of the following unsigned binary numbers. $(11010)_2 - (1000)_2$. 2+3

   c) State and explain De-morgan's theorems. 5

3. Find the complement of F = x + yz; then show that F. $\overline{F}$ = 0 and F + $\overline{F}$ = 1. 6

   Simplify the Boolean function 9

   F (w, x, y, z) = $\sum$(1, 3, 7, 11, 15)

   that has don't – care conditions

   d (w, x, y, z) = $\sum$ (0, 2, 5)

   and then implement the function using logic gates.

4. a) Design a combinational circuit that converts a 8, 4, -2, -1 code to BCD code. 8

   b) Implement a full-adder circuit with a decoder and two OR gates. 7

5. a) What is a flip-flop? Explain the operation of J-K flip-flop. Also mention the merits of J-K flip-flop over R-S flip-flop. 2+4 +2

   b) Design a 3-bit synchronous binary counter using T-flip-flops. 7

6. a) Design a 4-bit arithmetic circuit having 3-selection inputs. The circuit should be capable of performing eight different functions. 8

   b) Draw the block diagram of 4-bit ALU and explain it. 7

7. ***Write short notes on (Any Two)*** 2×5

   a) Nibble adder

   b) Shift registers

   c) Gray code

   d) Master-slave flip-flop.

POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2012
Programme: BE | Full Marks: 100
Course: Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	User's complement to subtract the following i. $(00101101)_2 - (10110101)_2$ ii. $(835701)_{10} - (569812)_{10}$	5
	b)	Compare and contrast digital system with analog system.	5
	c)	Explain the parity method of error detection with a suitable example.	5
2.	a)	Realize all the basic gates using NOR gate only	5
	b)	Distinguish between minterms and maxterms.	5
	c)	What is processor unit? Draw it's block diagram.	5
3.	a)	Simplify the following Boolean function: $F(W,X,Y,Z) = \sum(1,6,7,8,11,13)$ with don't care condition $d(W,X,Y,Z) = \sum(0,2,3,4,10,12)$ and then implement the function using NOR gates only	7
	b)	Design a code conversion circuit which converts BCD to excess-3 code.	8
		OR	
		Design a code converter circuit to convert 8, 4,-1,-2 code to gray codes.	8
4.	a)	Design a full Subtractor using two 4 ×1 MUX.	7
		OR	
		Implement the following function using 8×1 multiplexer. $Y(A,B,C,D)= \Sigma (0,1,2,5,9,11,13,15)$	7
	b)	Explain the following: i. Synchronous and asynchronous logic	8

ii. Combinational and sequential logic

5.	a)	Explain the operation of a J-K flip flop along with it's characteristic table. Write down it's characteristic equation and graphic symbol. What are the drawback of R-S flip flop?	7
	b)	Design 4 bit updown counter using T flip flop.	8
6.	a)	Describe the operation of a four bit shifter with a neat diagram.	7
	b)	Discuss the purpose of shift register. Explain serial in parallel out and parallel in parallel out shift register.	2+3+3
7.	Write short notes on **any two:**		2×5
	a)	State table and State diagram	
	b)	PLA	
	c)	State diagram and state table	

POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2011
Programme: BE | Full Marks: 100
Course: Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Compare analog and digital system. Which one is better and why? 5

   b) Use r′s complement to subtract the following: 5

      i. $(100)_2 - (110000)_2$

      ii. $(7850)_{10} - (7650)_{10}$

   c) What do you mean by alphanumerical code? "Excess- 3 codes are called self complementing code". Explain it. 5

2. a) Simplify the Boolean function **F** and don't care conditions **d** in (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given: 7

      i. **F**= A'B'D'+A'CD+A'BC

      ii. **d**=A'BC'D+ACD+AB'D'

   b) Design a code converter circuit which converts 8 4 -2 -1 code to binary. 8

3. a) Design a circuit that compares two 3 bit numbers A and B to check if they are equal. The circuit has one output 'y' so that y = 1 if A = B and y = 0 if A $\neq$ B. 8

   OR

   Design a combinational circuit using a ROM. The circuit accepts a 3 bit numbers and generates an output binary number equal to the sum of the input numbers. 8

   b) What is multiplexer? Describe 4:1 multiplexer with internal diagram. 7

4. a) Differentiate between combinational and sequential logic circuit. 5

   b) Implement a full adder using 3×8 decoder and OR gates. 5

c) Give the truth table, logic diagram and characteristics equation of J-K flip flop. 5

5. a) Define shift registers. Explain operation of parallel in parallel out shift register. 8

b) Design a 3-bit synchronous binary counter using T-flip-flop. 7

6. a) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations. 8

b) Design a 4- bit combinational logic shifter and explain it. 7

7. Write short notes on **any two:** 2×5

a) Tristate logic

b) Output Hazard Race

c) Universality of 'NAND' and 'NOR gate

d) Design of BCD adder

POKHARA UNIVERSITY

Level: Bachelor | Semester: Spring | Year : 2014
Programme: BE | Full Marks: 100
Course: Logic Circuit | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define positive and negative logic system. "Digital circuits are easier to design than analog circuit." Do you agree with this statement? Give reasons to support your answer. 7

   b) Find the value of X. 8

   i) $(777)_x = (212)_8$

   ii) $(DEC)_H = (0101)_x$

   iii) $(563)_7 = (X)_3$

   iv) $(100111)_{Gray} = (X)_{Binary}$

2. a) State and Prove De-Morgan's Theorem. List out the factors to be considered while constructing the Logic Gates. 7

   b) What is Don't care condition? Simplify given function using K-map with circuit design. 8
   $F(W,X,Y,Z)=\Sigma(1,4,5,6,12,14,15)$ and don't care condition $D(W,X,Y,Z)= \Sigma (10,11)$.

3. a) Define universal gate. Design the three bit EX-OR circuit using only Universal gates. 7

   b) Design a combinational circuit that accepts a 3 bit number as input and generates the output binary number equal to the 2's complement of input number. 8

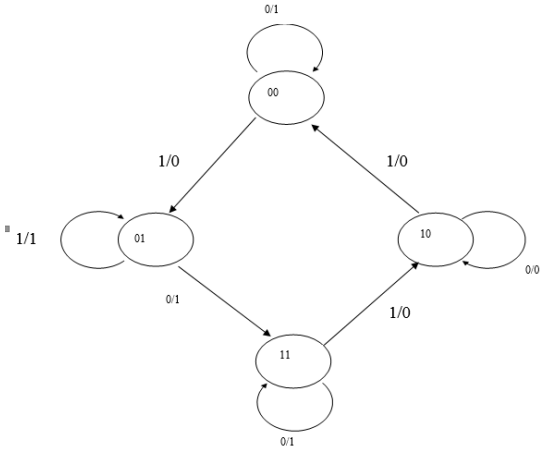
4. a) Show how a full adder can be converted to a full substractor with the addition of one inverter circuit. 7

   b) Implement the following :

   i. $F(A,B,C)= \sum (1,3,5,6)$ (using MUX) 8

ii. F1=∑(0,2,5) F2=∑(3,4,7) F3=∑(6,7) (using ROM)

5. a) Realize the following state diagram into a circuit using j-k flip-flop. 8



7

b) Describe read and write operation in RAM with diagram. Draw a circuit for 6-bit SIPO shift register.

6. a) Design an arithmetic circuit with one selection variable and two data inputs A and B, When S= 0, the circuit performs the addition operation F = A+B when S= 1, the circuit performs the increment operation F= A+1 (only show the block diagram). 8

b) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations. 7

7. Write short notes on: (**Any two**) 2×5

a) Master slave flipflop.

b) Nibble Adder.

c) PLA.

POKHARA UNIVERSITY

Level: Bachelor | Semester: Fall | Year : 2014
Programme: BE | Full Marks: 100
Course: Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the differences between Digital and Analog system. Why digital systems are preferred rather than Analog system. 5

   b) Add and multiply the following number in the given base without converting to decimal. 5

      i. $(1230)_4$ and $(23)_4$

      ii. $(135.4)_6$ and $(43.2)_6$

   c) Perform the following conversion. 5

      i. $(5849)_{10}$ = ( )$_{Excess-3}$

      ii. $(8412)_{10}$= ( )$_{2421}$

      iii. $(10101111)_{GRAY}$ = ( )$_2$

2. a) Simplify the following expression using Boolean algebra 5

      i. $(AB'+ABC)'+A(B+AB')$

      ii. $[(BC'+A'D)\ (AB'+CD')]'$

   b) Given the following Boolean function: $F= xy + x'y'+y'z$ 5

      i. Implement it with OR and NOT Gate

      ii. Implement it with only AND and NOT Gate

   c) A Boolean function is given by $F(A,B,C,D) = \sum(3,4,5,7,9,13,14,15)$ and don't care condition $d(A,B,C,D) = \sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only. 5

3. a) Design a combinational circuit that converts a decimal digit from the 2421 code to 84-2-1 code to binary. 8

   b) Design a BCD to Excess -3 code converter circuit. 7

4. a) Design a Comparator circuit that compared two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible 8

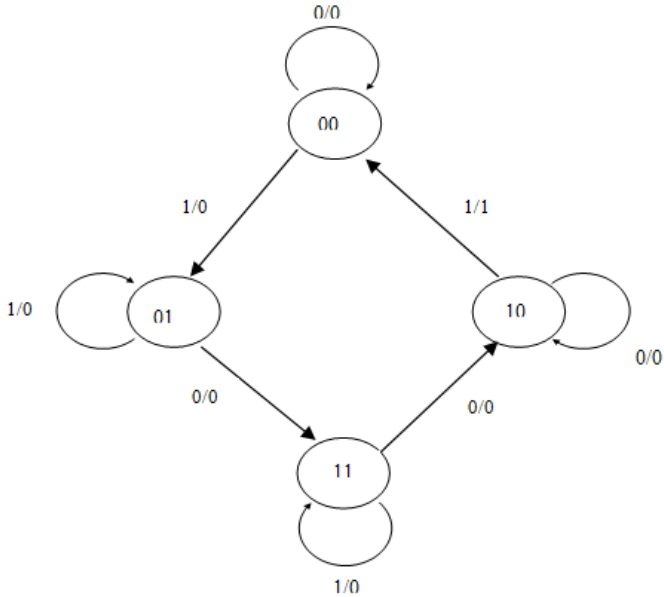
outcomes. i.e . A>B, A<B and A= B.

b) Implement the following with appropriate MUX: 7

i. $F(A,B,C)= \sum (1,3,5,6)$

ii. $F(A,B,C,D)= \sum(0,1,3,4,8,9,15)$

5. a) Design a sequential circuit corresponding to the given state diagram using S-R flipflop. 8



b) Explain operation of J-K Flip-flop with its logic diagram and truth table. 7

6. a) What is counter? Explain its any one of its type in brief. 8

b) Design 4-bit logical circuits which perform eight different logical operations. 7

7. Write short notes on: (**Any two)** 2×5

a) Parity checker

b) Output Hazard Races

c) Status Register.

POKHARA UNIVERSITY

Level: Bachelor | Semester: Fall | Year : 2015
Programme: BE | Full Marks: 100
Course: Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Which system is more efficient for logical computation? Differentiate between Digital and Analog system. 5

   b) Perform the conversion as indicated (any two). 5

      i. $(243)_6 = (\quad)_{\text{Excess-3}}$

      ii. $(816)_{10} = (\quad)_{2421}$

      iii. $(BE)_{16} = (\quad)_2$

   c) Use 2's complement to subtract the following: 5

      i. $(101)_2 - (10100)_2$

      ii. $(3950)_{10} - (876)_2$

      iii. $(378)_{BCD} - (256)_{BCD}$

2. a) Prove the following Boolean expression. 5

      i. $\overline{A}\,\overline{B} + BC + \overline{A}B\overline{C} = \overline{A} + BC$

      ii. $X\overline{Y} + Y\overline{Z} + Z\overline{X} = \overline{X}Y + \overline{Y}Z + \overline{Z}X$

   b) Simplify the Boolean function **F** and don't care conditions **d** in (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given: 5
   F= A'B'D'+A'CD+A'BC
   d=A'BC'D+ACD+AB'D'

   c) A Boolean function is given by F(A,B,C,D) = $\sum(3,4,6,8,10,12,14)$ and don't care condition d(A,B,C,D) = $\sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only. 5

3. a) Design a single combinational logic circuit that performs the addition of two input bits (a and b) when third input bit c is set to 0 whereas, 7

the same circuit performs the subtraction of same two input bits when c is set to 1.

OR

Design a code converter circuit that converts binary code into Gray code.

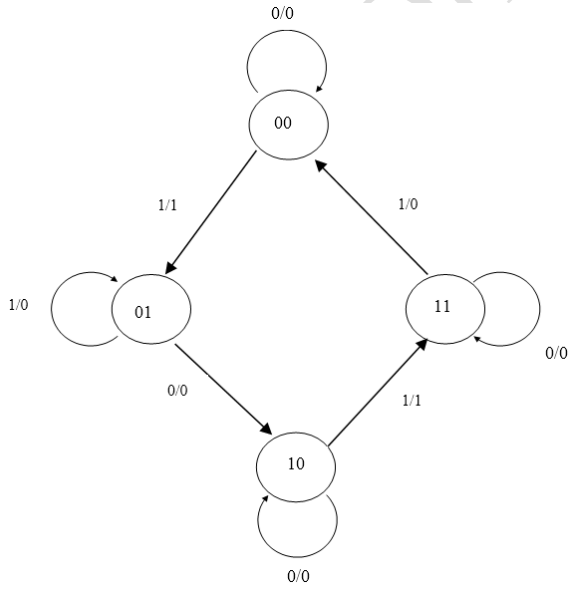
b) Design a BCD synchronous up counter using T-flip flop. 8

4. a) Implement the following three Boolean function with a PLA 8

$F_1 = \sum(0,1,2,4)$ $F_2 = \sum(0,5,6,7)$ $F_3 = \sum(0,3,5,7)$

b) What do you mean by Decoder? Implement the following Boolean function $F = \sum(1,3,5,6)$ using 4 * 1 MUX. 7

5. a) Design a sequential circuit corresponding to the given state diagram using D Flip Flop for the following state diagram. 8



b) Explain operation of J-K Flip-flop with its logic diagram, truth table, excitation table. 7

6. a) What is counter? Differentiate between serial in serial out register and parallel in serial out register with associated diagrams. 8

b) Illustrate the process how does binary value of 4 flags in status registers change with necessary diagram. 7

7. Write short notes on: (**Any two**) 2×5

a) Random Access Memory.

b) Self complementing code.

c) Universal Gates.

POKHARA UNIVERSITY

Level: Bachelor | Semester: Spring | Year : 2012
Programme: BE | Full Marks: 100
Course: Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Compare and contrast analog and digital system. 7
   b) Compute any four of the followings as indicated. 8
      i. $(11101)_{gray} = (\ )_2$
      ii. $(706)_8 = (\ )_{16}$
      iii. $(512)_{10} = (\ )_8$
      iv. $(110110.101)_2 = (\ )_{10}$
      v. $(3FAFE.1BA)_{16} = (\ )_{10}$
2. a) Perform the following operation using BCD method. 5
      i) $689 - 354$
      ii) $496 + 825$
   b) Discuss in brief about gray code. 5
   c) Explain the parity method of error detection with a suitable example. 5
3. a) Discuss the universal property of NAND and realize all the basic gates using NAND gate only. 7
   b) Use K-map to simplify the given Boolean function in POS and implement the simplified function using NOR gate only. 8
      $F(A,B,C,D) = \sum(1,3,8,9,12,13,14,15)$, and don't care
      $, d(A,B,C,D) = \sum(2,7,10)$
4. a) Design a code converter circuit which converts 8 4-2-1 code to binary. 8

Or

Design a circuit diagram to generate and check the Odd Parity.

b) Derive a PLA program table for the combinational circuit that squares 3 bit number. 7

Or

Implement the following Boolean functions using multiplexer

i. $F(w, x, y, z) = \sum(0, 1, 3, 4, 5, 8, 9, 15)$

ii. $F(x, y) = \sum(1, 2, 3)$. Also draw the internal circuit of the resulting multiplexer.

5. a) What is a shift register? With the help of timing diagram explain the operation of serial-in-serial-out shift register. 7 8

b) What are the basic differences between combinational and sequential logic circuits. Explain the operation of a T flip-flop

6. a) Design an arithmetic circuit with two selection variables S_1 and S_0 that generates the following arithmetic operations. 8

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$
0	0	F = A	F = A + 1
0	1	F = A-B-1	F = A - B
1	0	F = B – A -1	F = B - A
1	1	F = A + B	F = A + B +1

b) Design a 3-bit synchronous gray code up counter using D flip-flop. 8

Or

Design a 4 bit gray code synchronous counter .Using T flip-flop.

7. Write short notes on: (Any two) 2×5

a) Venn diagram.

b) Design of Accumulator.

c) State reduction and assignment.

d) Decoder and encoder.