MODEL QUESTION

Level: Bachelor | Semester – Spring | Year : 2023
Programme: BESE, BECE | Full Marks: 100
Course: Digital Logic | Pass Marks: 45
First Year: First Semester | Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) List out the advantages of digital system over analog systems. Give some examples if digital system applications. 5

   b) Perform the following operation using 9's complement and 2's complement method. 5

      i) $(203)_{10} - (103)_{10}$

      ii) $(103)_{10} - (203)_{10}$

   c) Convert the following numbers from the given base to the other bases indicated. 5

      i) $(110011.101)_2 = (\quad)_8$

      ii) $(2FE.CC)_{16} = (\quad)_8$

      iii) $(123)_8 = (\quad)_6$

      iv) $(776)_8 = (\quad)_{16}$

      v) $(1101)_{\text{GRAY CODE}} = (\quad)_2$

2. a) Simplify the following function F in (1) sum of products and (2) product of sums using K-map 5

      i) $F(A,B,C,D) = \Sigma\,(0,1,2,,6,11,13,14)$

   b) Find out the complement of the following function and draw the logic diagram using basic gates. 5

      i) $F(x, y, z) = (x + y' + z)(x' + z')(x + y)$ 5

   c) Write down the differences between combinational logic and sequential logic.

3. a) Design BCD to Excess-3 code converter and draw the logic diagram. 7

   b) Explain two bit magnitude comparator and draw the circuit diagram. 8

4. a) What do you mean by Multiplexer? Implement the following Boolean function $F(w, x, y, z) = \sum_m (1, 2, 5, 7, 11, 15)$ using 8 to 1 Multiplexer with x, y, z as selection lines S_2, S_1 and S_0 respectively. 4

   b) Implement Full Adder using ROM. 4

OR

A combinational circuit is defined by the function

$F_1(X,Y) = XY + XZ'$ and $F_2(X,Y) = XZ' + YZ$

Implement the circuit with a PLA having three inputs, three product terms and two outputs.

   c) What do you mean by decoder? Design a 4 to 2 line priority encoder and draw the circuit diagram. 7

5. a) Explain the working principle of T Flip with its logic diagram, truth table, characteristics table and excitation table. 5

   b) Use 'T' flip-flop to design a 3-bit Synchronous UP Counter. 5

   c) Convert the JK Flip flop to realize T Flip flop. 5

6. a) A sequential circuit with two T Flip flops, A and B; two inputs, x and y; and one output, z, is specified by the next state and output equations: 8

$A(t+1) = x'y + xA$

$B(t+1) = x'B + xA$

and $z = B$

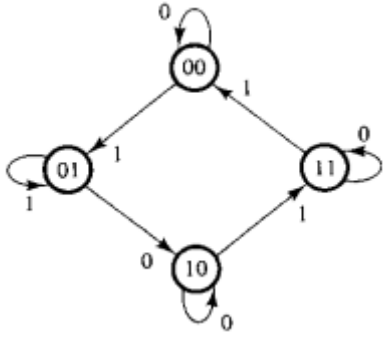
   i) Draw Logic diagram of the circuit.

   ii) Derive state table

   iii) Draw state diagram 7

OR

Draw the sequential circuit from the information provided in the state diagram in the figure below using JK flip-flops.



b) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations.

7. Write short notes on: (**Any Two**) 2×5

a) Output Hazard

b) Shift Register

c) Status Register