Optimizing Multiplier Performance with Advanced PTL-Based AND Gate and Efficient Full Adder Design

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***Abstract*--** **Multipliers are combinational circuits used to multiply binary digits. A multiplier circuit is commonly used in a variety of applications, including digital signal processing such as convolution, and filtering, audio and video processing, communication systems, etc. The multiplication process is carried out initially by generating the partial products (PP) and then summing them up to get the result. Due to the complexity of the multiplication operation and the number of operations needed to complete it, multiplier circuits typically use more power than other types of circuits. In a multiplier circuit, two numbers are multiplied by performing several additions and bit-shifting operations. Particularly when working with larger operands or operating at high frequencies, these processes demand a sizeable amount of power. There are several ways to improve the efficiency of the multiplier such as reducing the number of logic levels, using hardware acceleration like FPGA boards, etc. This study proposes an effective multiplier architecture that uses modified hybrid full adders (FA) and partial product generation using pass transistor logic (PTL) for AND gate. This architecture was to the conclusion after comparison of components such as AND gate, and Full Adders (FA) simulated under various designs using CMOS and TG logics. The suggested multiplier has good performance and low power consumption, making it a perfect option for digital signal processing applications.**

***Keywords:* Modified PTL AND, Delay, Power, Modified XOR XNOR**

# INTRODUCTION

A multiplier circuit is a digital circuit that multiplies two binary numbers by mathematics. The circuit has elementary logic gates cascaded together in several stages to form a multiplier circuit. There are several types of multipliers which include Array Multiplier, Booth Multiplier, Wallace Tree Multiplier, Logarithmic Multiplier.etc. In this paper, we will be working on an Array Multiplier. The array multiplier is the most popular kind of multiplier circuit. It comprises several AND gates in an array that do partial products, which are then added together by several adders to get the final product. Unlike adders and other arithmetic circuits, multipliers consume more power and have low speed comparably due to their increased number of stages and processing. Also, compared to simpler circuits, transistors used in multiplier circuits often have bigger gate areas, which means they consume more energy to turn on and off. The bigger gate area also causes a larger parasitic capacitance, which raises the circuit's overall power requirement.

In general, multiplier circuits can be built over various types of logic from CMOS logic, Pass Transistor Logic (PTL), Transmission Gates, or even modified logic using them. For certain applications as per requirement, the multiplier circuit also uses separate logic for AND gate and separate logic for the adder circuit. Authors [4] have proposed that CMOS logic in multipliers has several advantages, including high noise immunity and good performance at high frequencies. But CMOS logic consumes a large number of transistors contributing to the increased area of the circuit. On the other hand, Pass Transistor logic can also be used to implement an AND gate, but it may have higher power consumption and slower switching speeds compared to CMOS logic due to the extra capacitance and resistance added by the transistors in the circuit. Transmission Gates logic is another approach that can be used for implementing an AND gate. Transmission gate logic can offer high speed and low power consumption due to the use of transmission gates, but it can also suffer from increased area overhead and complexity compared to CMOS logic.

To overcome the above drawbacks in this paper we will be using separate logic for AND gate and Full Adders used in multiplier circuits. The multiplier circuit presented in this paper will constitute a modified Pass Transistor Logic based AND gate and a Hybrid Full Adder in which the XOR and XNOR gate logic will be modified. To have a clear understanding of the idea of combining the above logic for AND gate and Full Adder we have compared the power and area of multiple AND gates and Full Adders using CMOS logic, Pass Transistor Logic, Transmission gate logic, and other circuits like Domino based Full Adder and Ternary Adder.

# LITERATURE SURVEY

Many studies have been conducted in the aspect of reducing the overall power usage of the whole multiplier circuit and also not reducing its consistency and also to speed up the computation for use in many applications. We review related works on multiplier design and also the design of its important building blocks like AND gate and full adder circuits. J. Selvakumar; Vidhyacharan Bhaskar [1] proposed a low power 4×4 digital multiplier design to reduce power consumption of digital multipliers based on 2-dimensional bypassing method. Chang, Chip Hong.; Gu, Jiang Min.; Zhang, Mingyan [5] proposed a full adder circuit in hybrid style where the sum and carry generation circuits of the proposed design are designed with hybrid logic to operate at maximum-low supply voltage. Rajeev Kumar, Sandeep Gotam, Vikram Singh [3] proposed a XOR / XNOR gate circuit produces outputs separately by establishing simultaneous XOR - XNOR function and analyzed the power use and latency along with the yield capacity and short-circuit energy dissipation.

H. Naseri, S. Timarchi [6] proposed circuits that have highly optimized power consumption and delay by low short-circuit power dissipation and low output capacitance and the proposed circuits are seen for its merits in areas of driving capability, power-delay product (PDP), power consumption, speed. N.H.E. Weste, K. Eshraghian, [9] in their paper they studied the CMOS circuits, their processing technology, Circuit characterization and performance estimation of CMOS circuits.

Saeeid Oskuii, Per Kjeldsberg, Oscar Gustafsson [7] proposed an algorithm for reducing the stages which are employed in parallel multipliers which is used for reducing the power usage. A. Sadeghi, N. Shiri, M. Rafiee, P. Rahimi, [8] proposed circuits which use both the static and dynamic logic to see improvement in scalability and performance.

They proposed a new design called pseudo-dynamic logic (PDL) and the pull-up or pull-down networks are modified and float techniques, transmission gate, gate diffusion input and are combined in the provided complete adder to reduce area consumption.

# PROPOSED METHODOLOGY

*A. AND gate*

An AND gate is a logic circuit used in digital circuits that generates a logic ONE if all of its inputs are high. To put it another way, if any of its inputs are low, the result is logic ZERO. The AND gate in the array multiplier constitutes a major part along with the adder circuit to perform computation with simple circuitry and the role of AND gate in an array multiplier is to produce partial products that are subsequently added together to acquire the final result. Each bit in the partial product column is formed by multiplying the one bit of multiplier and one of multiplicand and this continues for every column.

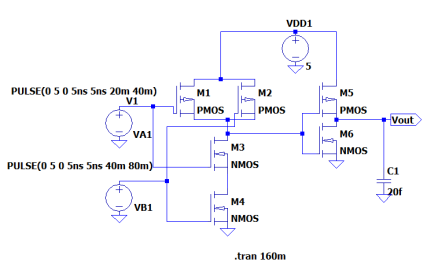
Conventional gates are typically built on technologies like complementary metal-oxide semiconductors (CMOS) [9], gate diffusion input (GDI) [10], and Transmission gate logic (TG) [11]. CMOS-based AND gates create a direct path between the power source and ground, leading to potential excessive power consumption and requiring substantial design area, which in turn can result in short-circuit power dissipation [12]. While GDI techniques demand minimal area, they don't yield maximum swing output, impacting system performance when used in multipliers.

On the other hand, TG gates, by requiring a minimal number of transistors in parallel formation, generate full-swing output, consuming less power and enabling faster computation [13]. However, they necessitate additional inverter circuits at the input side for transistor gate connections, making their area occupation comparable to CMOS-based gates. Designing the AND circuit involves a crucial trade-off among area, delay, power consumption, and output swing.

*B. Proposed AND gate based on Pass transistor logic (PTL)*

Here, an AND gate using Pass Transistor logic (PTL) is designed with a total of 7 transistors where 5 for the main circuit and 2 for giving the inverted form of input A. In this circuit, we have made use of floating technique which reduces the short circuit power dissipation [5]. Here, no inverter circuits are used in the critical path so we will experience a considerable increase in switching speed [9] as compared to CMOS circuits. Input signal A is only connected to the transistor’s gates and the output signal is completely dependent on Input signal B. As the most significant bit, Input A will involve low switching activity so this reduces the gate’s overall power. In the proposed AND gate, the output signals are produced by M3, M5, and M7 where the output is not maximum swing output.

For more clarity, when AB=01 the transistors are off and there is no path to the output. So, to restore this M4 and M6 are added to the circuit. When AB=00 and AB=01 the

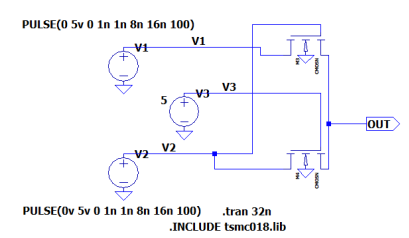
transistors M3, M4, M5, and M7 are OFF and the transistors M6 produces the output 0. When AB=10 then M3 is ON and the output is OFF. In this case, the 0 generated by M7 is passed M5 to output making the output voltage stronger and giving high driving capability it also ensures the elimination of high impedance [5] in previous as both these transistors M5 and M7 are in series. When AB=11 then these transistors M3, M5, and M7 produce the output and M6 is off and the output is made stronger and in full swing by M4. These all contribute to the low power-consuming circuit (as M6 is said to be ON in only state AB=00 and AB=01), and also the logic is faster due to fewer internal nodes and no inverter in the critical path. When coming to the importance of M5 and M7 they give add-on advantages as M3, M4, M6, and M7 are enough to produce full swing but these extra two transistors are level restoration transistors which can give benefits such as improved transition time, high logic swing generation when AB=11 and high noise immunity. The M7 transistor in this AND gate has capacitance Cx which ensures the fast transition of output state and it is a speed-up transistor. When it comes to delay, M5 and M7 transistors play a major role as without them we experience more delay in the computation. When AND gate output is given to subsequent circuits, the capacitors of next circuit will affect its speed. So, the M5 and M7 transistors are important [5] to boost the generation of 1 and due to absence of Vdd in the proposed circuit, in low voltages, these two transistors will play an influential role.

Thus, the high power of swing in both conventional and low voltages, can increase the swing and increase the speed and also the area. The width of both PMOS and NMOS transistors in the proposed AND gate is made to be equal and to minimum allowable value (120 nm).

So, adding up all these points, the overall circuit experiences low energy and power consumption and appropriate speed, the full swing and reasonable noise margin. On the other hand, in the circuit without M5 and M7 will give high speed, lower area but more energy and power dissipation are attained. Even Though the presence of these two transistors occupies more area and give a higher delay the power dissipation is reduced.

Table 1. Working of proposed AND gate

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | **Transistors** | | | | | | | **Output** |
| ***A*** | ***B*** | ***M1*** | ***M2*** | ***M3*** | ***M4*** | ***M5*** | ***M6*** | ***M7*** |  |
| 0 | 0 | OFF | ON | OFF | OFF | OFF | OFF | ON | 0 |
| 0 | 1 | OFF | ON | OFF | OFF | OFF | OFF | ON | 0 |
| 1 | 0 | ON | OFF | ON | ON | OFF | OFF | OFF | 0 |
| 1 | 1 | ON | OFF | ON | ON | OFF | ON | OFF | 1 |

Fig 1. AND gate designed using CMOS logic

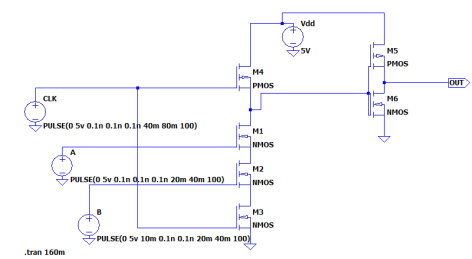
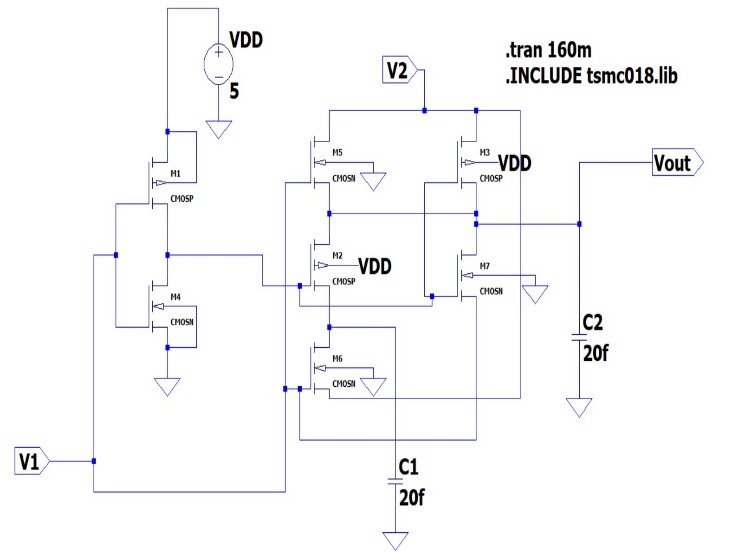
Fig 2. AND gate designed using Pass Transistor logic (PTL)

Fig 3. AND gate designed using Domino logic

*C. Adders in multiplier*

In today’s world as the portable mobile devices are being evolved it is important to design a circuit which satisfies all the requirements such as low power consumption, higher throughput and decreased overall circuit area and low possible delay. These factors are the challenges for the VLSI designers to provide efficient circuits which satisfies all these requirements.

Fig 4. Modified AND gate

In the multiplier circuit, adder circuit forms the major part as that of AND gate and it is considered for modifying as it may influence the major factors of the multiplier circuit. In that adder circuit, basic blocks are XOR-XNOR gates and Multiplexers. So, increasing the performance of the XOR,

XNOR gate and Mux circuits can improve the performance of the adder circuit which adversely affects the performance of the multiplier circuit.

*D. Proposed XOR-XNOR logic*

The XNOR gate exhibits a distinctive structure yielding nearly ideal non-complementary outputs, as illustrated in Figure 2. It performs flawlessly for input combinations of AB=00, 01, and 11. However, when A=1 and B=0, the nMOS transistor turns ON, leading to a weak "HIGH" output signal level, which is deemed inadequate. Nevertheless, this concern can be addressed by adjusting the ratios (W/L) of the MP1 and MN1 transistors until the logic level is restored.

*E. Modified full adder circuit*

The XNOR output is connected to gates M10, M11, M17, and the drain or source of M15. Since M15 is an NMOS, it doesn't fully pass a high logic level. Removing Mx would result in a slight voltage drop in the high mode of XNOR output, equaling Vdd-Vth-PMOS = 1.02V, which is less than 1.2V. Consequently, there wouldn't be any issue in the switching of M10, M11, and M17, which are connected to the gates of XNOR. When M15 is on to conduct the XNOR to the sum output, it wouldn't generate a '1' when AB=11.

Considering AB=11, if Cin=0, M15 would be off, leading to no output path for XNOR due to the voltage drop. In this case, the '0' of the sum is produced in full swing by transistor M17. If Cin=1, M15, M17, and M14 would be on. As M14 is a PMOS, the voltage drop in XNOR output through M15 wouldn't affect the output. AB=11 is crucial, and the XNOR experiences a voltage drop. For other states, the XNOR output is full swing, and there's no need for a PMOS transistor like Mx. Removing Mx would reduce power consumption and circuit area. Then, the input signal A is applied as the most significant bit (MSB) signal of the full adder with less switching activity than other inputs, instead of input B to transistor M12. Consequently, in the MUX Carry stage, by doing this, signal A is applied to transistors, resulting in a full swing output. [14,8].

Therefore, to decrease effective capacitance, prioritize lowering the switching activity of nodes with higher capacitance. This can be achieved by directing signals with lower switching activity to output nodes. Additionally, reduce dynamic power consumption by employing transistors with lower switching activity, such as signal A in the modified AND and XOR-XNOR of the modified full adder, to prevent toggling. Consequently, this minimizes toggle switches and results in a reasonable reduction in power consumption.

In full adders, the carry output typically relies on the sum output, indicating the critical path is formed by the output. Thus, optimizing the carry path enhances circuit efficiency in larger systems. Consequently, the modified circuit integrates Transmission Gates (TG) to minimize short-circuit and static power for XOR-XNOR and the two MUX circuits of Sum and Carry.

The absence of power supply Vdd in its body, combined with strong driving capability and full swing outputs, renders the circuit more power-efficient and faster. Therefore, this modified version resolves the inappropriate driving factor for the chain structure. Moreover, in the modified circuit, balance input capacitances are achieved by adjusting inputs and removing unnecessary transistors.

Sum = ( A ⊕ B ).Cin + (A ⊕ B).Cin

Cout =( A ⊕ B).A + (A ⊕ B).Cin

*F. Delay Considerations*

In terms of delay, the speed of a logic gate depends on various factors such as the number of stages, transistor sizes, and operating conditions. CMOS is a popular logic family used in digital circuits due to its low power consumption and high noise immunity. CMOS logic uses transistors in pairs to create complementary logic gates, which means that one transistor is used to pull the output to a high voltage level while the other transistor pulls the output to a low voltage level. The delay in CMOS logic is typically low to medium, depending on the size of the transistors used. PTL logic has a low transistor count, is a type of logic that uses transmission gates instead of traditional logic gates to control the flow of data. Transmission gates use two complementary MOSFETs to create a switch that can pass or block data. PTL logic has a shorter delay than CMOS logic since the transistors used in transmission gates have a

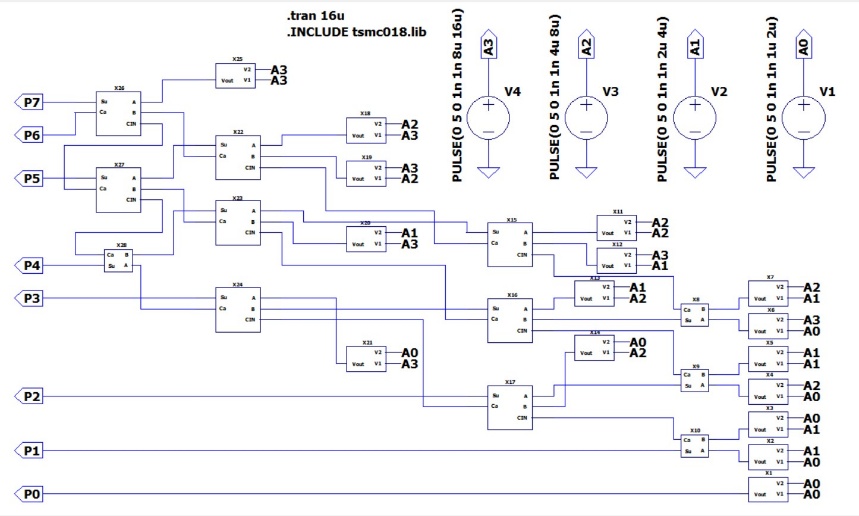
lower resistance than those used in CMOS logic.

Fig 5. Modified full adder circuit

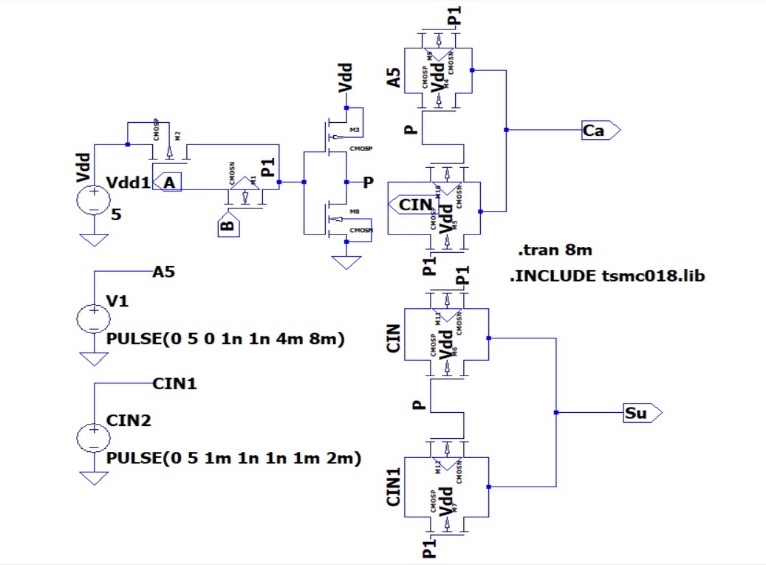
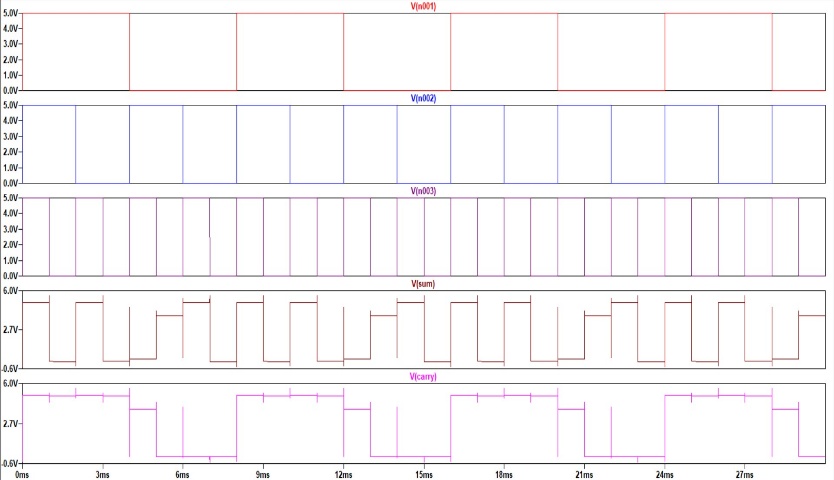
However, PTL logic consumes more power than CMOS logic. Domino logic is a type of dynamic logic that uses precharge and evaluation phases to reduce the delay of the logic circuit. In the precharge phase, the output node is charged to a high voltage level, and in the evaluation phase, the output node is discharged if the input signal satisfies the logic function. Domino logic has a shorter delay than both CMOS and PTL logic since it can operate at a higher clock frequency. However, domino logic consumes more power than CMOS logic and requires careful design to prevent signal glitches. Taking into account both the benefits and drawbacks, the modified PTL-based AND gate employs a floating technique to diminish short-circuit power dissipation. Unlike CMOS AND gates, the suggested gate doesn't include an inverter on its critical path to the output, thereby boosting switching speed.

Table 2. Delay Considerations

|  |  |  |
| --- | --- | --- |
| **Design** | **Delay (ps)** | **Transistors** |
| CMOS | 150 | 6 |
| PTL | 1.2 | 2 |
| DOMINO-LOGIC | 52.84 | 6 |
| PROPOSED | 0.787 | 7 |

Fig 6. Multiplier circuit replaced with modified AND gate and full adder circuit

# SIMULATION RESULTS

Fig 7. Simulated waveform of modified AND gate circuit Fig 8. Simulated waveform of modified full adder circuit

# CONCLUSION

In our study, we have used pass transistor logic (PTL) technology for designing our modified AND gate of the multiplier which offers low latency and power consumption, effective at energy usage, and producing full swing output. And full adder (FA) circuit is designed using the transmission gate and floating technique. In the full adder circuit, the logic of XOR-XNOR circuit is modified by using PTL logic and modifying the width-to-length ratio of transistors to get desired signal to feed into MUX. The MUX circuit is similarly adjusted without a power supply, employing boost transistors to enhance throughput. These modified designs are integrated into both partial product and final product generation in the A x A array multiplier. Test results validate the introduction of a new AND gate utilizing the pass transistor logic (PTL) technique, known for its low power consumption, low latency, efficient energy-saving capabilities, and full-swing output. Additionally, the operational speed of the full adder is enhanced.

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