



Faculty of Engineering & Technology
Electrical & Computer Engineering Department

ENCS 3330

Assignment 2

Prepared by:

Rasha Daoud - 1210382

Instructor:

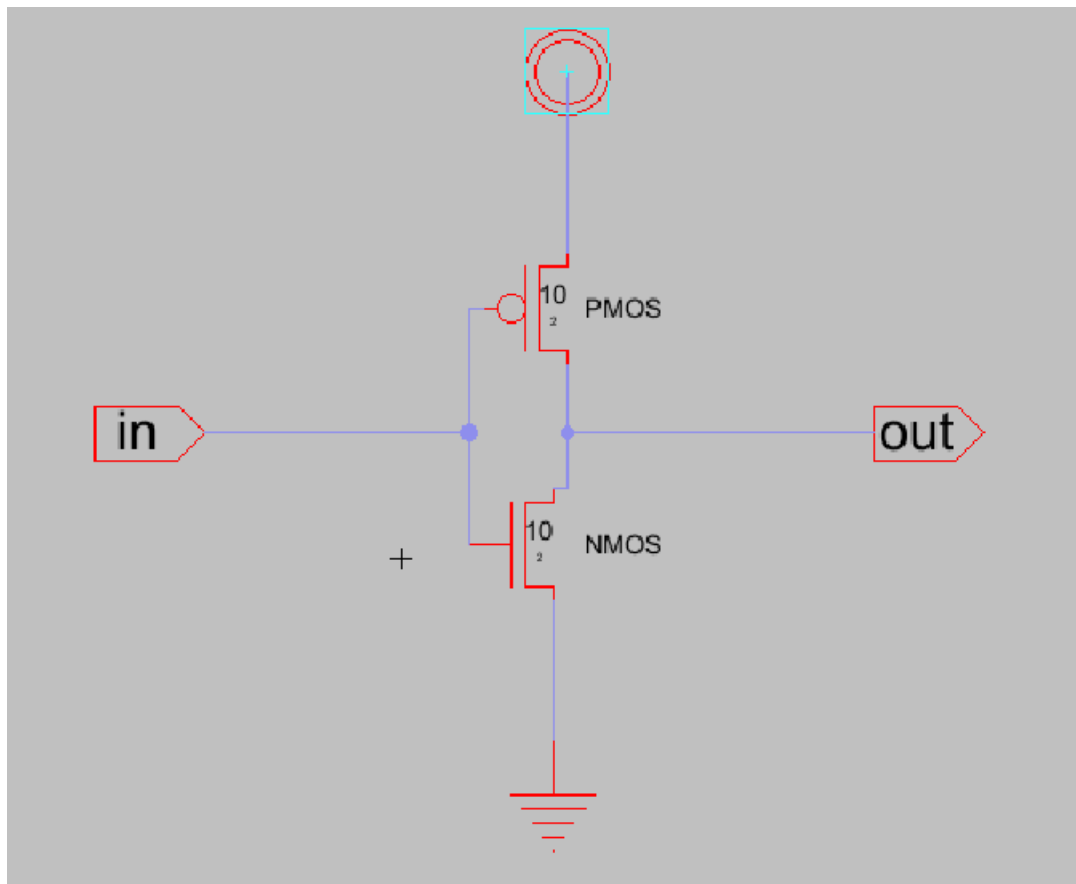
Dr. Khader Mohammed

Section: 2

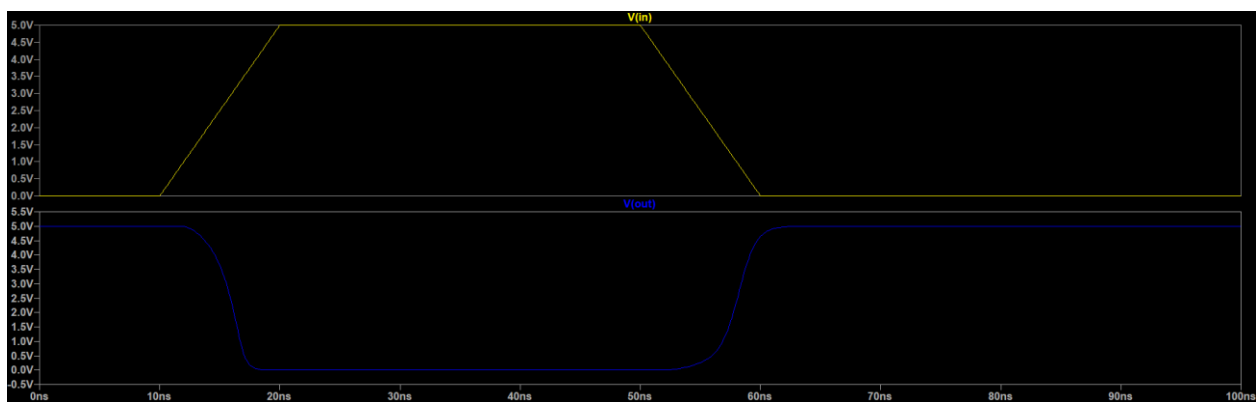
Date: 10 Nov. 2023

Invertor:

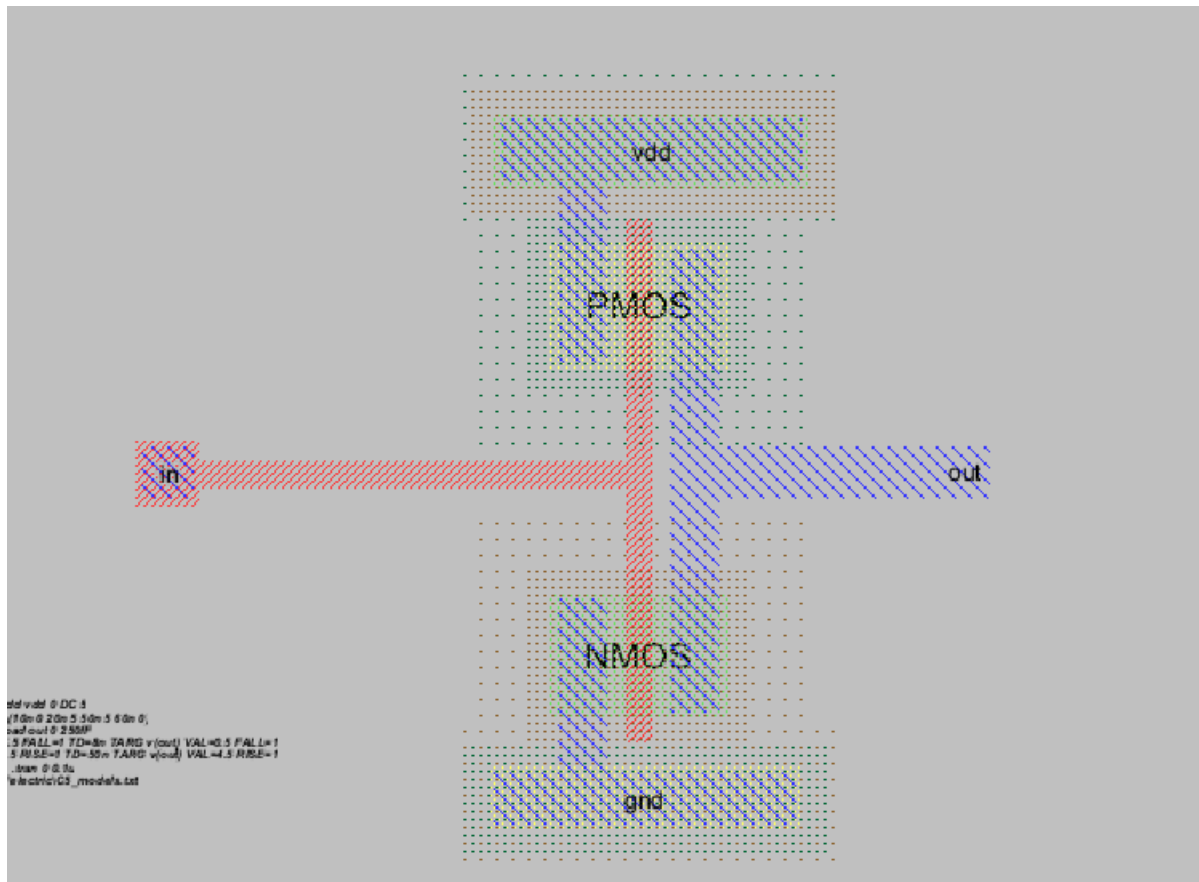
Schematic:



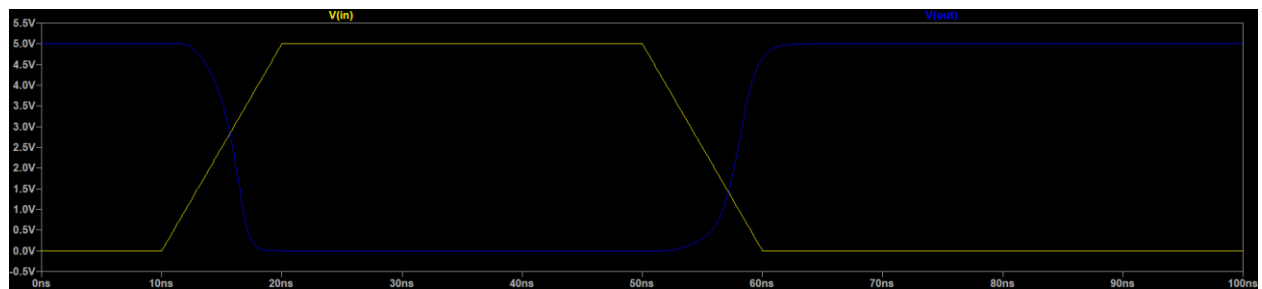
Schematic simulation:



Layout:

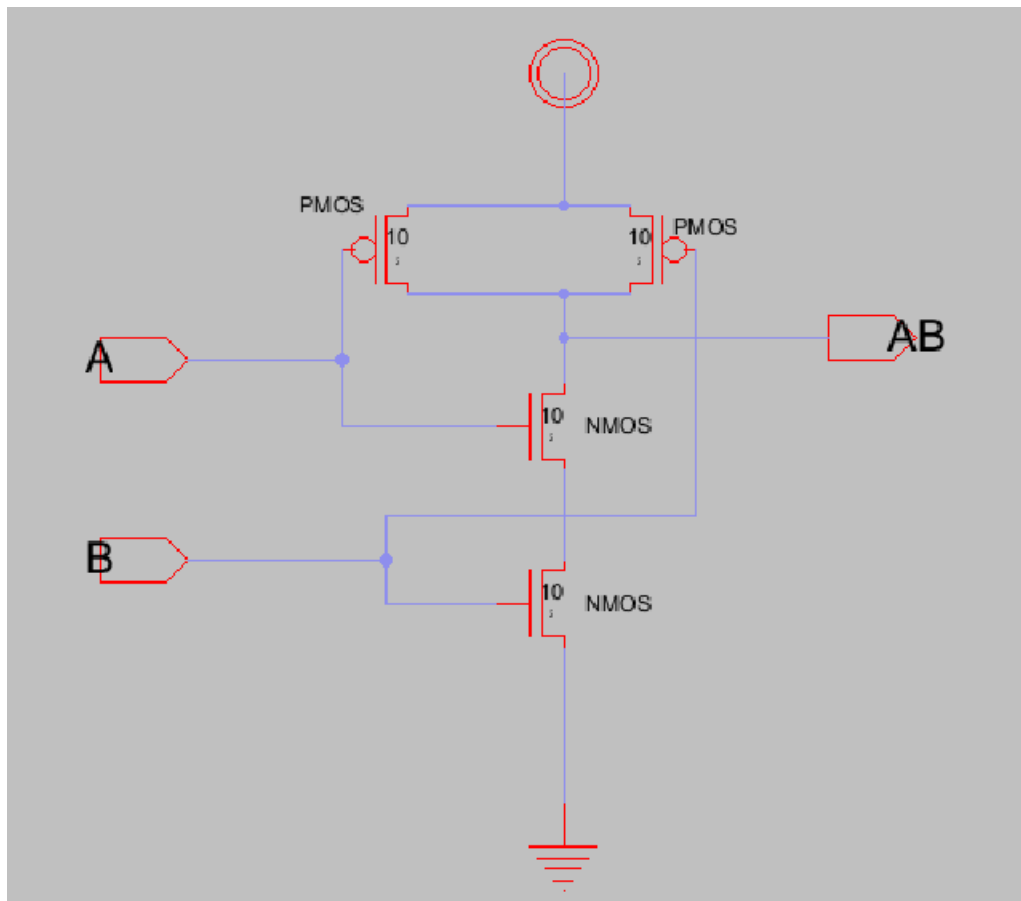


Layout Simulation:

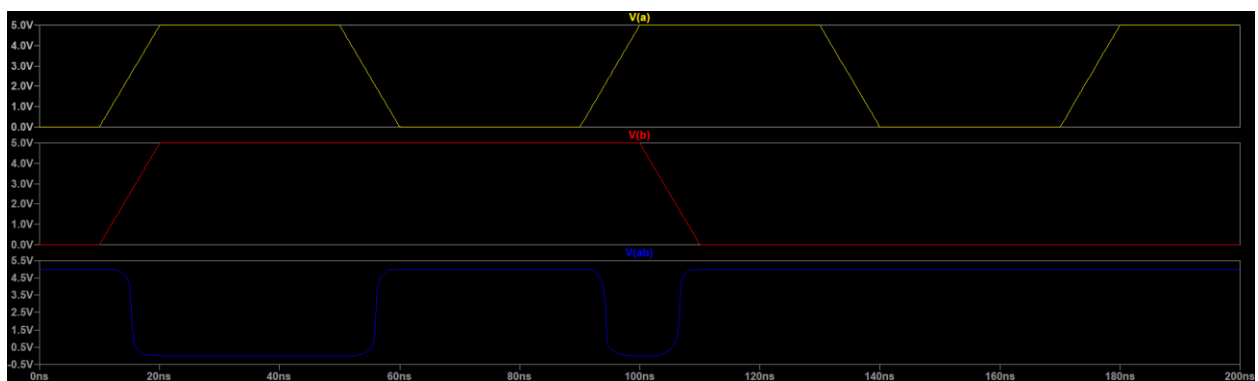


NAND:

Schematic:



Simulation of the schematic:



VDD

PMOS

PMOS

B

AnandB

+

A

NMOS

NMOS

GND

```

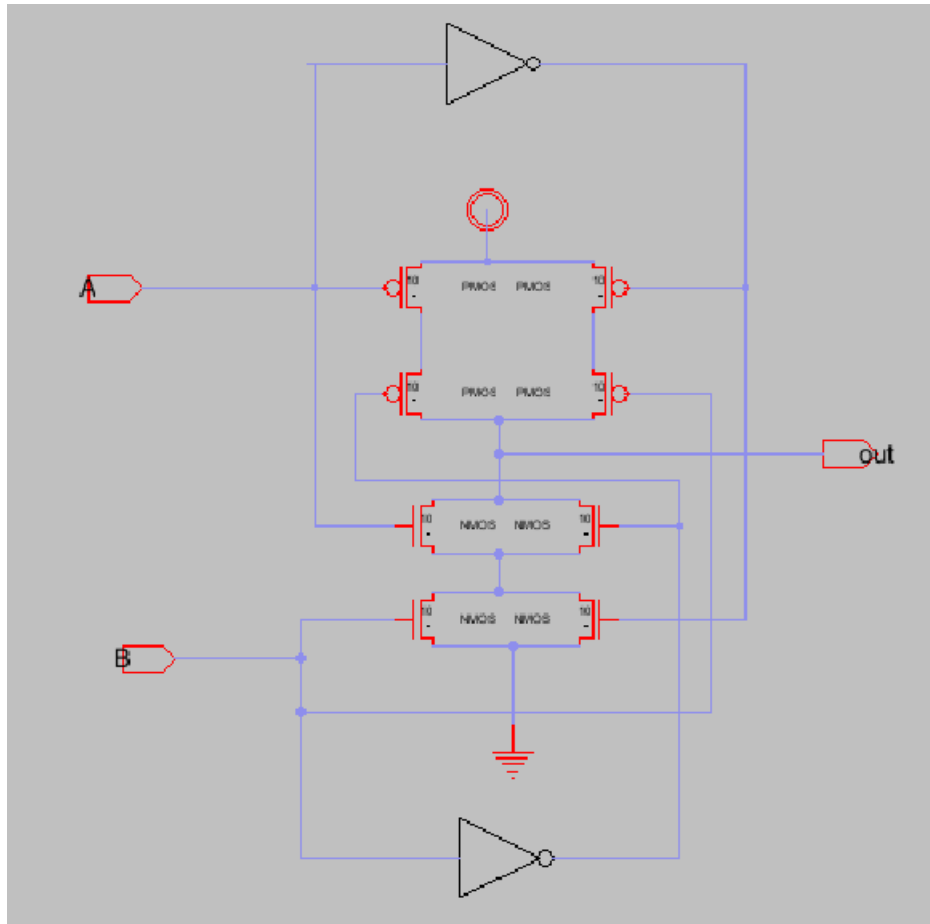
verilog
vdd vdd0DC 5
vaA0 DC pw10n630n550n 540n 0 50n 5 150n 5 140n 0 110n 0 110n 0
vb00 DC pw110n020n510n5 110n 1
measure tran ttrig v(A)and0 yval=4.5 full=1 id=4 n targ v(A)and0 yval=0.5 full=1
measure tran ttrig v(B)and0 yval=0.5 full=1 id=4 n targ v(B)and0 yval=4.5 full=1
1 Jan 2002
./include/C/behavioral/C5_parallel.vcl

```

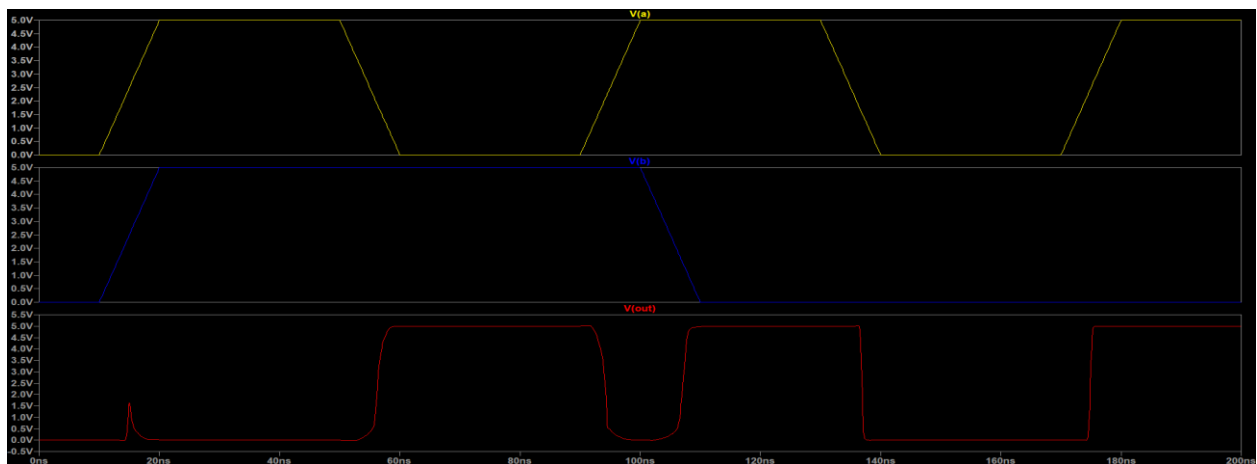
The figure displays three stacked digital waveforms over a 20ns time interval. The top waveform, labeled V(a), is a yellow trapezoidal signal that rises from 0V to 5V at 10ns, stays at 5V until 130ns, and then falls back to 0V. The middle waveform, labeled V(b), is a blue trapezoidal signal that rises from 0V to 5V at 10ns, stays at 5V until 100ns, and then falls back to 0V. The bottom waveform, labeled V(anandb), is a red square wave that is high (5V) from 0ns to 10ns, low (0V) from 10ns to 50ns, high (5V) from 50ns to 100ns, low (0V) from 100ns to 130ns, and high (5V) from 130ns to 200ns.

XOR:

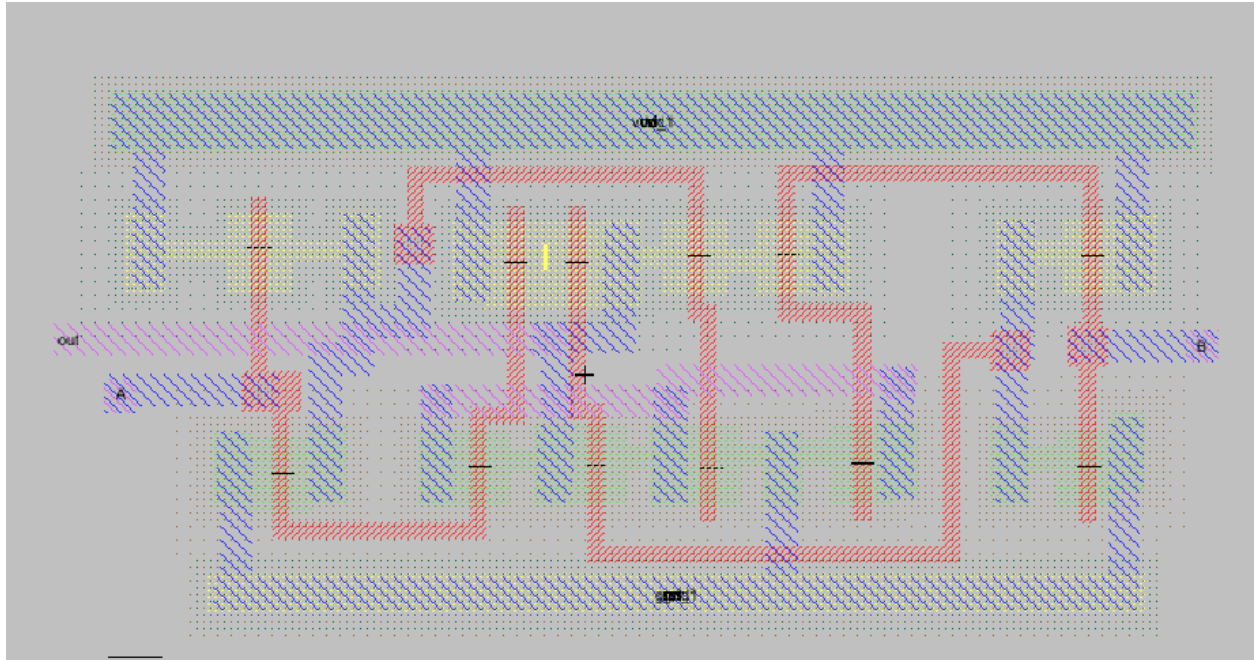
Schematic:



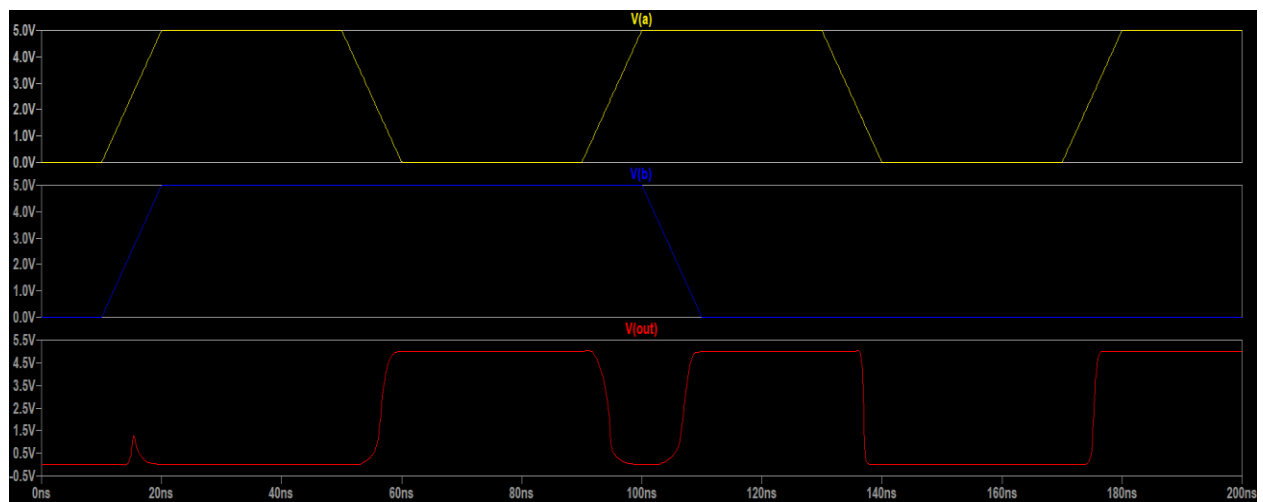
Simulation of schematic:



Layout:

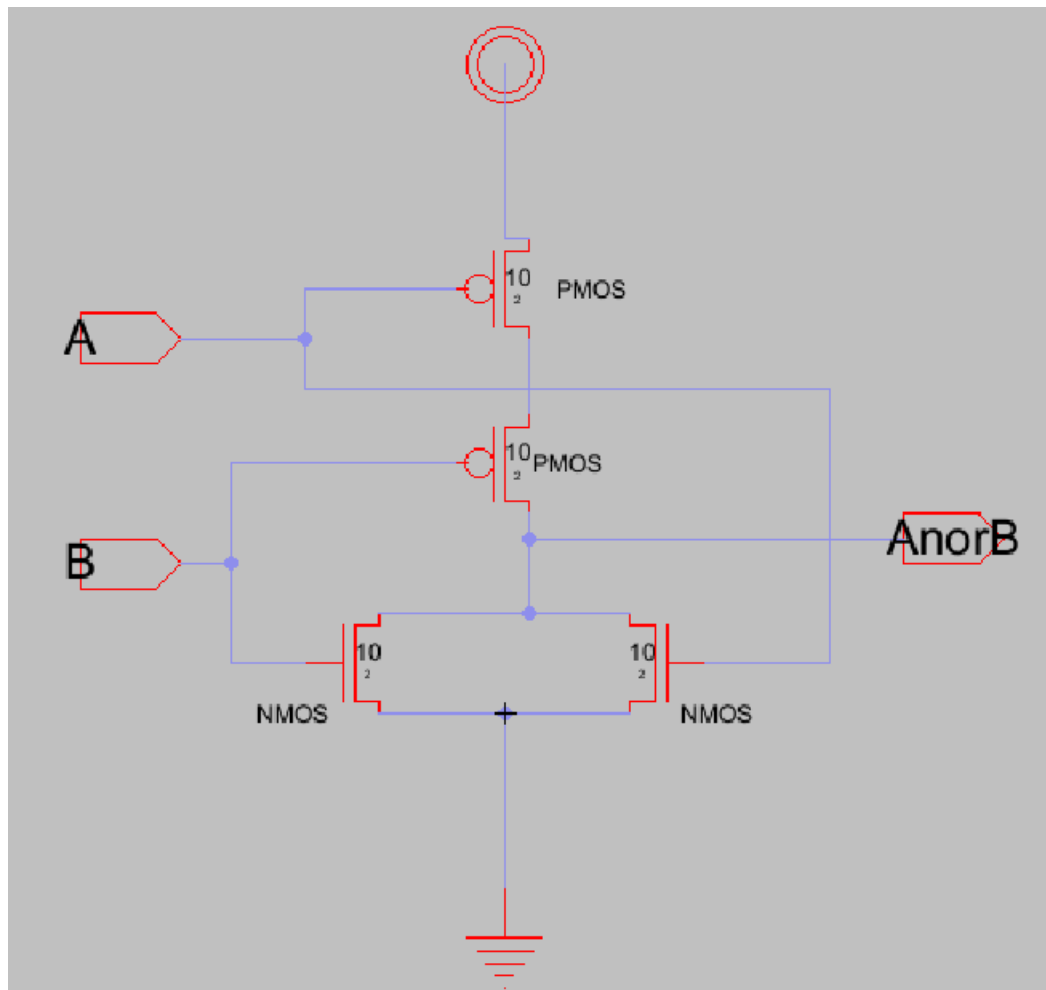


Simulation of Layout:

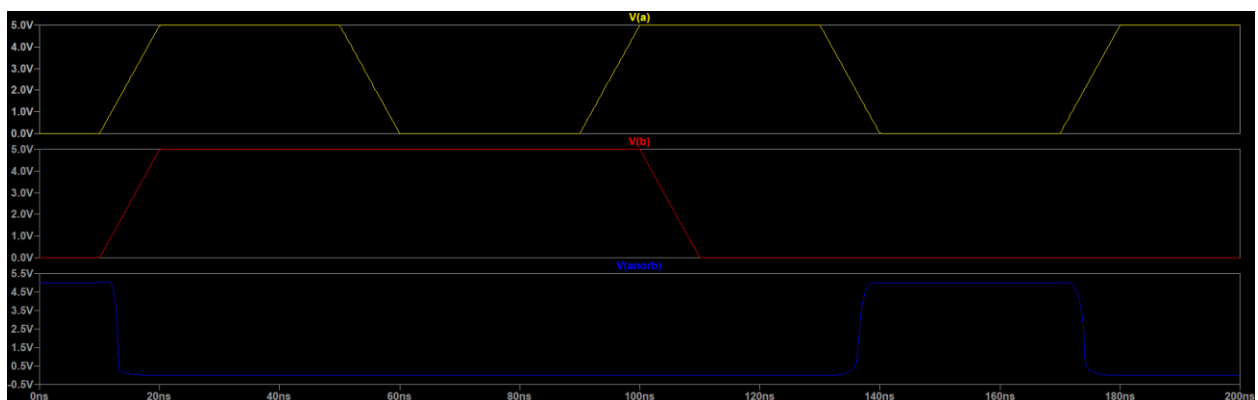


NOR:

Schematic:

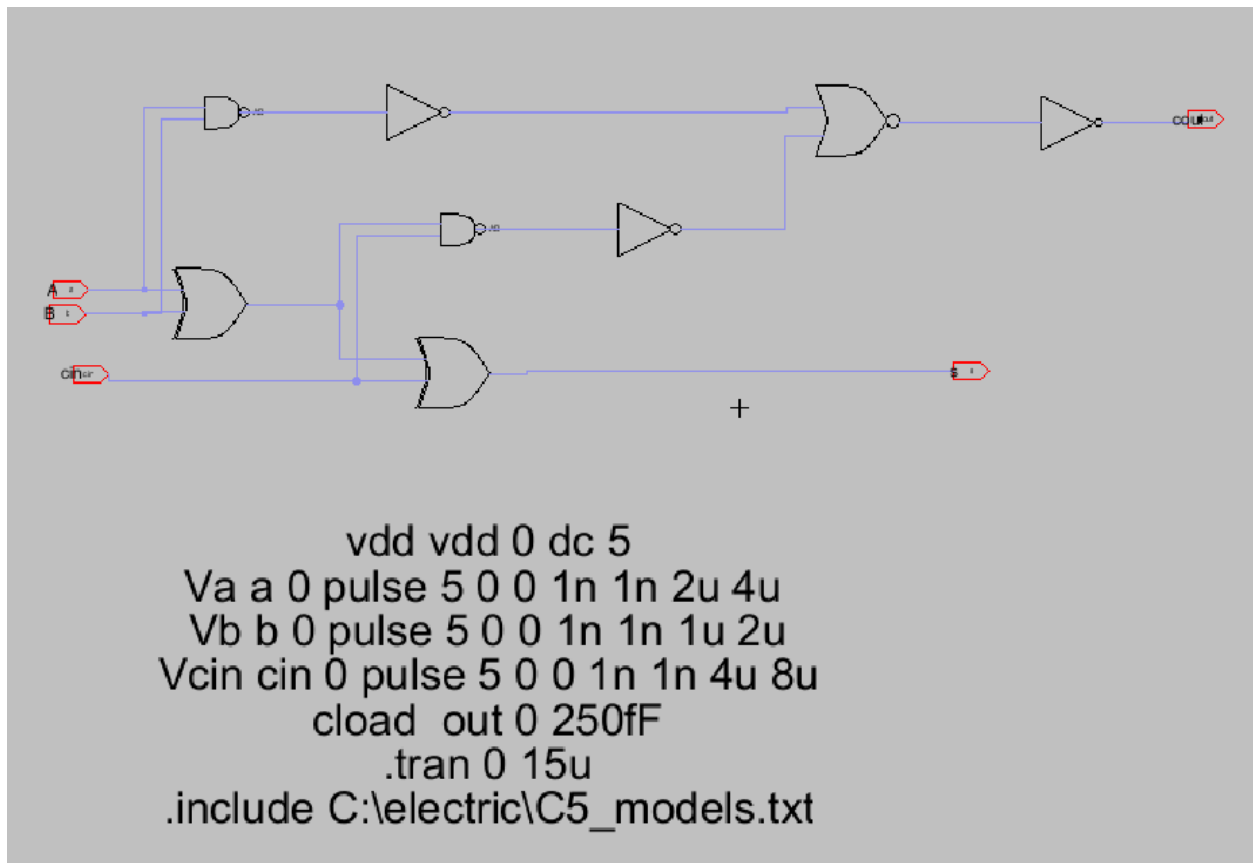


Simulation of the Schematic:

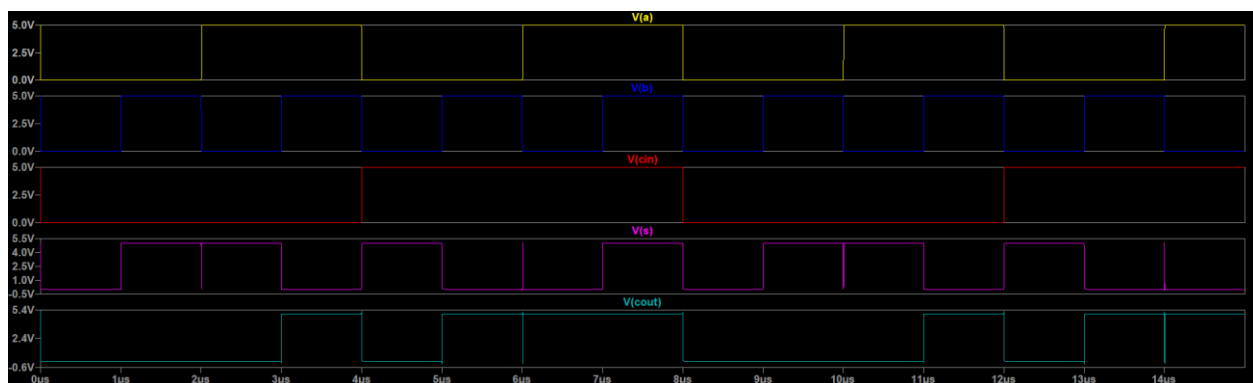


Full Adder:

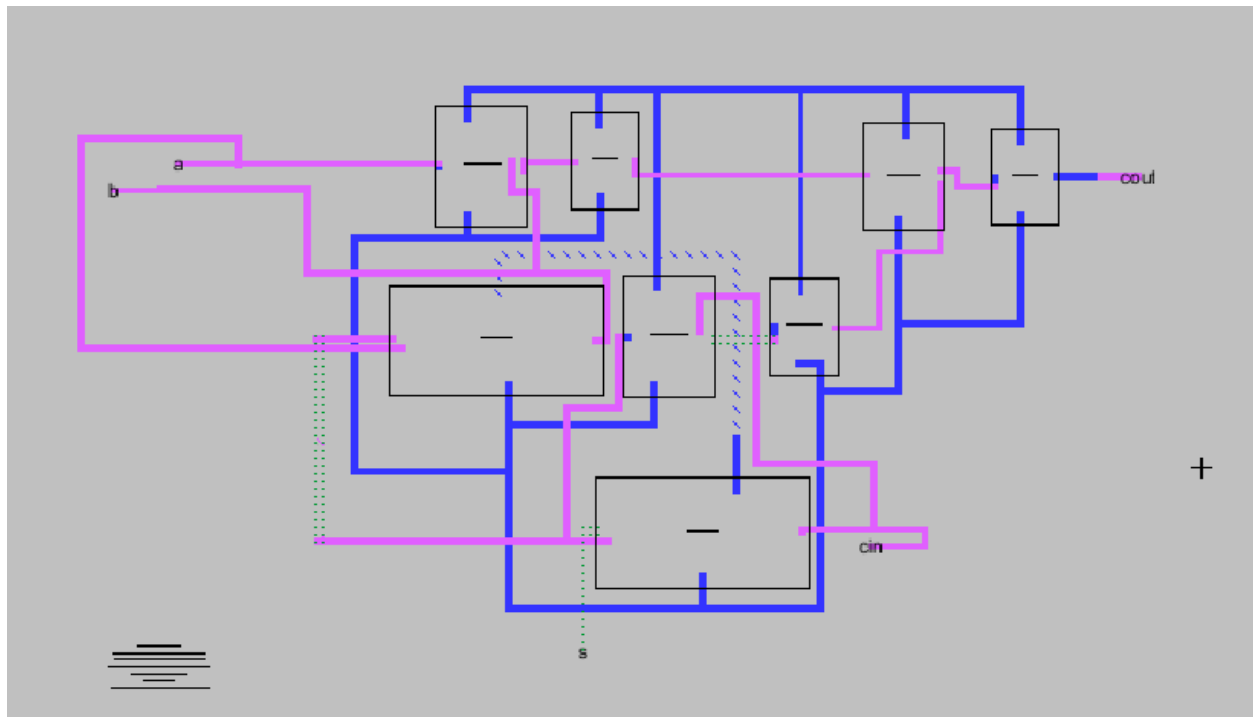
Schematic:



Schematic Simulation:



Layout:



Layout Simulation:

