SHEHZAD RASHEED

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SUMMARY

Electrical and Computer Engineer with 10 years of experience designing and implementing complex embedded systems. Experienced in the complete product development lifecycle, from interpreting requirements and defining functional specifications to delivering robust, high-performance solutions.

HIGHLIGHTS

Areas of Expertise include:

- Digital signal processing.
- Embedded system design.
- FPGA board and firmware design.

Engineering Softwares:

- Xilinx Vivado/ISE, Intel Quartus, Lattice Diamond, Modelsim
- QuestaSim, OrCAD, Microsoft Visual Studio, CCS, Pspice, Jenkins, AVR Studio, Reqtify, Diamond Lattice, Gitlab.

Programming / Scripting Languages:

- **System Verilog/VHDL**, **C++/C**, **Python**, **MATLAB**, **Tcl**.

EXPERIENCE

ABACO Systems | AMETEK, Inc. — **Austin, TX**

- **Senior FPGA Design Engineer** — **Aug 2021 – Current**

  Digital system design for **signal processing** applications (SDR, RADAR, SIGINT).

  FPGA microarchitecture, **RTL** and automated test bench design.

  Develop and execute the validation plan for high bandwidth interfaces.

  Ultra-high sample rate **ADC/ DAC - 64 GSPS**

  Ethernet 1G/10G/40G/100G - JESD204C - Aurora

  Board to board – **JESD204C/Aurora**

  High speed memory interfaces **DDR3/DDR4**

  FPGA planning, ICDs, schematic/code reviews, board bring-up and system integration.

  Customer support for Abaco products integration into systems.

ALSTOM Signaling, Inc. — **Rochester, NY**

- **Hardware Architect** — **Dec 2019 – Aug 2021**

  Development and validation activities for safety-critical onboard railroad systems.

  Development and execution of the environmental/functional/EMC validation plans.

  Execution of FPGA design (VHDL) and validation activities.

  Produce and maintain the electronic design and validation documents

  Define the electronic hardware/FPGA requirements from the system level requirements (Reqtify).

  Execution of change request cycle (CR) and creation of engineering change order (ECO).

  Define serial test procedures and automated test benches; monitor and support the serial production.

Re-Engineering with Research (RWR) **ISB, PAK**

- **Technical Lead** **Jan 2018 – April 2019**

  Design and development of real-time digital communication receivers using FPGA/DSP/ADC.
  Development of hardware and programmable component requirement specifications.
  Design complex digital signal processing algorithms as per requirement specifications
  Design microarchitectures, estimate the resource utilization and power budget.
  Support in the development of real-time embedded systems.
  Develop the automated test benches for the FPGA validation, perform system integration of subsystems.

- **Hardware Design Engineer** **Sep 2014 – Dec 2017**

  Digital signal processing-based algorithm development (MATLAB).
  Development of FPGA and DSP firmware (Verilog/C++) and interfacing with RF components.
  FPGA/DSP design testing using COTS hardware.
  Schematic design, component selections, BOM generation, and pin planning for custom hardware (Cadence OrCAD).
  FPGAs and ADCs based PCB bring-up and hardware testing using RF synthesizers, pulse generators, oscilloscopes, spectrum analyzer, and VNA.
  Board to board link tests, synchronization, and calibration logic development.

PROJECTS

Schematic Designing and PCB Bring Up

Tools: Cadence OrCAD Capture

- Dual FPGA (Kintex-7) schematic design (1500+ component count) with no design iteration needed.
- Ultra-High-Speed Analog to Digital Converter (19.2 Gbps) schematic design.
- Mixed-signal schematic design for the interface of Zynq-7000 evaluation board (Pico Zed) with a custom board.

Digital Signal Processing

Tool: MATLAB

- Researched, and implemented multiple techniques for improvement of frequency resolution with defined latency.
- Designed and implemented sub-Nyquist & Nyquist sampling-based frequency measurement algorithms with defined specifications (SNR, resolution, sensitivity, latency, throughput).
- Designed multi-level custom tracker for multiplexed data.
- Morphological dilation and erosion implementation in MATLAB.
- Fruit sorting and grading algorithm design.

FPGA Firmware Development/Hardware Interfacing

Tools/Language: Xilinx Vivado/ Verilog

- Interfacing Digital Signal Processor with FPGA (KC-705).
- Interfaced ultra-high sampling rate ADC/DAC 64 GSPS with Virtex Ultrascale+ and Versal FPGAs.
- Interfacing single-bit de-multiplexer 12.5 Gbps with FPGA (Artix-7).
- Ethernet (UDP) communication link between FPGA (KC-705) and PC.
- FPGA to FPGA High Speed (Aurora 8b10b) Communication Link (3.125 Gbps).
- Developed a line tracking and hurdles handling robot.

EDUCATION

BS Electrical Computer Engineering |SEP 2010- Sep 2014 |
Comsats IIT Islamabad, Pak.

- CGPA: 3.89/4.00 (**Institute and Campus Gold Medals)**
- Final Project: Fruit Sorting and Grading Machine

MS Electrical Engineering | 2017-|
NUST Islamabad, Pak.

- CGPA: 3.94/4.00
- Major: Digital System and Signal Processing
- Related coursework: Deep Learning in Digital Pathology, Estimation and Detection, Adaptive Filters, ASIC and System Validation

SKILLS

Hardware skills

- Complex high speed real-time embedded systems developments.
- FPGAs firmware development, static timing analysis, synthesis, optimization, debugging, testing.
- PCB schematic designing and board bring up.
- Embedded system interfacing **(SPI, RS232, I2C, PMBUS, EMIF, and AXI).**
- DSP firmware development in **C++.**

Hardware

Field Programmable Gate Arrays (FPGA)
Xilinx: 7 Series, Sparatn-6, Ultra-scale, Ultra-scale plus and Zynq MPSoC
Intel / Lattice: LFE5UM5G-85F, LFE5U-45F

Digital Signal Processors (DSP) / Microcontrollers
TMS320C6416, TMS320C6713, Raspberry Pi Board, AVR Micro controllers

Ultra-High-Speed Analog to Digital Converters (ADC)
AD9081/2, ADC12DL3200, ADC12D1600, ADS8345

Lab Equipment

- Oscilloscope, Pulse Generators (Signal Generators), Frequency Synthesizers, Spectrum Analyzers, Digital Multi Meters (DMM), Network Analyzer

Honors

- Institute Gold Medal (COMSATS IIT).
- Campus Gold Medal (COMSATS IIT).
- Merit scholarships for BS Studies