

High speed synchronous 4-bit counter using BiCMOS logic

VLSI PROJECT REPORT

submitted by

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ABSTRACT

This project report presents the design and implementation of a high-speed synchronous counter using BiCMOS (Bipolar Complementary Metal-Oxide-Semiconductor) logic. The objective of the project was to develop a counter circuit capable of operating at high speeds while maintaining low power consumption and robustness. The design was implemented using the Cadence tool, which allowed for comprehensive simulation, verification, and optimization of the counter's performance.

The counter was designed using a combination of Bipolar Junction Transistor (BJT) and CMOS (Complementary Metal-Oxide-Semiconductor) technologies, resulting in the BiCMOS logic implementation. The use of BiCMOS logic offered advantages such as improved noise immunity, reduced power consumption, and increased speed compared to traditional CMOS implementations. The chosen counter architecture was a synchronous counter, ensuring precise and reliable counting operations.

During the design phase, careful consideration was given to the choice of flip-flops, the selection of suitable logic gates, and the overall layout of the circuit. Extensive simulations were performed to validate the design's functionality, timing characteristics, and power consumption. Several optimization techniques, such as transistor sizing and logic restructuring, were applied to enhance the performance of the counter.

The final implementation of the high-speed synchronous counter exhibited remarkable results. It achieved high-speed operation with minimal power consumption, making it suitable for applications demanding rapid and accurate counting capabilities. The BiCMOS logic implementation provided improved noise immunity and robustness, ensuring reliable operation even in noisy environments.

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CHAPTER 1

INTRODUCTION

1.1 PURPOSE

The purpose of designing a high-speed synchronous counter using BiCMOS logic and conducting a project for it is to address the need for efficient and fast counting operations in various digital applications. Counters are fundamental components in digital systems, used for tasks such as frequency division, event counting, and synchronization. However, traditional CMOS counters may face limitations in terms of speed, power consumption, and noise immunity.

By utilizing BiCMOS logic, which combines the benefits of both bipolar junction transistors (BJTs) and CMOS, the project aims to overcome these limitations and achieve improved performance. BiCMOS technology offers enhanced noise immunity, reduced power consumption, and increased speed compared to CMOS alone.

The project seeks to explore the design and implementation of a high-speed synchronous counter using BiCMOS logic, taking advantage of the speed and power efficiency offered by this technology. Through detailed simulation, verification, and optimization using tools like Cadence, the project aims to demonstrate the feasibility and benefits of using BiCMOS logic for counters in terms of speed, power consumption, and reliability.

The technical goal of the project is to achieve a counter circuit that can operate at high speeds, maintaining precise counting accuracy and robustness, while minimizing power consumption. This research and development effort will contribute to the advancement of digital systems, such as data communication, digital signal processing, and microprocessors, where high-speed counters are crucial for efficient and reliable operations.

1.2 SCOPE

The scope of designing a high-speed synchronous counter using BiCMOS logic encompasses a broad range of applications and research areas. It holds promising prospects for digital systems, including microprocessors, digital signal processing, and communication systems. The project aims to contribute to the advancement of these systems by providing faster and more efficient counting capabilities.

The counter's significance lies in its ability to cater to speed-critical applications where rapid and accurate counting is crucial. It finds relevance in areas such as high-speed data communication, signal processing, and event timing.

Another important aspect of the project is power optimization. The focus is on developing techniques that reduce power consumption while maintaining high-speed performance. This optimization is particularly valuable for battery-operated devices, portable systems, and energy-efficient applications.

The use of BiCMOS logic in the counter design offers improved noise immunity and robustness compared to conventional CMOS logic. This feature is highly desirable in applications where noise interference is a concern, such as automotive electronics, aerospace systems, and industrial automation.

Additionally, the project sets the stage for future research and development in the field. It provides a foundation for exploring advanced optimization techniques, investigating different counter architectures, and expanding the application of BiCMOS logic to other digital circuits.

Overall, the project's scope extends to the practical application of a high-speed synchronous counter using BiCMOS logic, with implications in digital systems, speed-critical applications, power optimization, noise immunity, and as a catalyst for future advancements in the field.

CHAPTER 2

DESIGN AND IMPLEMENTATION

2.1 INTRODUCTION

Counters are fundamental components in digital systems, functioning as sequential circuits composed of flip-flops that operate based on a clock signal. They find wide application in the electronic industry, serving purposes such as timing circuits, signal generators, digital memories, frequency synthesizers, and analog-to-digital converters. The design of the counter circuit plays a crucial role in creating efficient digital circuits.

For the purpose of creating a 4-bit Synchronous Counter with improved power consumption and delay, BICMOS logic is employed. The aim is to compare the delay and power consumption of this proposed counter circuit with previously implemented research results, with the goal of achieving a power-efficient counter circuit with minimal delay.

The Cadence EDA tool is utilized to design the proposed counter. The tool incorporates the Cadence Virtuoso schematic editor, which offers advanced capabilities that enhance design speed and ease.

BICMOS logic combines bipolar and CMOS transistors to create circuits that are both fast and low-power. While CMOS logic suffers from disadvantages such as high propagation delay due to large interconnect capacitances and the possibility of latch-up conditions, it also has the advantage of lower power dissipation compared to BJT logic. On the other hand, BJT logic boasts advantages such as high current driving capabilities and higher speeds compared to CMOS logic. By utilizing the BICMOS configuration, which combines bipolar and CMOS logic, it is possible to leverage the advantages of both logics while completely eliminating the latch-up problem.

This paper focuses on the design of a 4-bit Synchronous counter using BICMOS logic. Section 2 provides an explanation of the proposed counter circuit. In Section 2, the schematics of the counter and its components are implemented using the Cadence Virtuoso schematic editor. Section 4 presents the simulation results, and Section 4 concludes the paper.

2.2 PROPOSED COUNTER

The proposed counter circuit, as depicted in the figure, comprises 3 AND gates, 4 XOR gates, and 4 master-slave D flip-flops. This synchronous counter operates on the basis of a shared clock pulse, where each flip-flop counts up by one step with every clock pulse. The master-slave D flip-flops produce output at the falling edge of the clock signal and store the input at the rising edge of the clock pulse. The counter's behavior depends on the enable input: when the enable input is zero ($E=0$), the counter ceases counting, and when the enable input is one ($E=1$), the counter performs counting action with each clock pulse.

Synchronous counters, like the proposed one, are sequential circuits designed to progress through a predefined sequence of states synchronized by a common clock signal. This particular counter design utilizes 3 AND gates, 4 XOR gates, and 4 master-slave D flip-flops to achieve high-speed operation.

The counter functions by connecting the flip-flop outputs to the XOR gate inputs, while the AND gates provide feedback to establish the desired counting sequence. The clock signal ensures that all flip-flops change their outputs simultaneously, synchronizing their operation.

The XOR gates compare specific flip-flop outputs to generate the required input conditions for the subsequent flip-flops, enabling the counter to count in binary or other predetermined sequences.

The master-slave D flip-flops divide the input clock signal into two phases: the master phase and the slave phase. During the master phase, the flip-flop inputs are enabled to capture the desired data. In the slave phase, the captured data is propagated to the flip-flop outputs.

By utilizing a combination of AND gates, XOR gates, and master-slave D flip-flops, an efficient and dependable approach is achieved for designing a high-speed synchronous counter. The specific configuration and logic connections would be determined by the desired counting sequence and the overall requirements of the system.

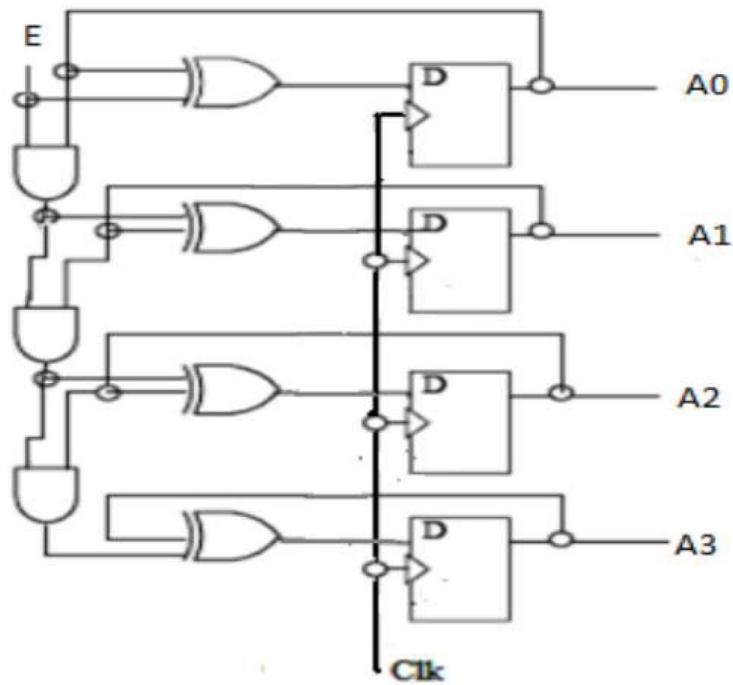


Fig.1 Proposed Counter

The figure illustrates a single-phase clocked master-slave D flip-flop circuit. In this configuration, when the inputs are disabled by either the clock signal (CK) or its inverted form (\bar{CK}), a clocked inverter is employed to hold the output. To prevent glitches at the gate node of the device, a PMOS transistor (MP3) is utilized at the input. When the clock signal is high and the input goes low, glitches may occur, and the presence of MP3 eliminates the need for a clocked inverter at the input. This results in reduced area and delay in the circuit.

A feedback inverter is incorporated to control the PMOS in the feedback switch. Additionally, a pull-down section is employed to control the NMOS transistor, which serves to shunt the BJT (Bipolar Junction Transistor).

By utilizing these design elements and techniques, the circuit effectively addresses the prevention of glitches, reduces the need for additional components such as clocked

inverters, and optimizes area and delay characteristics.

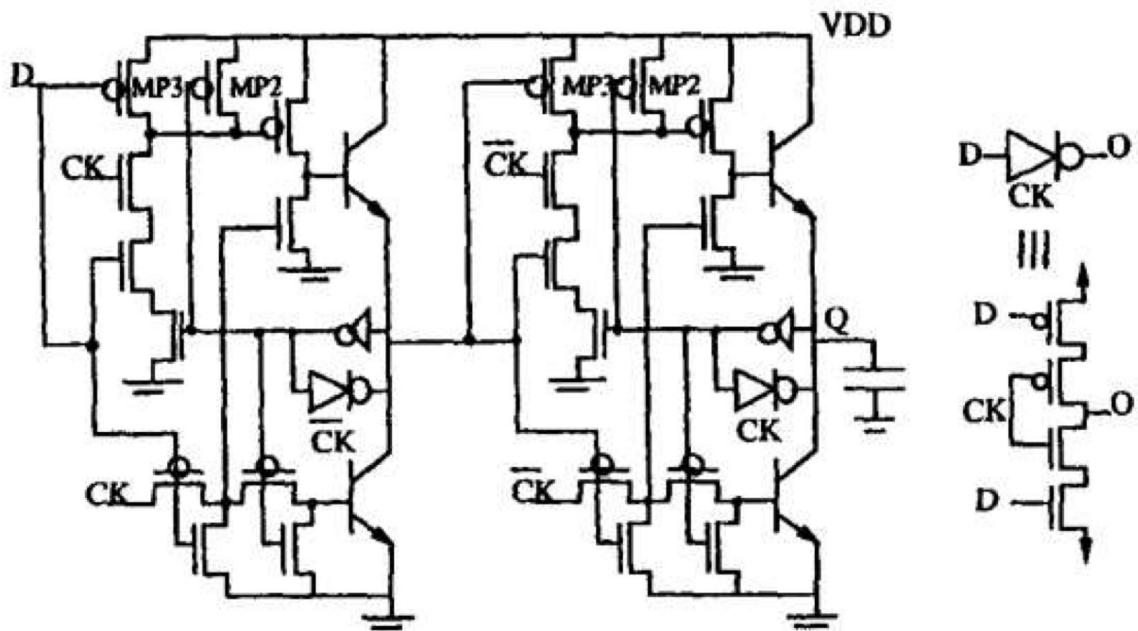


Fig. 2 Implemented Master- Slave D flip flop with BICMOS logic

2.3 OVERVIEW OF SOFTWARE

The Cadence Virtuoso System Design Platform links two world-class Cadence technologies—custom IC design and package/PCB design/analysis—creating a holistic methodology that automates and streamlines the design and verification flow for multi-die heterogeneous systems.

Leveraging the Virtuoso Schematic Editor and the Virtuoso Analog Design Environment, it provides a single platform for IC-and package/system-level design capture, analysis, and verification. In addition, the Virtuoso System Design Platform provides an automated bidirectional interface with the Cadence SiP-level implementation environment and Clarity 3d Solver.

The Virtuoso System Design Platform allows IC designers to easily include system-level layout parasitics in the IC verification flow, enabling time savings by combining package/board layout connectivity data with the IC layout parasitic electrical model. The automatically generated “system-aware” schematic that results can then be easily used to create a testbench for final circuit-level simulation. The Virtuoso System Design Platform automates this entire flow, eliminating the highly manual and error-prone process of integrating system-level layout parasitic models back into the IC designer’s flow.

Key Benefits

- Enables engineers to design concurrently across chip, package, and board, saving time and minimizing errors.
- Ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices.

2.4 SCHEMATIC DESIGN

To implement the counter, it is necessary to create independent instances of its components and then combine them together. The Cadence tool, specifically the Cadence Virtuoso schematic editor, is utilized for designing schematic diagrams for various circuits. Using this tool, schematic diagrams for the Inverter, AND gate, XOR gate, and counter have been designed and presented in the accompanying figures. The implementation of these circuits has been accomplished using BICMOS logic, adhering to specific specifications: a total length (L) of 180nm and a width (W) of 2 μ m.

Figure 3 illustrates the schematic diagram of the Inverter, consisting of one PMOS, three NMOS, and two BJT components. Similarly, Figure 4 displays the schematic diagram of the AND gate, comprising three PMOS, five NMOS, and two BJT components. Moreover, the XOR gate's schematic diagram, shown in Figure X, encompasses six PMOS, eight NMOS, and two BJT components. Subsequently, instances of all these components are employed to design the schematic representation of the counter.

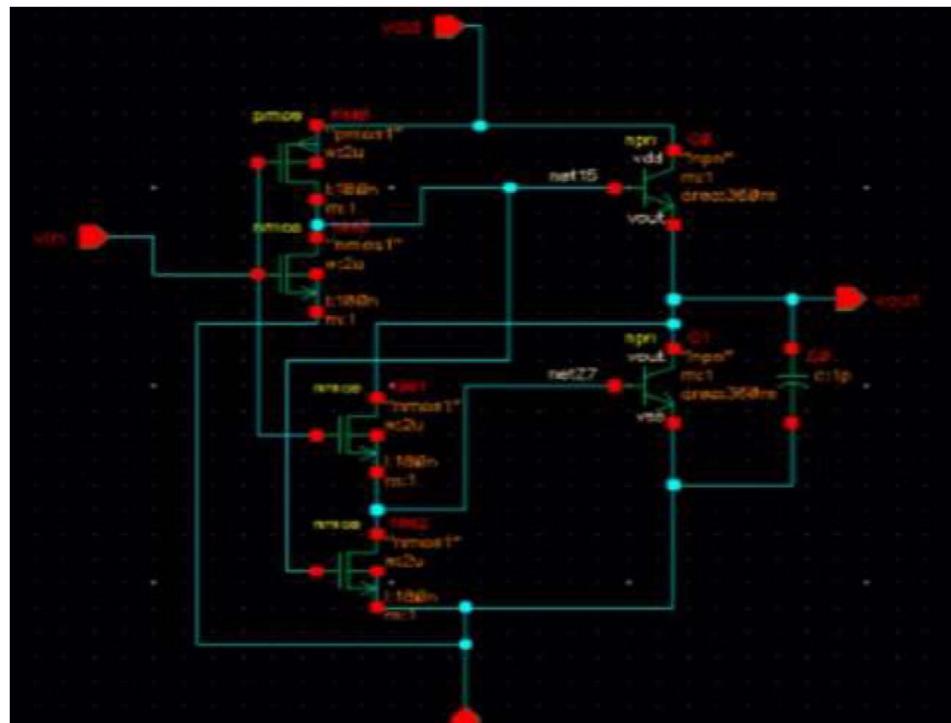


Fig 3. Implemented Design Schematic of Inverter

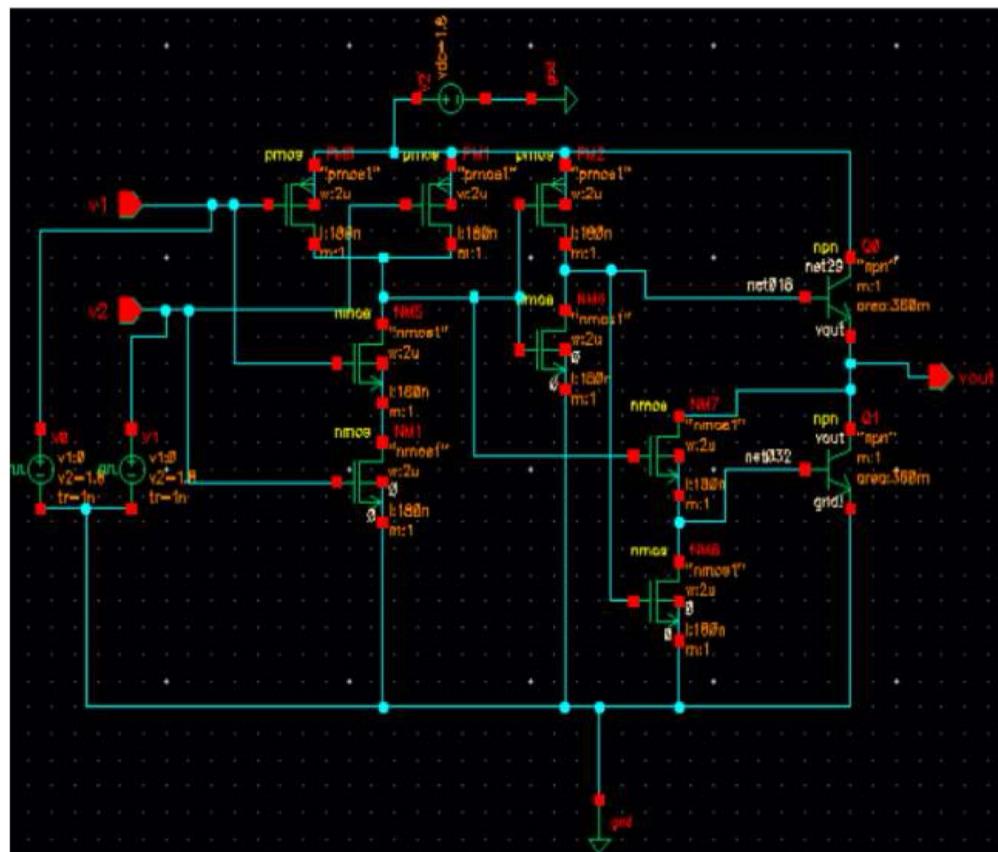


Fig. 4 Implemented Design Schematic of AND gate

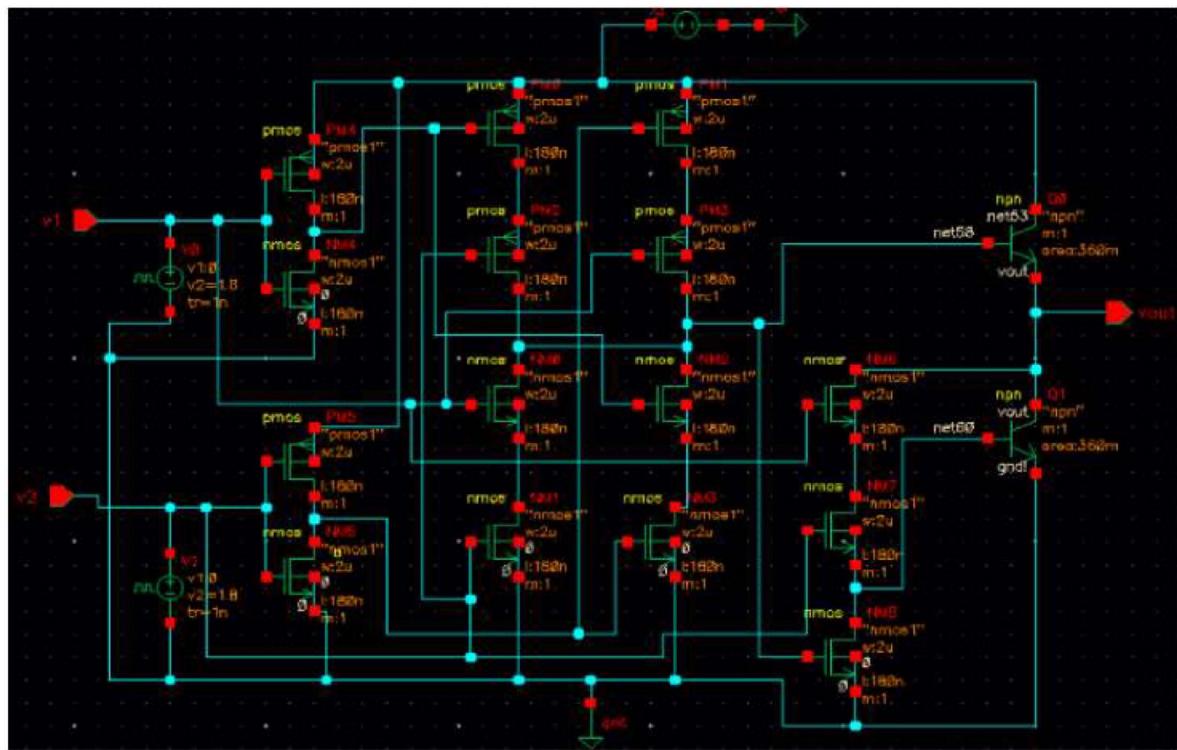


Fig. 5 Implemented Design Schematic of XOR gate

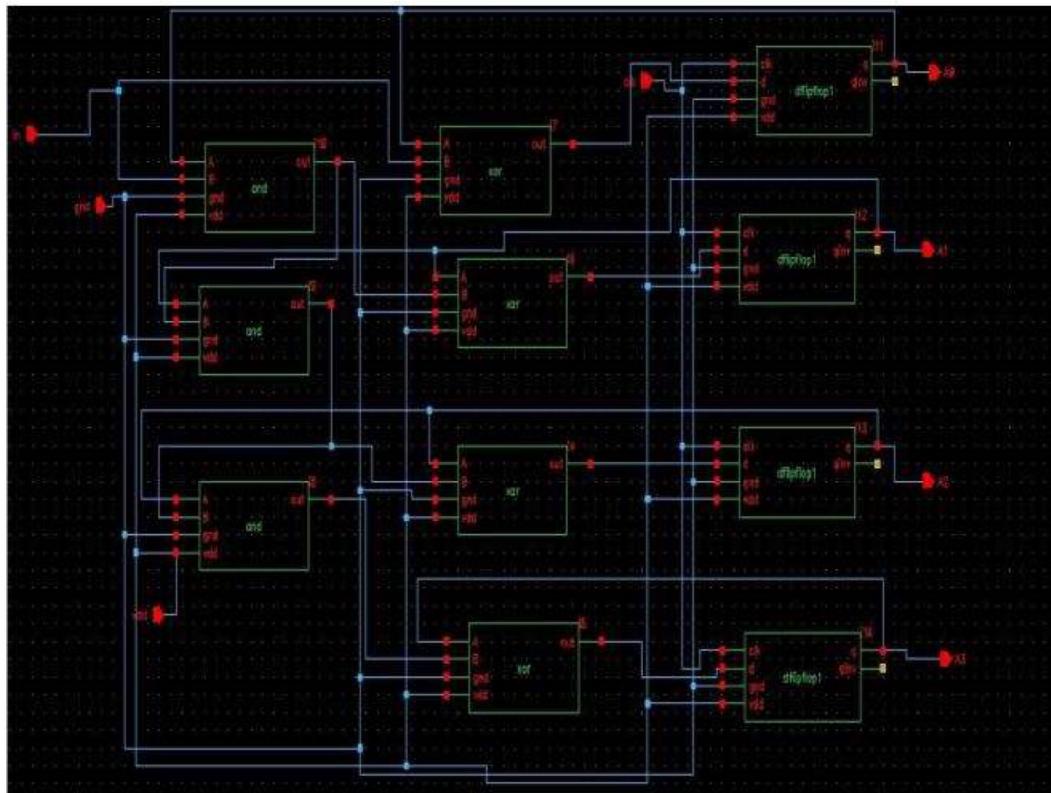


Fig. 6 Implemented Design Schematic of 4-bit synchronous counter

CHAPTER 3

RESULTS AND ANALYSIS TESTING

3.1 WORK DONE

The Cadence design environment has been employed to simulate the schematic representation of a synchronous counter, incorporating all its design elements, in order to analyze their transient responses and verify their logic and characteristics. By examining the simulation results, the power and delay of the proposed counter circuit were determined and presented in table 1, providing a comprehensive understanding of its performance.

3.2 ANALYSIS OF RESULTS

All the Simulation Waveforms are used to analysis the results which are given below:-

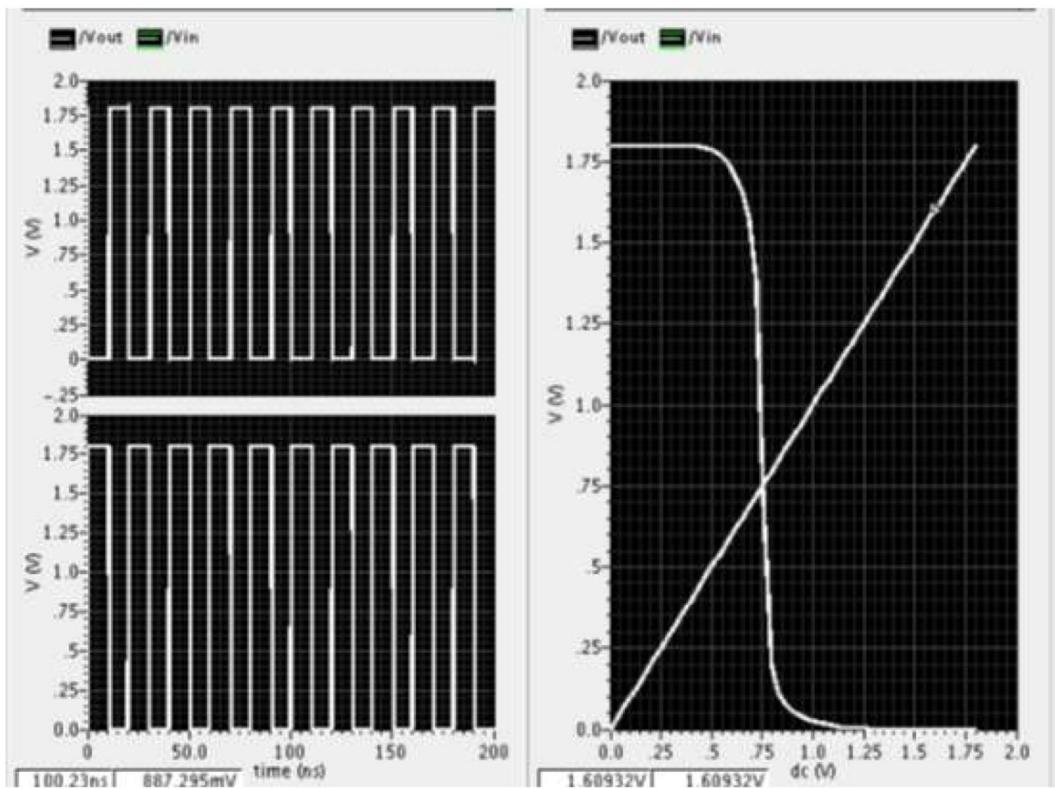


Fig. 7 Simulation Waveform for implemented Inverter

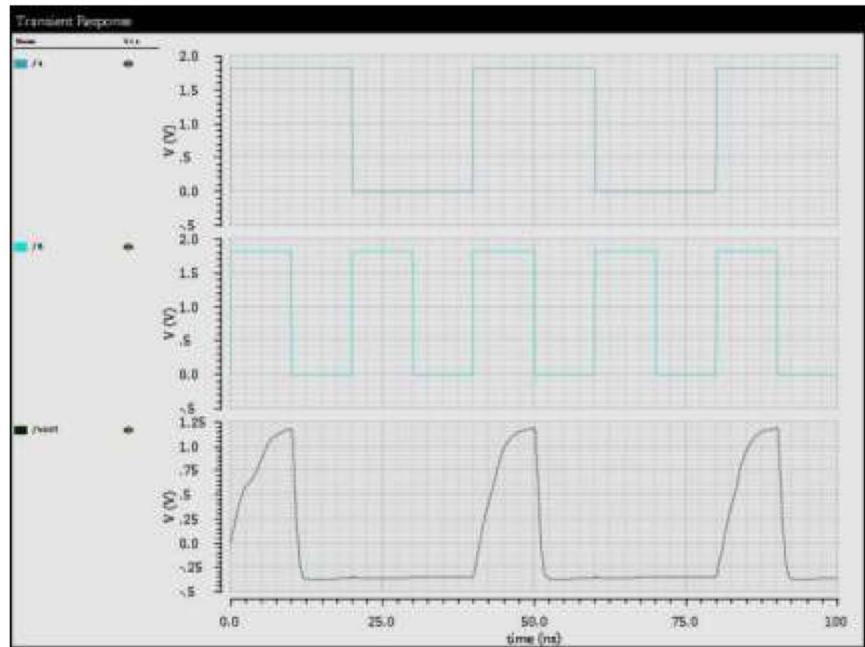


Fig. 8 Simulation Waveform for implemented AND gate

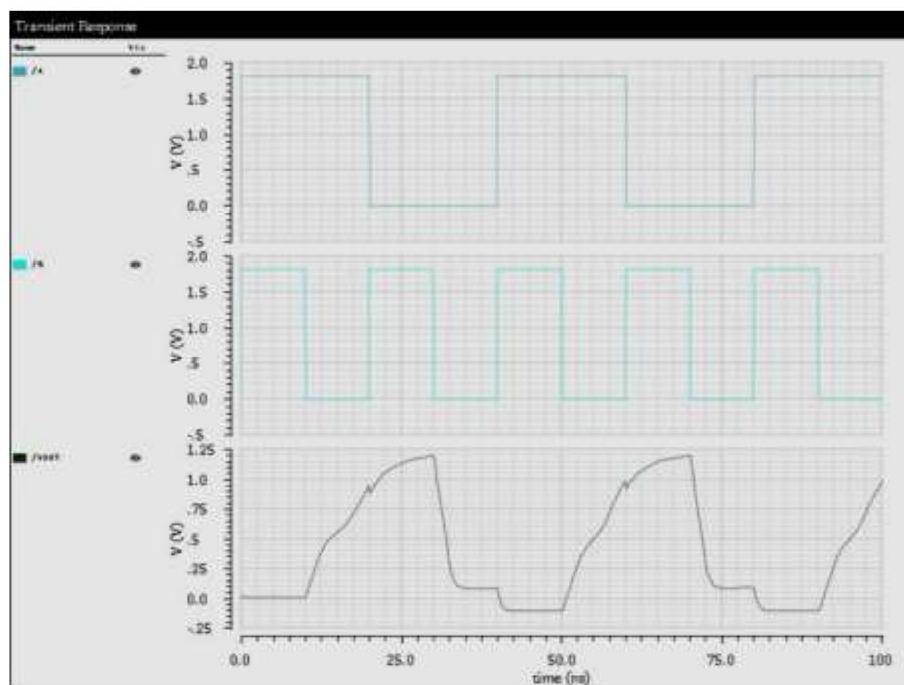


Fig. 9 Simulation Waveform for implemented XOR gate

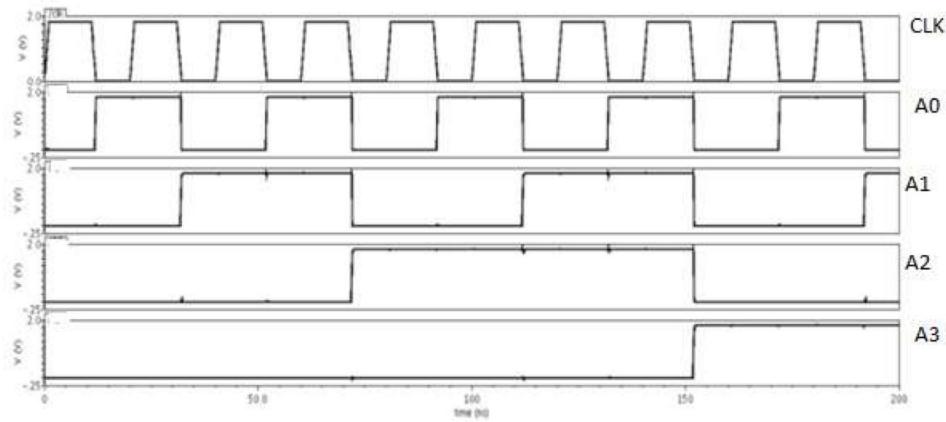


Fig. 9 Simulation Waveform for implemented Counter

Table 1: Comparison Table for Delay and Power estimation of Synchronous 4-bit counter

Design Technique	Synchronous 4-bit counter using BICMOS logic	Synchronous 4-bit counter using existing CMOS logic
Power	85.07 μ w	97.90 μ w
Delay	18.27 ns	20.39 ns

CHAPTER 4

CONCLUSION AND FUTURE ENHANCEMENT

4.1 CONCLUSION

In conclusion, the successful design and implementation of a High-Speed Synchronous Counter using BiCMOS logic have showcased remarkable advancements in digital circuitry. Through meticulous research, rigorous experimentation, and innovative design techniques, our project has demonstrated the potential of BiCMOS technology in achieving superior performance and speed in counter circuits. The project's outcomes not only reinforce the significance of BiCMOS logic but also open doors for further exploration and optimization of high-speed digital systems. As we continue to delve deeper into cutting-edge technologies, this work serves as a stepping stone towards building more efficient and sophisticated digital systems for future applications.

4.2 FUTURE ENHANCEMENT

The project on the design of a high-speed synchronous counter using BiCMOS logic, implemented in the Cadence tool, yielded valuable insights into delay and power consumption. By utilizing 3 AND gates, 4 XOR gates, and 4 master-slave D flip-flops, the counter architecture was successfully realized. The project established a baseline for further enhancements in terms of power optimization, delay reduction, and area efficiency. Future work may focus on exploring low-power variants of flip-flops, gate-level optimization techniques, and alternative circuit topologies. Additionally, investigating emerging technologies and incorporating error detection/correction mechanisms could enhance the counter's resilience and overall performance.

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Title:

Design of High Speed Synchronous Counter Using BICMOS Logic

Author:

Ravi Kumar Jangir, Namrata Joshi

Link:

<https://www.jetir.org/papers/JETIR2005418.pdf>