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[ACNW3190-000E](#)

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# ACNW3190

## 5.0 Amp High Output Current IGBT Gate Drive Optocoupler



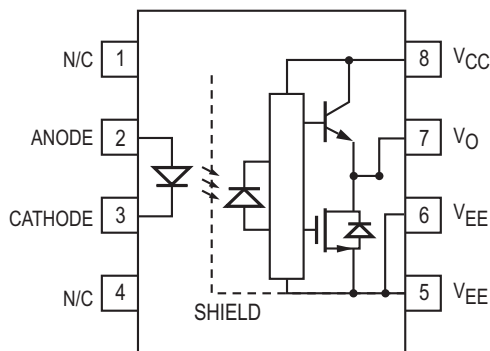
### Data Sheet



#### Description

The ACNW3190 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBTs with ratings up to 1200V/200 A, 600 V/300 A. For IGBTs with higher ratings, the ACNW3190 can be used to drive a discrete power stage which drives the IGBT gate. The ACNW3190 has the highest insulation voltage of  $V_{IORM}=1414 V_{peak}$  in the IEC/ EN/DIN EN 60747-5-2.

#### Functional Diagram



#### TRUTH TABLE

LED	$V_{CC} - V_{EE}$ "POSITIVE GOING" (i.e., TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (i.e., TURN-OFF)	VO
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSI- TION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1  $\mu$ F bypass capacitor must be connected between pins 5 and 8.

#### Features

- 5.0 A Maximum Peak Output Current
- 15 kV/ $\mu$ s Minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500 V$
- 0.5 V Maximum Low Level Output Voltage ( $V_{OL}$ ) Eliminates Need for Negative Gate Drive
- $I_{CC} = 5$  mA Maximum Supply Current
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- Wide Operating  $V_{CC}$  Range: 15 to 30 Volts
- 500 ns Maximum Switching Speeds
- Industrial Temperature Range:  $-40^{\circ}C$  to  $100^{\circ}C$
- Safety Approval

#### UL Recognized

5000  $V_{rms}$  for 1 min.

#### CSA Approval

IEC/EN/DIN EN 60747-5-2 Approved

$V_{IORM} = 1414 V_{peak}$

#### Applications

- IGBT/MOSFET Gate Drive
- AC/Brushless DC Motor Drives
- Industrial Inverters
- Switch Mode Power Supplies

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Ordering Information

ACNW3190 is UL Recognized with 5000Vrms for 1 minute per UL1577.

Part number	Option	Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant						
ACNW3190	-000E	400mil DIP-8				X	42 per tube
	-300E		X	X		X	42 per tube
	-500E		X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACNW3190-500E to order product of 400mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

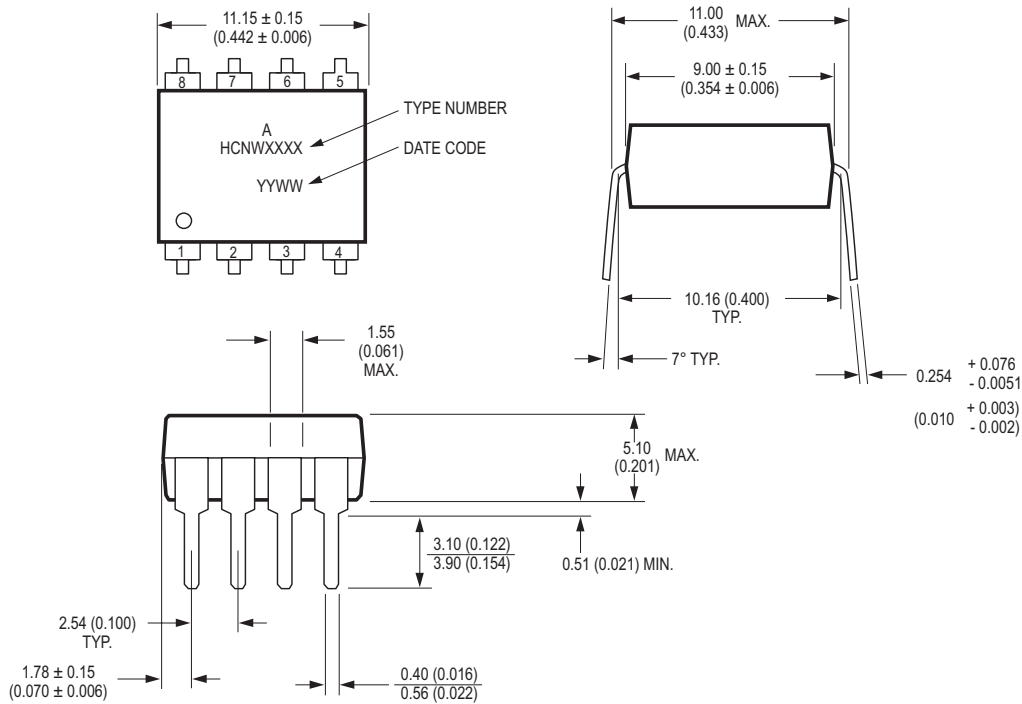
Example 2:

ACNW3190-000E to order product of 400mil DIP package in tube packaging and RoHS compliant.

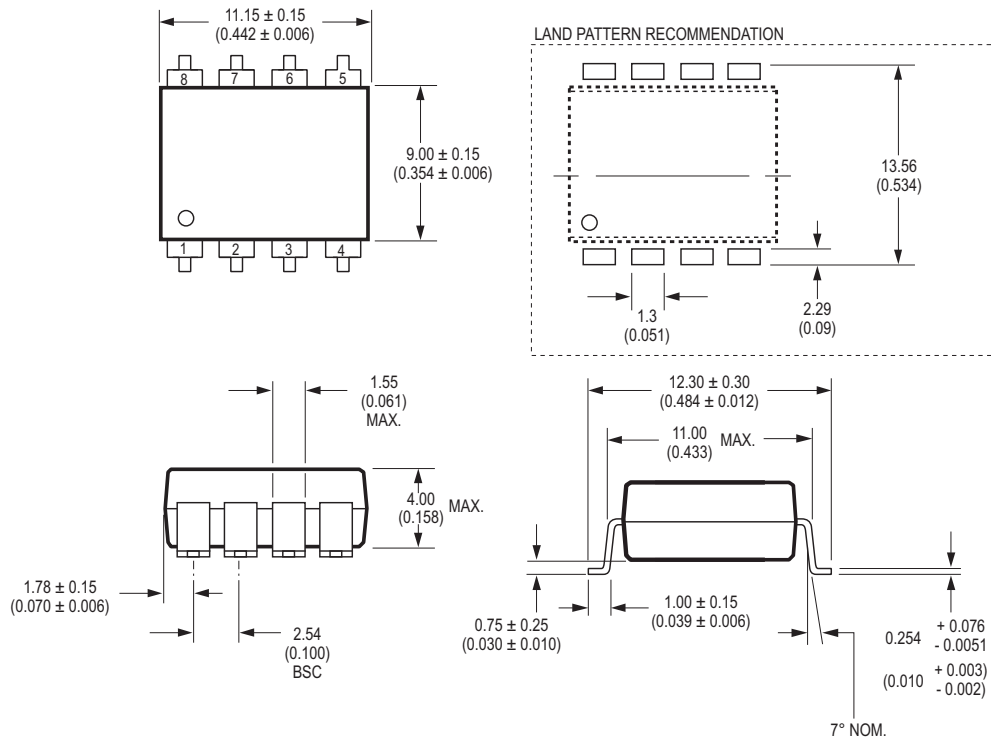
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

### ACNW3190 Outline Drawing (8-pin Wide Body Package)



### ACNW3190 Gull Wing Surface Mount Option 300 Outline Drawing

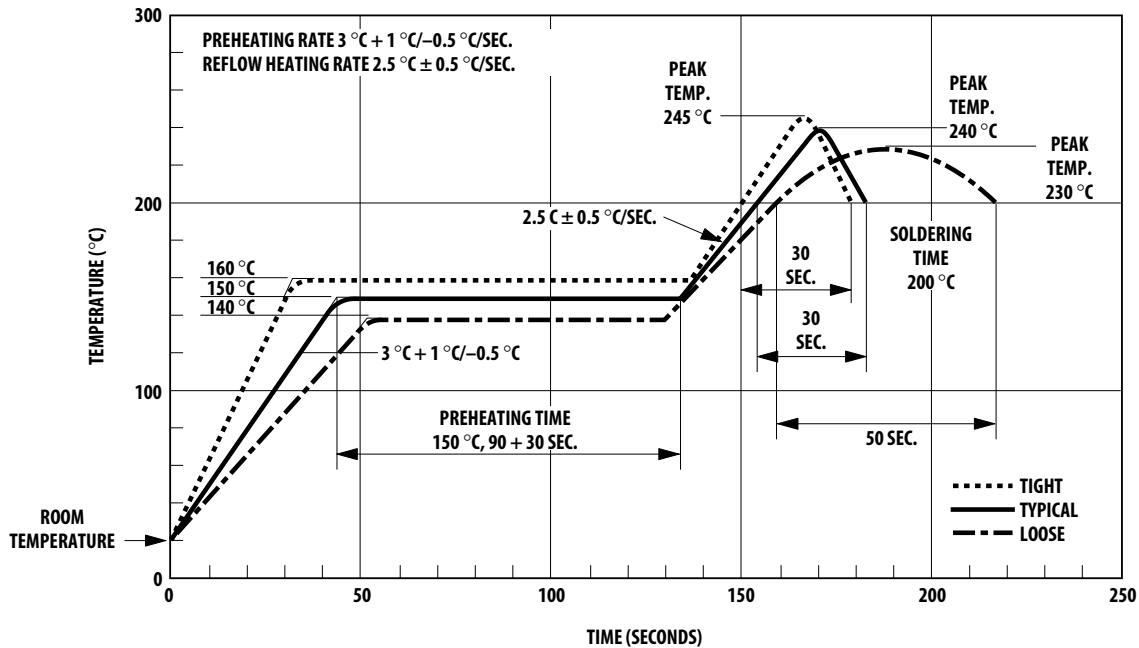


Dimensions in inches (millimeters)

Note:

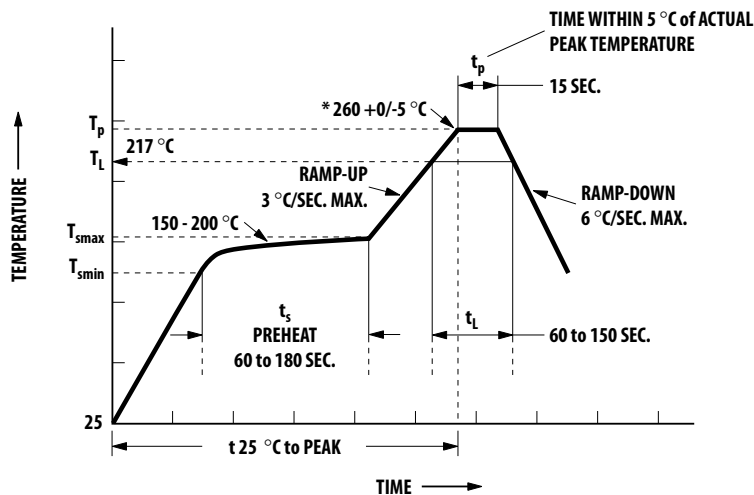
Floating Lead Protrusion is 0.25 mm (10 mils) max.

## Solder Reflow Temperature Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

## Recommended Pb-Free IR Profile



### NOTES:

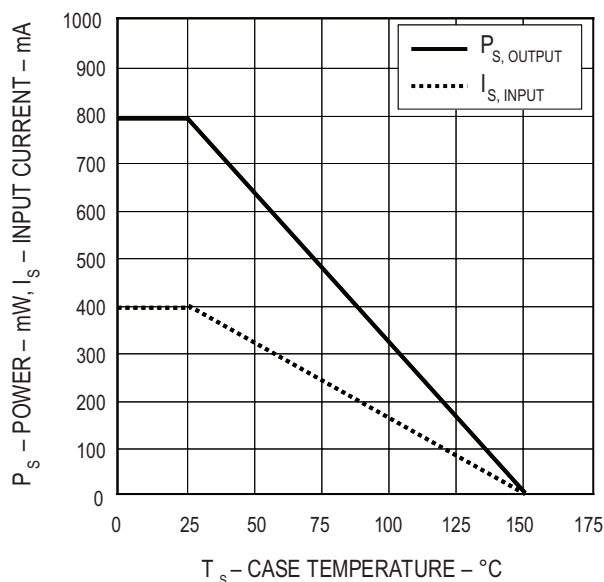
THE TIME FROM  $25^{\circ}\text{C}$  TO PEAK TEMPERATURE = 8 MINUTES MAX.

$T_{smax} = 200^{\circ}\text{C}$ ,  $T_{smin} = 150^{\circ}\text{C}$

NOTE: NON-HALIDE FLUX SHOULD BE USED.

\* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS  $245^{\circ}\text{C}$

## Dependence of Safety Limiting Values on Temperature



Note:

The Thermal Derating Graph above is in relation to Figure 30 and Figure 31 and S = 2cm.

## Regulatory Information

The ACNW3190 is approved by the following organizations:

### IEC/EN/DIN EN 60747-5-2

Approval under:

IEC 60747-5-2 :1997 + A1:2002

EN 60747-5-2:2001 + A1:2002

DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

### UL

Approval under UL 1577, component recognition program up to V<sub>ISO</sub> = 5000 V<sub>RMS</sub> expected prior to product release. File E55361.

### CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324 expected prior to product release.

**Table 1. IEC/EN/DIN EN 60747-5-2 Insulation Characteristics\***

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V <sub>rms</sub>		I – IV	
for rated mains voltage ≤ 300 V <sub>rms</sub>		I – IV	
for rated mains voltage ≤ 450 V <sub>rms</sub>		I – IV	
for rated mains voltage ≤ 600 V <sub>rms</sub>		I – IV	
for rated mains voltage ≤ 1000 V <sub>rms</sub>		I – III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V <sub>IORM</sub>	1414	V <sub>peak</sub>
Input to Output Test Voltage, Method b**			
V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 sec, Partial discharge < 5 pC	V <sub>PR</sub>	2652	V <sub>peak</sub>
Input to Output Test Voltage, Method a**			
V <sub>IORM</sub> × 1.5 = V <sub>PR</sub> , Type and Sample Test, t <sub>m</sub> = 60 sec, Partial discharge < 5 pC	V <sub>PR</sub>	2121	V <sub>peak</sub>
Highest Allowable Overvoltage (Transient Overvoltage t <sub>ini</sub> = 10 sec)	V <sub>IOTM</sub>	8000	V <sub>peak</sub>
Safety-limiting values			
– maximum values allowed in the event of a failure, also see Figure 2.			
Case Temperature	T <sub>S</sub>	150	°C
Input Current	I <sub>S, INPUT</sub>	400	mA
Output Power	P <sub>S, OUTPUT</sub>	800	mW
Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V	R <sub>S</sub>	≥ 10 <sup>9</sup>	Ω

\* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.

\*\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description of Method a and Method b partial discharge test profiles.

**Table 2. Insulation and Safety Related Specifications**

Parameter	Symbol	ACNW3190	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		1.0	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIla		Material Group (DIN VDE 0110, 1/89, Table 1)

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T <sub>S</sub>	-55	125	°C	
Operating Temperature	T <sub>A</sub>	-40	100	°C	
Output IC Junction Temperature	T <sub>J</sub>		150	°C	
Average Input Current	I <sub>F(AVG)</sub>		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300pps)	I <sub>F(TRAN)</sub>		1.0	A	
Reverse Input Voltage	V <sub>R</sub>		5	V	
“High” Peak Output Current	I <sub>OH(PEAK)</sub>		5.0	A	2
“Low” Peak Output Current	I <sub>OL(PEAK)</sub>		5.0	A	2
Total Output Supply Voltage	(V <sub>CC</sub> - V <sub>EE</sub> )	-0.5	35	V	
Input Current (Rise/Fall Time)	t <sub>r(IN)</sub> / t <sub>f(IN)</sub>		500	ns	
Output Voltage	V <sub>O(PEAK)</sub>	-0.5	V <sub>CC</sub>	V	
Output IC Power Dissipation	P <sub>O</sub>		800	mW	3
Total Power Dissipation	P <sub>T</sub>		850	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T <sub>A</sub>	- 40	100	°C	
Output Supply Voltage	(V <sub>CC</sub> - V <sub>EE</sub> )	15	30	V	
Input Current (ON)	I <sub>F(ON)</sub>	10	16	mA	
Input Voltage (OFF)	V <sub>F(OFF)</sub>	- 3.6	0.8	V	

**Table 5. Electrical Specifications (DC)**

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 30\text{ V}$ ,  $V_{EE} = \text{Ground}$ ; all Minimum/Maximum specifications are at Recommended Operating Conditions ( $T_A = -40$  to  $100^\circ\text{C}$ ,  $I_{F(ON)} = 10$  to  $16\text{ mA}$ ,  $V_{F(OFF)} = -3.6$  to  $0.8\text{ V}$ ,  $V_{CC} = 15$  to  $30\text{ V}$ ,  $V_{EE} = \text{Ground}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	$I_{OH}$	1.0	2.75		A	$V_O = V_{CC} - 4$	2, 3, 17	5
		4.0			A	$V_O = V_{CC} - 15$		2
Low Level Output Current	$I_{OL}$	1.0	3.5		A	$V_O = V_{EE} + 2.5$	5, 6, 18	5
		4.0			A	$V_O = V_{EE} + 15$		2
High Level Output Voltage	$V_{OH}$	$V_{CC}-4$	$V_{CC}-3$		V	$I_O = -100\text{ mA}$	1, 3, 19	6, 7
Low Level Output Voltage	$V_{OL}$		0.1	0.5	V	$I_O = 100\text{ mA}$	4, 6, 20	
High Level Supply Current	$I_{CCH}$		3.0	5.0	mA	Output open, $I_F = 7$ to $16\text{ mA}$	7, 8	
Low Level Supply Current	$I_{CCL}$		3.0	5.0	mA	Output open, $V_F = -3.0$ to $+0.8\text{ V}$		
Threshold Input Current Low to High	$I_{FLH}$		3.5	8.0	mA	$I_O = 0\text{ mA}$ , $V_O > 5\text{ V}$	9, 15, 21	
Threshold Input Voltage High to Low	$V_{FHL}$	0.8			V			
Input Forward Voltage	$V_F$	1.2	1.6	1.95	V	$I_F = 10\text{ mA}$	16	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$		-1.3		mV/ $^\circ\text{C}$			
Input Reverse Breakdown Voltage	$BV_R$	5			V	$I_R = 100\text{ }\mu\text{A}$		
Input Capacitance	$C_{IN}$		75		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		
UVLO Threshold	$V_{UVLO+}$	11.0	12.3	13.5	V	$V_O > 5\text{ V}$ , $I_F = 10\text{ mA}$	22, 28	
	$V_{UVLO-}$	9.5	10.7	12.0				
UVLO Hysteresis	$UVLO_{HYS}$		1.6					

**Table 6. Switching Specifications (AC)**

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 30\text{ V}$ ,  $V_{EE} = \text{Ground}$ ; all Minimum/Maximum specifications are at Recommended Operating Conditions ( $T_A = -40$  to  $100^\circ\text{C}$ ,  $I_{F(ON)} = 10$  to  $16\text{ mA}$ ,  $V_{F(OFF)} = -3.6$  to  $0.8\text{ V}$ ,  $V_{CC} = 15$  to  $30\text{ V}$ ,  $V_{EE} = \text{Ground}$ ).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	$t_{PLH}$	0.10	0.30	0.50	$\mu\text{s}$	$R_g = 10\text{ }\Omega$ , $C_g = 10\text{ nF}$ , $f = 10\text{ kHz}$ , Duty Cycle = 50%, $I_F = 10\text{ mA}$ , $V_{CC} = 30\text{ V}$	10, 11, 12, 14 13, 14, 23	
Propagation Delay Time to Low Output Level	$t_{PHL}$	0.10	0.30	0.50	$\mu\text{s}$			
Pulse Width Distortion	PWD			0.30	$\mu\text{s}$			15
Propagation Delay Difference Between Any Two Parts	PDD ( $t_{PHL} - t_{PLH}$ )		0.35		$\mu\text{s}$		35, 36	10
Rise Time	$t_r$		0.1		$\mu\text{s}$		23	
Fall Time	$t_f$		0.1		$\mu\text{s}$			
UVLO to Turn On Delay	$t_{UVLO,ON}$		0.8		$\mu\text{s}$	$V_O > 5\text{ V}$ , $I_F = 10\text{ mA}$	22	
UVLO to Turn Off Delay	$t_{UVLO,OFF}$		0.6		$\mu\text{s}$	$V_O < 5\text{ V}$ , $I_F = 10\text{ mA}$		
Output High Level Common Mode Transient Immunity	$ CM_H $	15	30		kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $I_F = 10$ to $16\text{ mA}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$	24	11, 12
Output Low Level Common Mode Transient Immunity	$ CM_L $	15	30		kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $V_F = 0\text{ V}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$		11, 13



**Table 7. Package Characteristics**

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	5000			$V_{RMS}$	$RH < 50\%$ , $t = 1 \text{ min.}$ , $T_A = 25^\circ\text{C}$		8, 9
Input-Output Resistance	$R_{I-O}$	$10^{12}$	$10^{13}$		$\Omega$	$V_{I-O} = 500 V_{DC}$ , $T_A = 25^\circ\text{C}$		9
		$10^{11}$				$V_{I-O} = 500 V_{DC}$ , $T_A = 100^\circ\text{C}$		
Input-Output Capacitance	$C_{I-O}$		0.5	0.6	pF	$f = 1 \text{ MHz}$		
LED-to-Ambient Thermal Resistance	$\theta_{LA}$				$^\circ\text{C/W}$		29, 30, 31	
LED-to-Detector Thermal Resistance	$\theta_{LD}$		See Thermal Model Section			See Thermal Model in Application Notes Section		
Detector-to-Ambient Thermal Resistance	$\theta_{DA}$							

\* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.3 \text{ mA}/^\circ\text{C}$ .
- Maximum pulse width =  $10 \mu\text{s}$ . This value is intended to allow for component tolerances for designs with  $I_O$  peak minimum =  $4.0 \text{ A}$ . See Applications section for additional details on limiting  $I_{OH}$  peak.
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $4.8 \text{ mA}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $5.4 \text{ mA}/^\circ\text{C}$ .
- Maximum pulse width =  $50 \mu\text{s}$ .
- In this test  $V_{OH}$  is measured with a dc load current. When driving capacitive loads  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero amps.
- Maximum pulse width =  $1 \text{ ms}$ .
- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000 \text{ Vrms}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ ).
- Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two ACNW3190 parts under the same test condition.
- Pins 1 and 4 need to be connected to LED common.
- Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (i.e.,  $V_O > 15.0 \text{ V}$ ).
- Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (i.e.,  $V_O < 1.0 \text{ V}$ ).
- This load condition approximates the gate load of a  $1200 \text{ V}/100\text{A}$  IGBT.
- Pulse Width Distortion (PWD) is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.

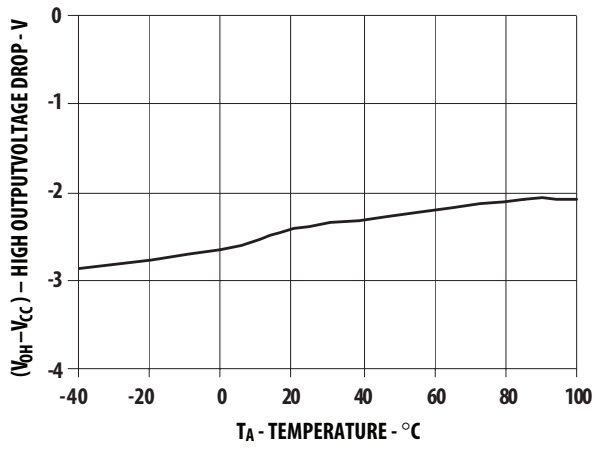


Figure 1.  $V_{OH}$  vs. Temperature

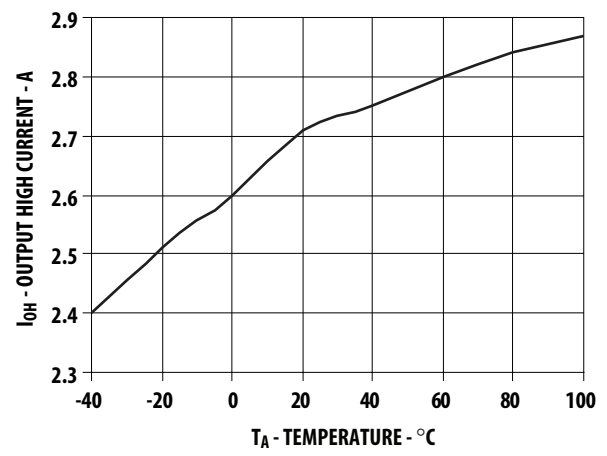


Figure 2.  $I_{OH}$  vs. Temperature

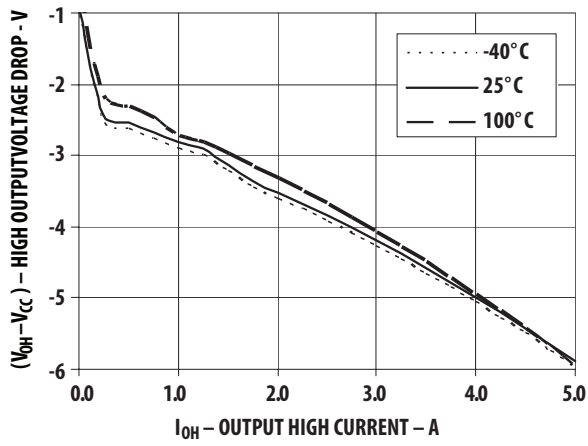


Figure 3.  $V_{OH}$  vs.  $I_{OH}$

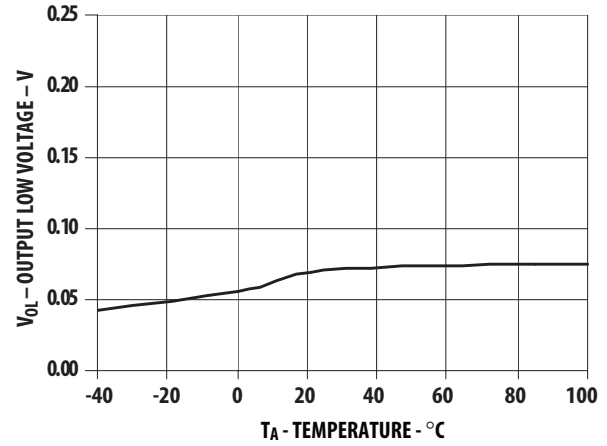


Figure 4.  $V_{OL}$  vs. Temperature

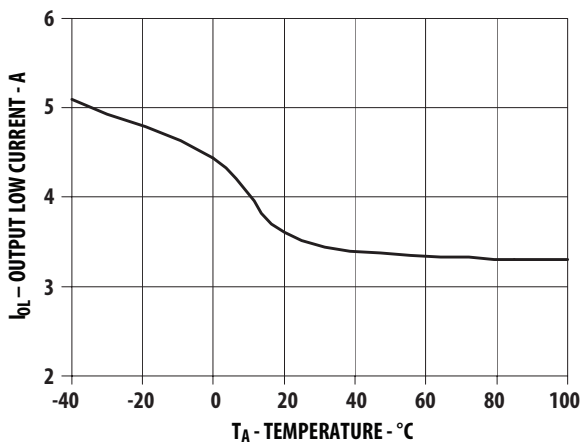


Figure 5.  $I_{OL}$  vs. Temperature

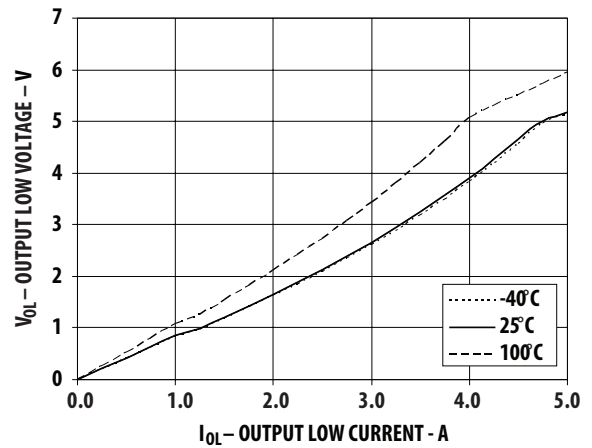


Figure 6.  $V_{OL}$  vs.  $I_{OL}$

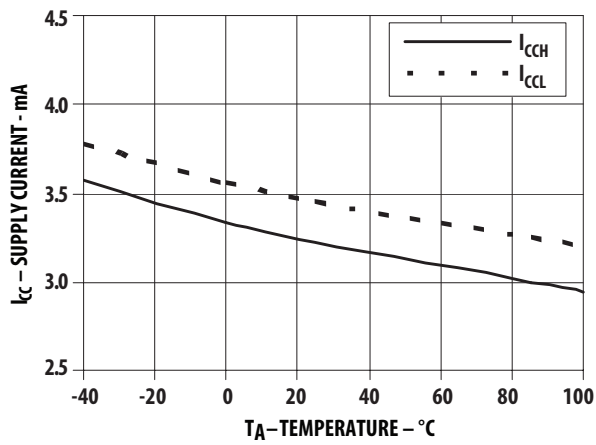


Figure 7.  $I_{CC}$  vs. Temperature

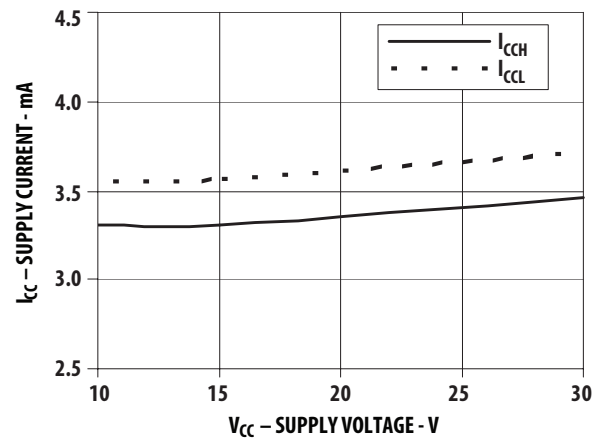


Figure 8.  $I_{CC}$  vs.  $V_{CC}$

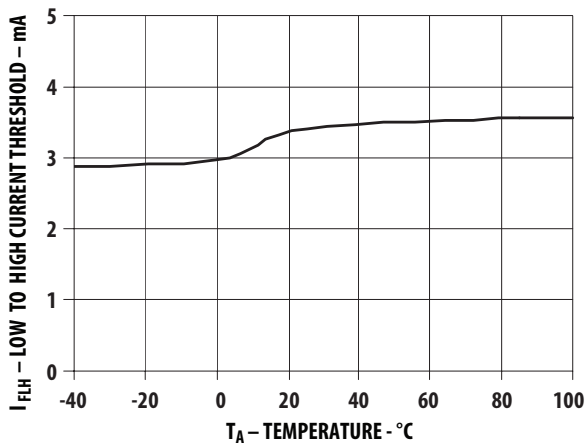


Figure 9.  $I_{FLH}$  vs. Temperature

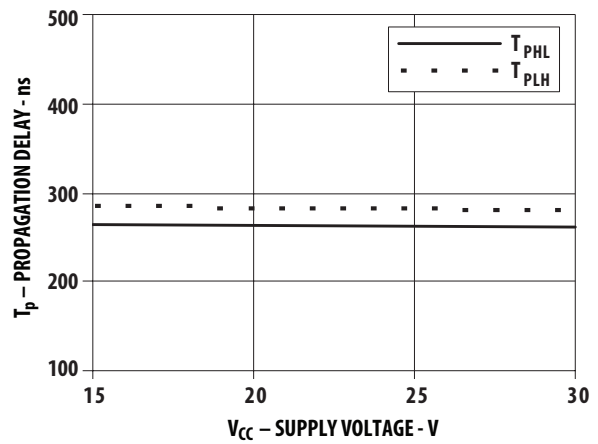


Figure 10. Propagation delay vs.  $V_{CC}$

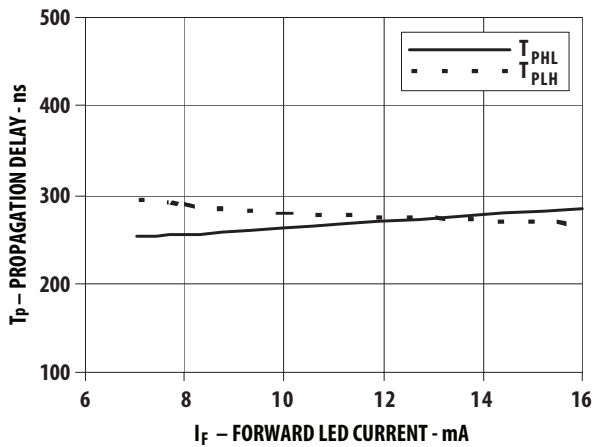


Figure 11. Propagation delay vs.  $I_F$

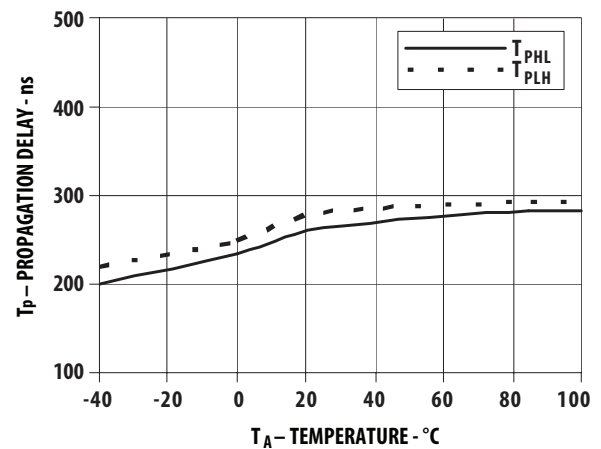


Figure 12. Propagation delay vs. Temperature

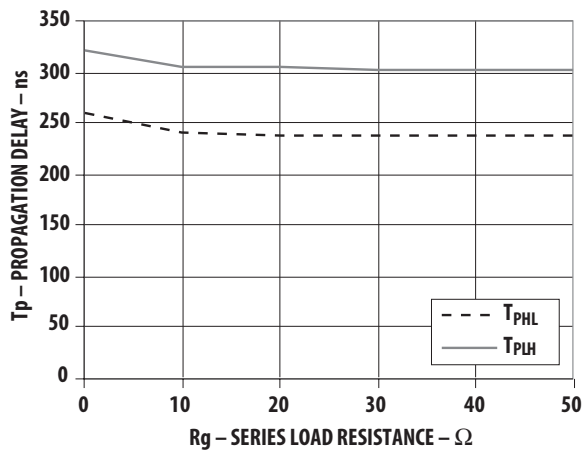


Figure 13. Propagation Delay vs.  $R_g$

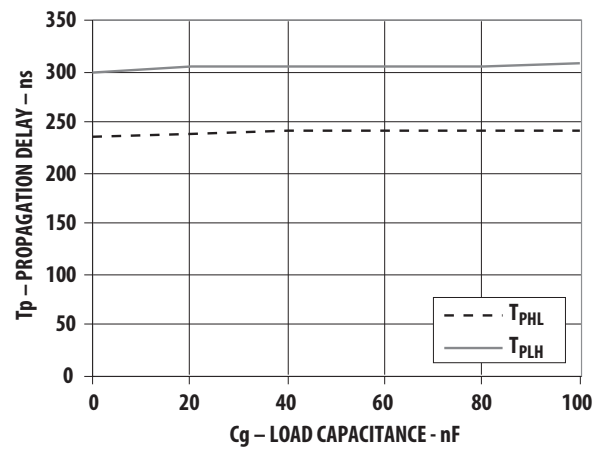


Figure 14. Propagation Delay vs.  $C_g$

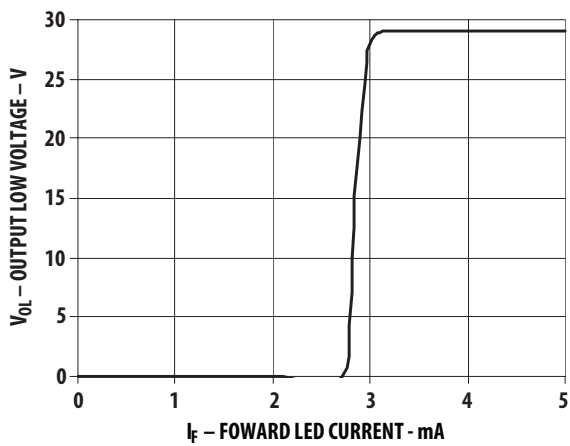


Figure 15. Transfer Characteristics

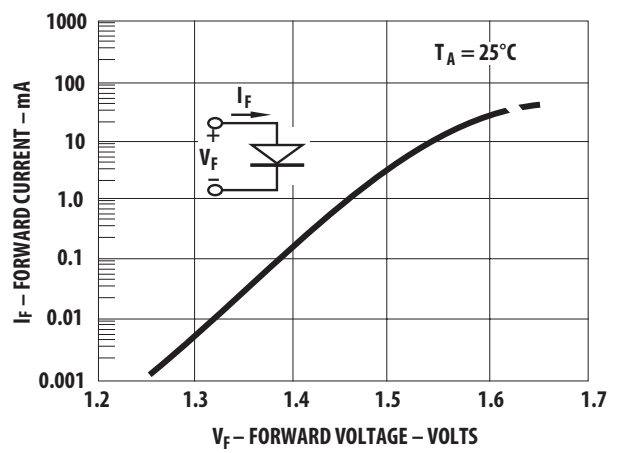


Figure 16. Input Current vs. Forward Voltage

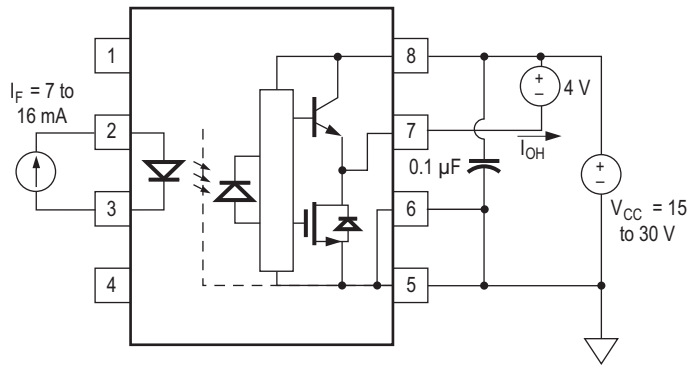


Figure 17.  $I_{OH}$  Test Circuit

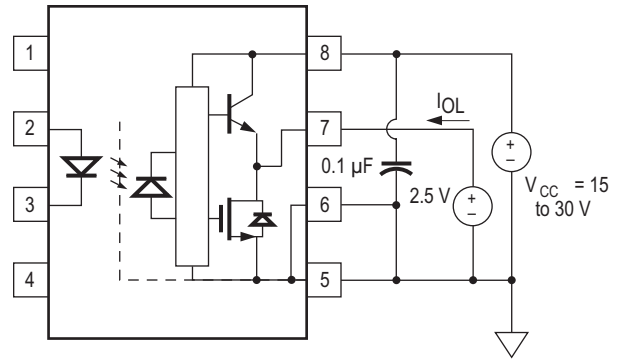


Figure 18.  $I_{OL}$  Test Circuit

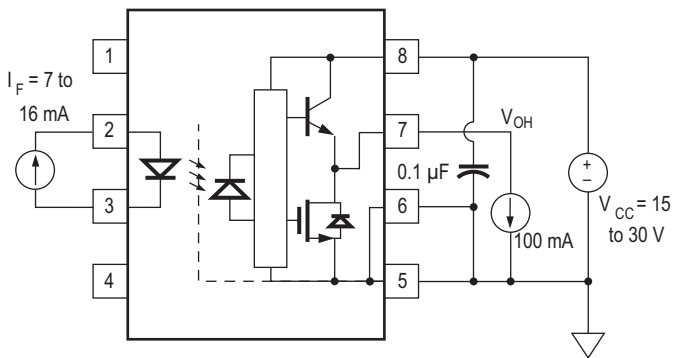


Figure 19.  $V_{OH}$  Test Circuit

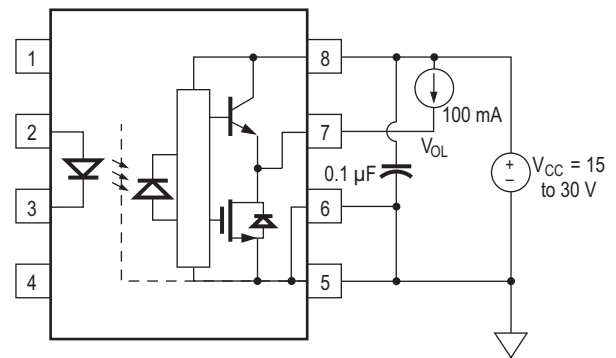


Figure 20.  $V_{OL}$  Test Circuit

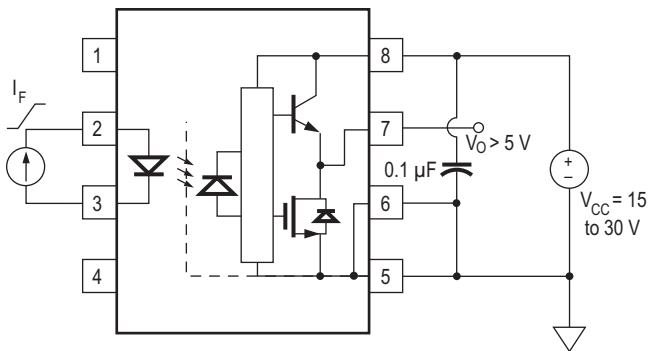


Figure 21.  $I_{FLH}$  Test Circuit

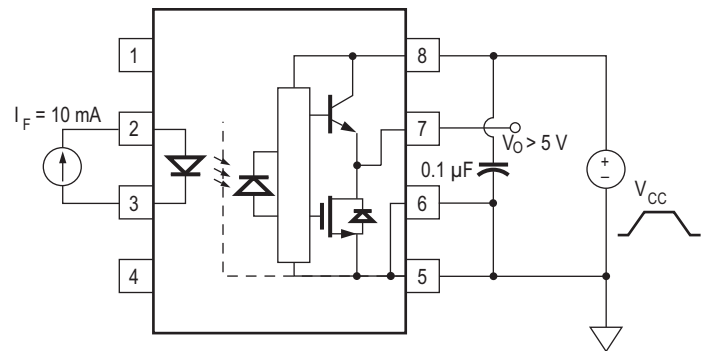


Figure 22. UVLO Test Circuit

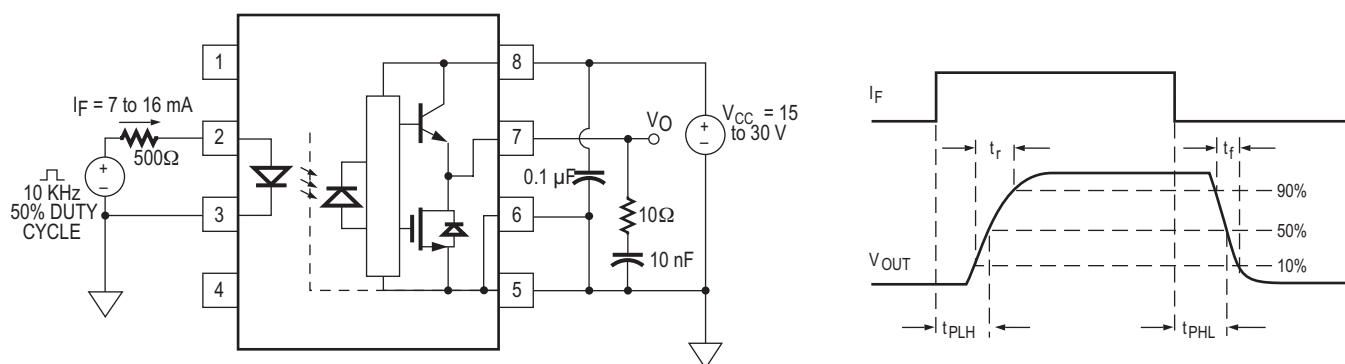


Figure 23.  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$  Test Circuit and Waveforms

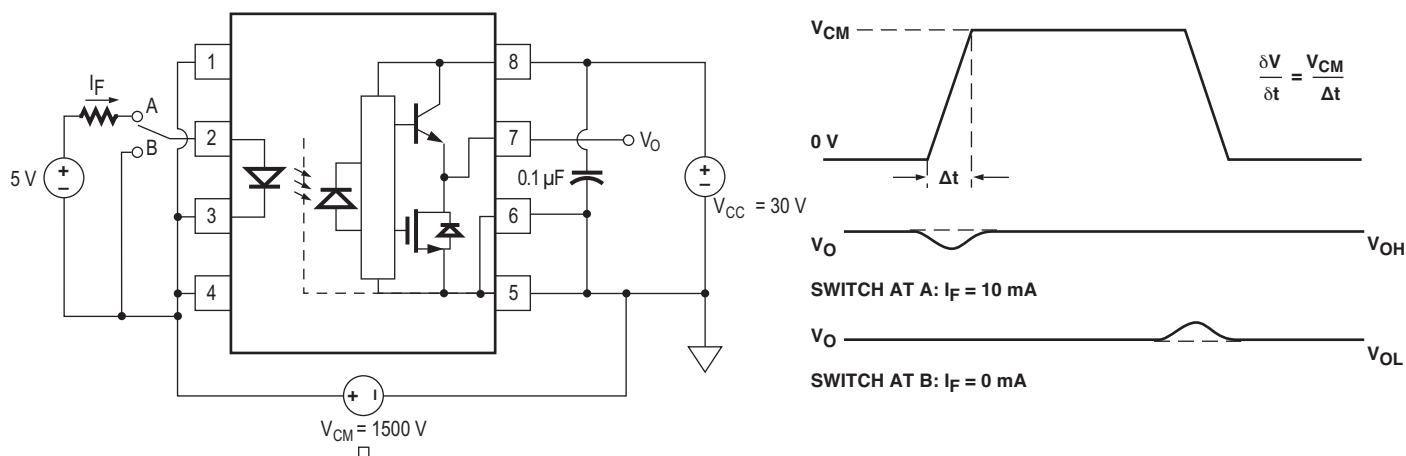


Figure 24. CMR Test Circuit and Waveforms

## Application Notes

Figure 25 and 26 show two recommended application circuits. Figure 25 shows a single power supply gate driver using the driver's maximum  $V_{OL}$  value of 0.5V. Figure 26 shows a dual power supply gate driver circuit which is applicable for higher power IGBT driving due to the existence of higher miller capacitance in these IGBTs.

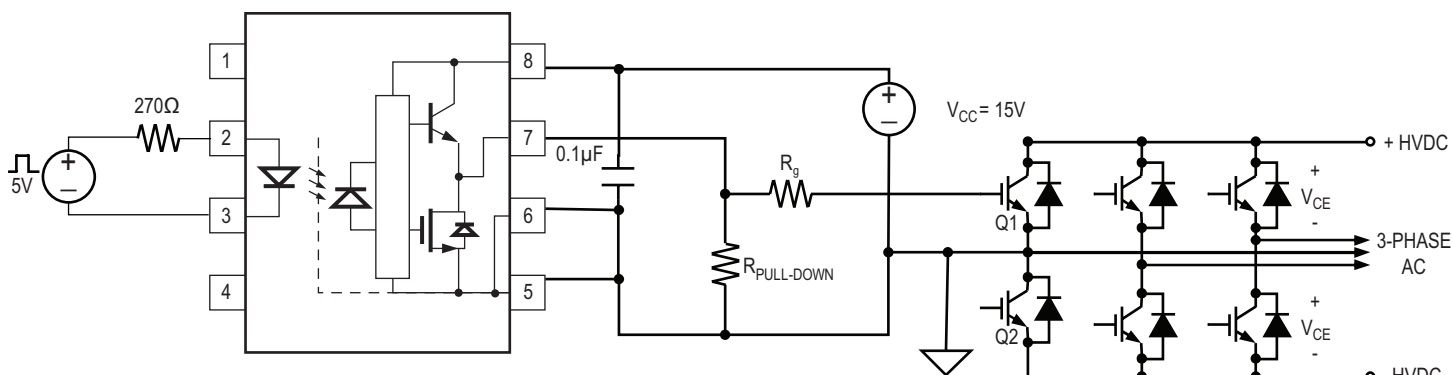


Figure 25. Recommended LED drive and application circuit

For high side bootstrap driving, note that the bypass capacitor of 0.1μF in parallel with 10μF or above to be connected across VCC and VEE is important to deliver high peak output current.

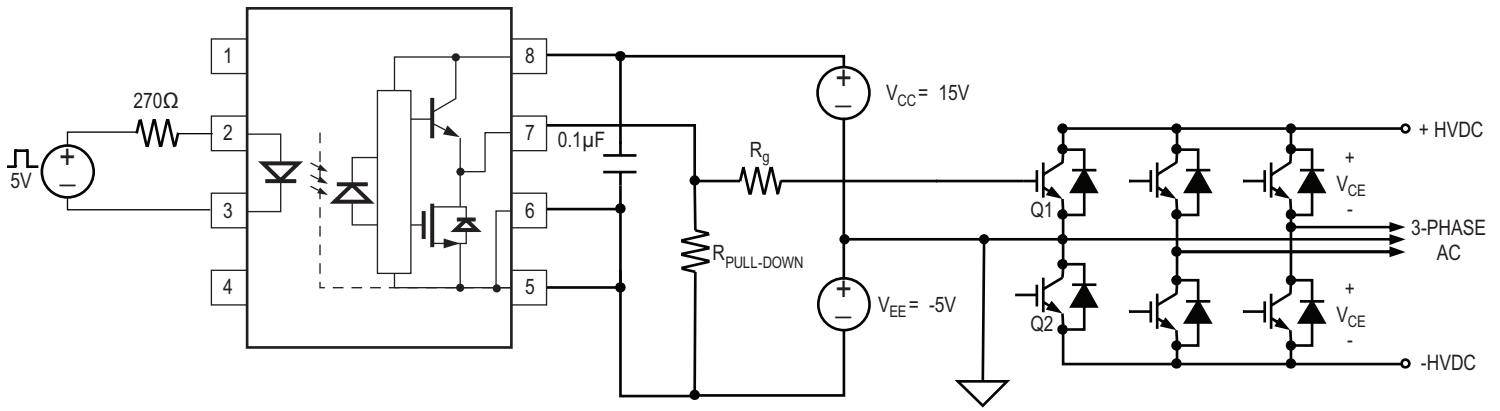


Figure 26. ACNW3190 typical application circuit with negative IGBT gate drive

### Selecting the Gate Resistor (Rg) to minimize IGBT Switching Losses.

#### Step 1: Calculate Rg Minimum from the IOL Peak Specification

The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the ACNW3190. The operating temperature is 100°C.

$$R_g \geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}}$$

$$= \frac{(15V + 5V - 3.5V)}{4A}$$

$$\approx 4.3\Omega$$

The VOL value of 3.5V in the previous equation is a conservative value of VOL at the peak current of 4.0A (see Figure 6). At lower Rg values the voltage supplied by the ACNW3190 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used, VEE in the previous equation is equal to zero volts.

#### Step 2: Check the ACNW3190 Power Dissipation and Increase Rg if Necessary.

The ACNW3190 total power dissipation (PT) is equal to the sum of the emitter power (PE) and the output power (PO):

$$P_T = P_E + P_O$$

$$P_E = I_F * V_F * \text{Duty Cycle}$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$$

$$= I_{CC} * (V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G) * f$$

For the circuit in Figure 26 with IF (worst case) = 16 mA, Rg = 4.3Ω, Max Duty Cycle = 80%, Qg = 1000 nC, f = 15 kHz and TA max = 85°C:

$$P_E = 16 \text{ mA} * 1.95V * 0.8 = 25 \text{ mW}$$

$$P_O = 3.25 \text{ mA} * 20 \text{ V} + 13\mu\text{J} * 15 \text{ kHz}$$

$$= 65 \text{ mW} + 195 \text{ mW}$$

$$= 260 \text{ mW}$$

$$< 728 \text{ mW} (P_{O(MAX)} @ 85^\circ\text{C} = 800 \text{ mW} - 15^\circ\text{C} * 4.8 \text{ mW}/^\circ\text{C})$$

The value of 3.25 mA for ICC in the previous equation was obtained by derating the ICC max of 5 mA to ICC max at 100C (see Figure 7).

The above computation shows that the power dissipation is within the specified limits. However, designers should verify that the thermal limits have not been violated by using the thermal model provided in this datasheet. This thermal model obtained based on JEDEC specification.

PE Parameter	Description
IF	LED Current
VF	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

PO Parameter	Description
ICC	Supply Current
VCC	Positive Supply Voltage
VEE	Negative Supply Voltage
Esw(Rg,Qg)	Energy Dissipated in the HCPL-3120 for each IGBT Switching Cycle (See Figure 27)

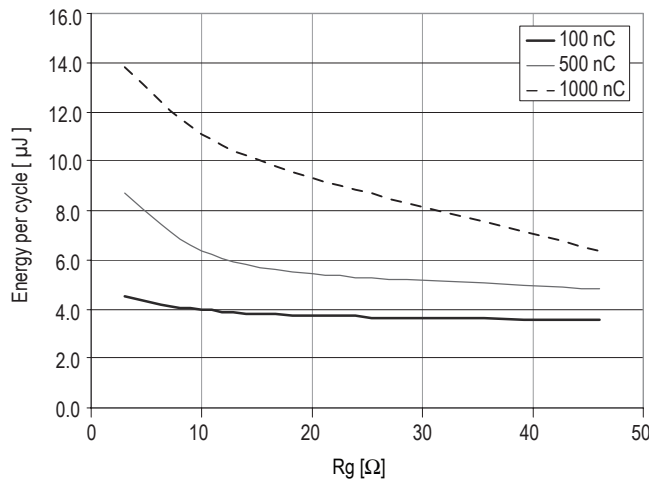


Figure 27. Energy dissipated in the ACNW3190 for each IGBT switching cycle

### Under Voltage Lockout Feature

The ACNW3190 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the ACNW3190 supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the ACNW3190 output is in the high state and the supply voltage drops below the ACNW3190  $V_{UVLO-}$  threshold ( $9.5 < V_{UVLO-} < 12.0$ ) the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of  $0.6 \mu s$ . When the ACNW3190 output is in the low state and the supply voltage rises above the ACNW3190  $V_{UVLO+}$  threshold ( $11.0 < V_{UVLO+} < 13.5$ ) the optocoupler output will go into the high state (assumes LED is "ON") with a typical delay, UVLO Turn On Delay of  $0.8 \mu s$ .

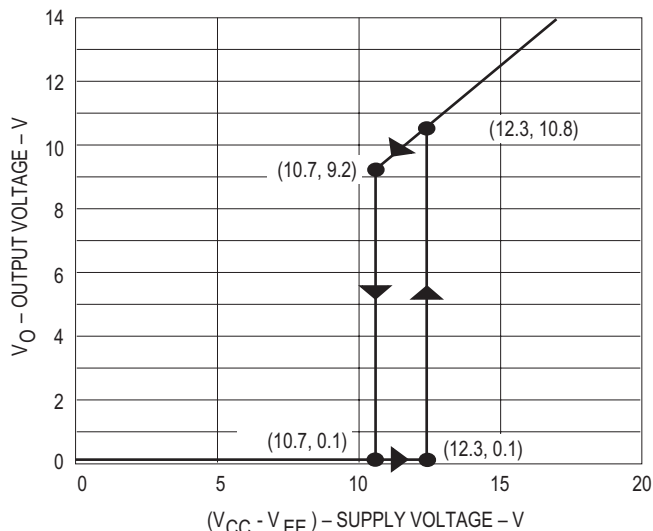


Figure 28. Under Voltage Lock Out

## Thermal Model

### Introduction

For application which requires an output gate current more than 2A, adequate PCB pad heat-sink must be provided to dissipate the power loss in the package. Failure to provide proper heat dissipation will potentially damage the gate drive after pro-long usage. This thermal model allows designer to compute the temperature of the LED and detector.

### Definitions

$\theta 1$ : Thermal impedance from LED junction to ambient

$\theta 2$ : Thermal impedance from LED to detector (output IC)

$\theta 3$ : Thermal impedance from detector (output IC) junction to ambient

Ambient Temperature: Measured approximately 1.25 cm above the optocoupler, with no forced air.

### Description

This thermal model assumes that an 8-pin single-channel plastic package optocoupler is soldered into a  $7.62 \text{ cm} \times 7.62 \text{ cm}$  printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$\Delta T_{EA} = A11 * P_E + A12 * P_D$$

$$\Delta T_{DA} = A21 * P_E + A22 * P_D$$

where,

$\Delta T_{EA}$  = Temperature difference between ambient and LED

$\Delta T_{DA}$  = Temperature difference between ambient and detector

$P_E$  = Power dissipation from LED

$P_D$  = Power dissipation from detector

$A11, A12, A21, A22$  thermal coefficients (units in  $^{\circ}\text{C}/\text{W}$ ) are functions of the thermal impedances  $\theta 1, \theta 2, \theta 3$  (See Note 2).

Table 1. Thermal Model-B Coefficient Data (units in  $^{\circ}\text{C}/\text{W}$ )

S (cm)	A11	A12, A21	A22
1	218.9	39.31	55.3
2	200.6	29.8	45
4	198	23.59	41.7

Jedec Specifications	A11	A12, A21	A22
low K board	254	50.3	66.8
High K board	151.2	16.72	39.06



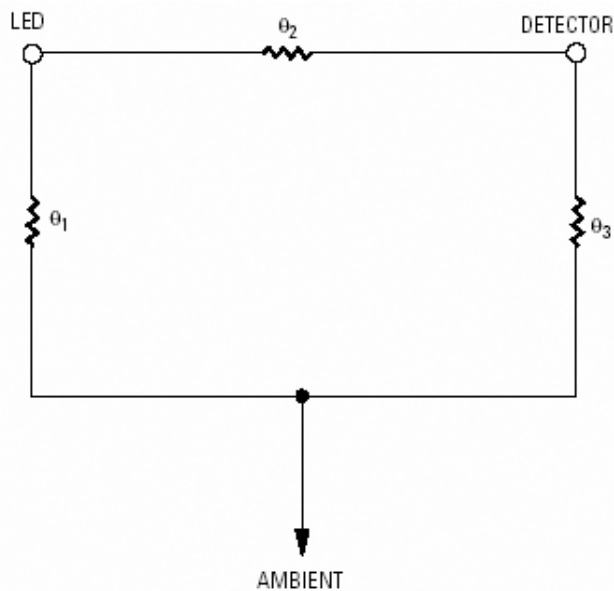


Figure 29. Thermal Model-B Diagram

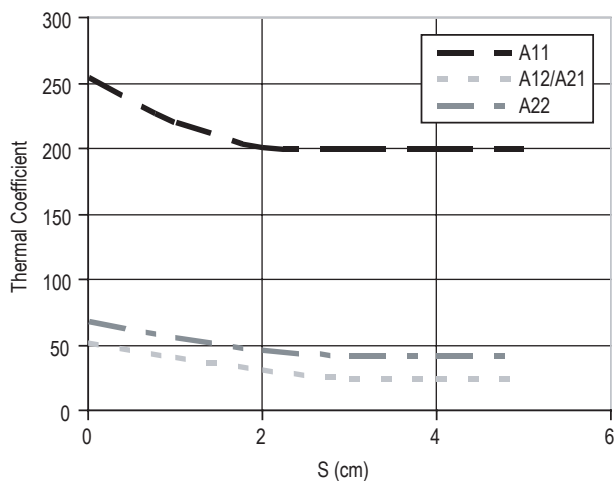


Figure 31. Thermal Coefficient Plot against S

Notes:

1. Maximum junction temperature for above parts: 150 °C.
2.  $A11 = \theta_1 \parallel (\theta_2 + \theta_3)$ ;  $A12 = A21 = (\theta_1 \theta_2) / (\theta_1 + \theta_2 + \theta_3)$ ;  $A22 = \theta_3 \parallel (\theta_2 + \theta_3)$ .

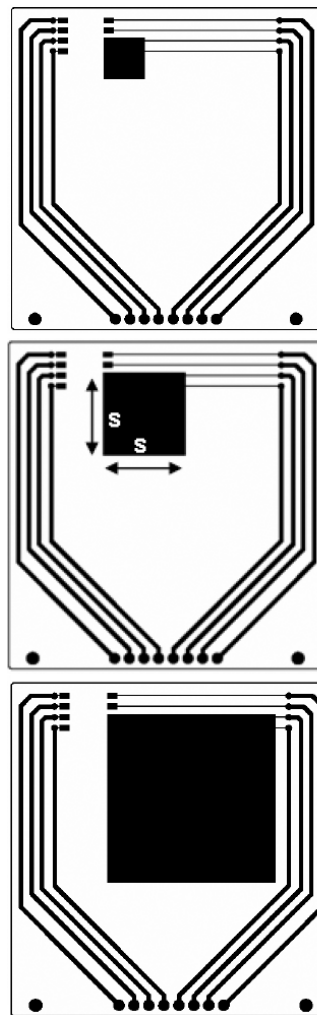


Figure 30. Evaluation thermal board design

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