MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EE463 - Static Power Conversion-I

Hardware Project Report

AC to DC Motor Drive

28/01/2018

Raşit GÖKMEN - 2333086

CONTENTS

1. INTRODUCTION

The three basic switching power supply topologies in common use are the buck,boost, and buck-boost. These topologies are nonisolated, that is, the input and output voltages share a common ground. There are, however, isolated derivations of these nonisolated topologies. In this project, buck topology is used to step down the input voltage. To convert AC input voltage to input voltage of buck converter full bridge rectifier is used. A power mosfet is used as an switch and also a gate driver is used to drive this power mosfet and isolation. This report includes also computer simulations, component selections and power loss calculations.

2. TOPOLOGY SELECTION

AC/DC motor drive can be impelemented with various topologies. The AC input must be rectified. Diodes and thyristors are main component used in rectifier circuit. The gate control of thyristor is quite complicated and it can not controlled fixed value. They are also more expensive than diodes. So, rectification is implemented using diodes. As for number of phase of input voltage, single phase is consideration more convinient. Because, when three phase input voltage used, the voltage at the rectifier circuit is about 540V, so all components in the converter must be withstand this voltage. For this voltage level, it is hard to find commercial capacitor and mosfet etc. It is also expensive. Since the rated voltage of motor is 200V, approximately %70-80 duty cycle is enough with single phase input voltage. The inductor and capacitor at the output of buck converter act as a filter so output becomes more smoother. Also, filter capacitors are used at the rectifier output. The block diagram of selected topology is given below.

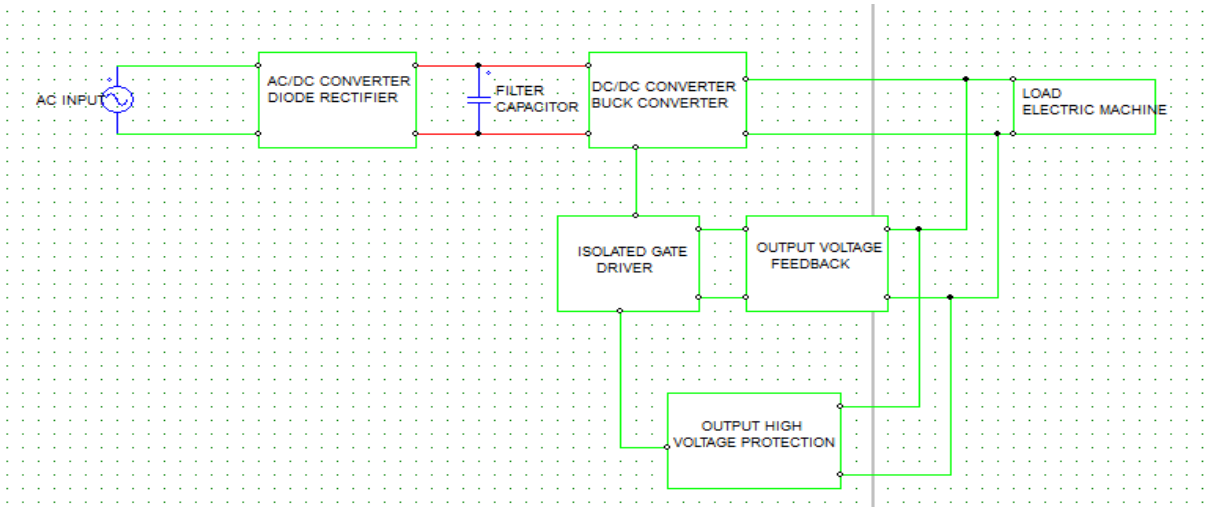


Figure 1 Block Diagram of selected topology

3. PROJECT SPECIFICATIONS

The project specifications are given in table 1 below.

Table 1 : Project Specifications

Input Voltage	230Vrms
Line frequency	50 Hz
Output Voltage	120 - 200 V
Output Current	6A
Duty Cycle	0.625
Switching Frequency	20 kHZ
Inductor current ripple	50%

4. BRIDGE RECTIFIER

The input voltage of buck converter is produced from phase voltage using bridge rectifier. The body diodes of TO-247 mosfet's are used as a diode. Output capacitance is calculated using simulation. 20 picies of 47uF capactior is used. The input voltage of buck converter is changing between 322V. Simulation result is shown in Figure 3.

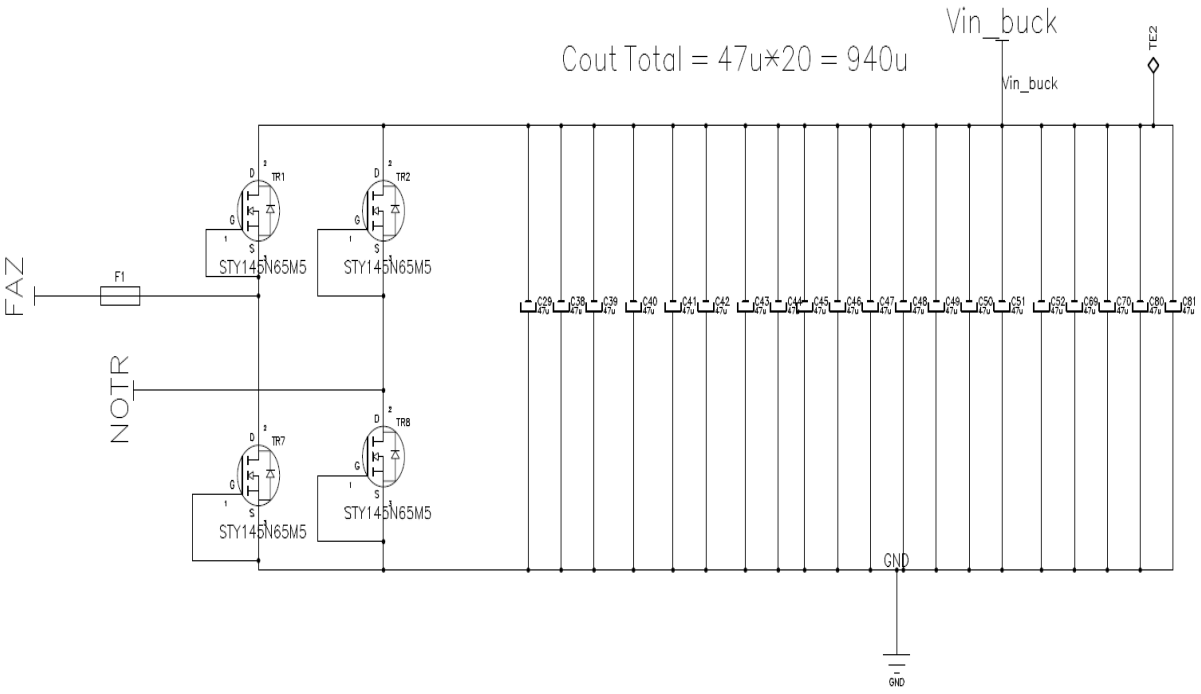


Figure 4.1 : Single Phase Bridge Rectifier

5. BUCK CONVERTER

A buck converter is implemented after the bridge rectifier output. The buck converter has the filter inductor on the output side, which provides a smooth continuous output current waveform to the load. Basic diagram of buck converter is given below.

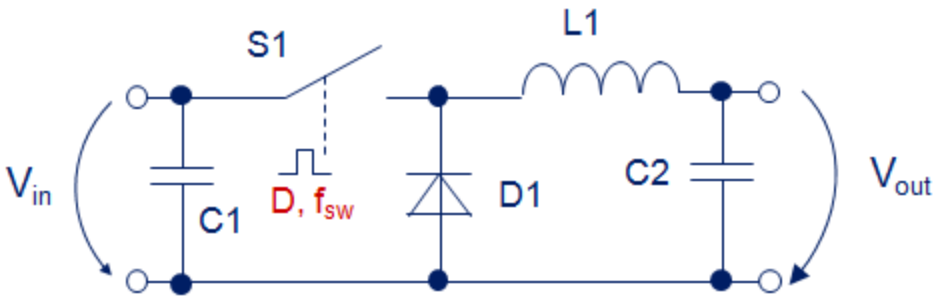
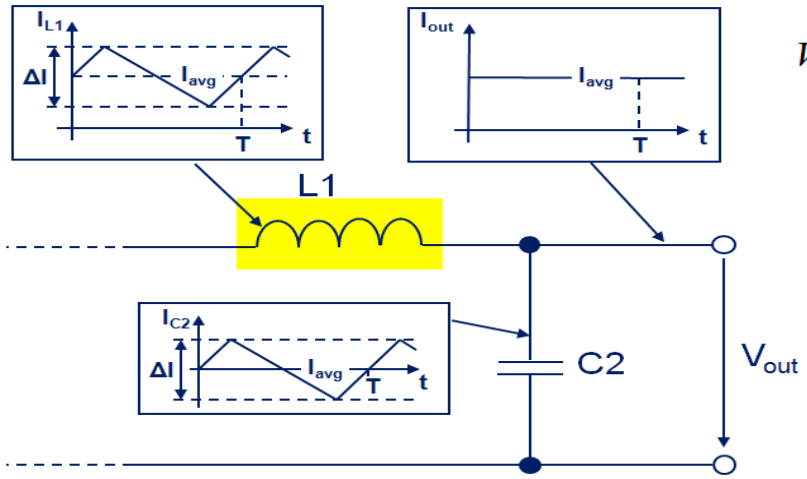


Figure 5.1 (Buck Converter – Basic Diagram)

5.1 Component Selection :

The filter inductor value and its peak current are determined based on the specified maximum inductor current ripple.



$$V_{L1} = L_1 \cdot \frac{di_{L1}}{dt}$$

$$= L_1 \cdot \frac{\Delta I_{L1}}{(1-D)\cdot T} = V_{out}$$

$$L_1 = \frac{V_{out} \cdot (1-D)}{f_{sw} \cdot \Delta I_{L1}}$$

Figure 5.2 Buck converter inductance calculation

From our specification table 1 . The inductor value is calculated :

$$L = \frac{Vout}{fsw} \cdot \frac{(1-D)}{\Delta IL} = \frac{200}{20*10\text{^}3} \cdot \frac{(1-200/320)}{6*\%50} = 1.25 \text{ mH} \qquad \text{(Equation 5.1)}$$

As shown below 25 pieces of 47uH inductor is used. The total inductance is 1.175 mH. The maximum rms current and saturation current of this inductor is 8.5A. For 6A output current, the maximum value of inductor current is 7.64 A which is in safety range. The curent waveform of inductor for worst case i.e for maximum input voltage and maximum output current is given below.

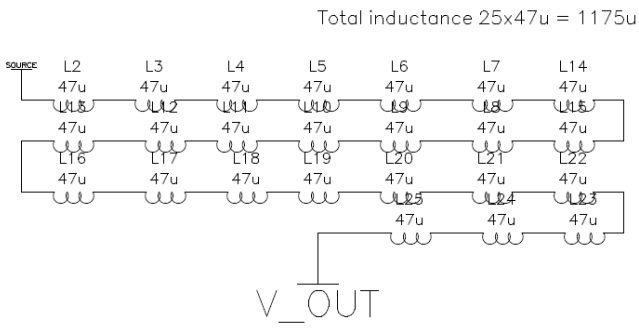


Figure 5.3 A series connection of inductors to obtain inductance value

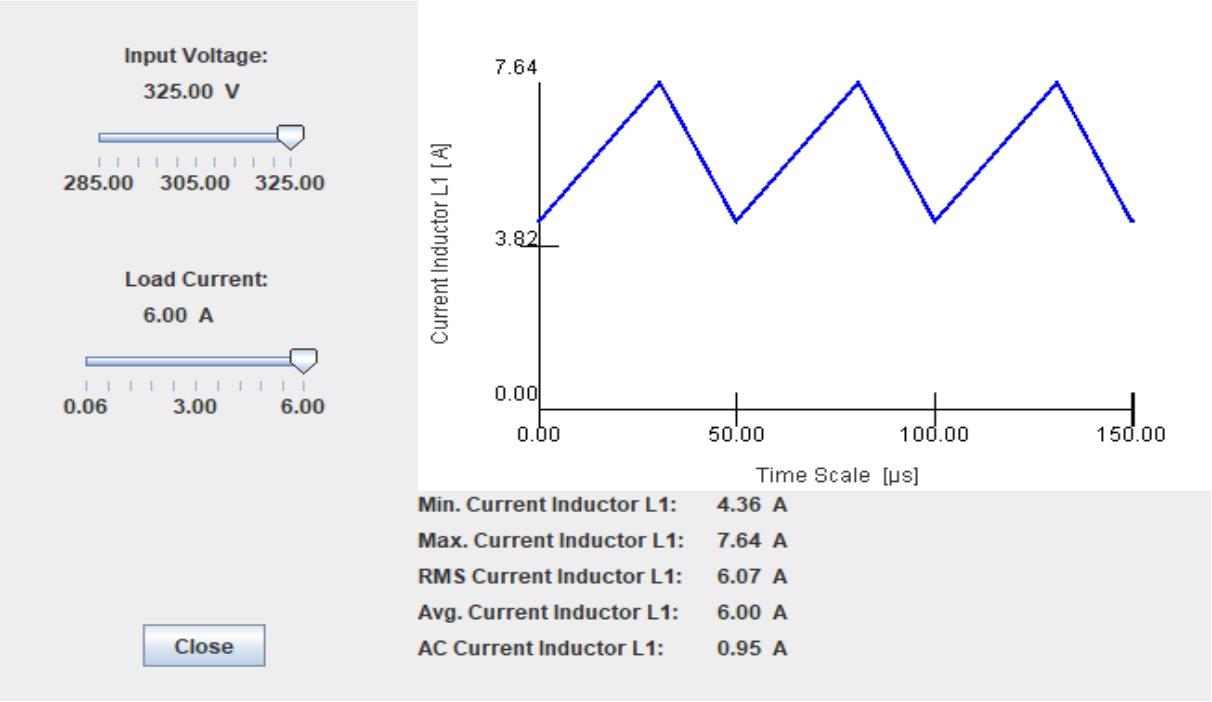


Figure 5.4 Inductor current waveform for selected inductance

For continuous inductor current mode operation, to determine the amount ofcapacitance needed asa function of inductor current ripple, ΔIL, switchingfrequency, fs, and desired output voltageripple, ΔVo, the following equation is used assuming all the output voltage ripple is due to the capacitor'scapacitance.

$$C \geq \frac{\Delta I_L}{8 \times f_S \times \Delta V_O}$$

(Equation 5.2)

where $\Delta IL = 7.64 - 4.36 = 3.28\ A$

fs = 20 kHz

ΔVo = %10 (assumed)

So C is must be greater than 205 uF. The output capacitance is choosed 20*47uF = 940uF. 20 pieces of capacitor used, because the maximum rms current rating of selected capacitor is 0.4 A . To not exceed this current rating, the output current is shared to 20 pieces of capacitor. The rms current of each capacitor ;

Iout(rms) / 20 = 6.07/20 = 0.3 A which is in safety region.

The switch is implemented by using power mosfet. This mosfet must withstand with the voltage which is observed 325 V in simulation but it may be greater in experimental enviroment due to transient overshoot. It must also be capable to carry minimum 7.64 A current. A power mosfet with x product number which is 650V, 138A TO247 package is selected. The datasheet of this mosfet given in appendix section at the end of this report.
The selection process of free wheeling diode is same with the selection process of switch. It will be also used with heatsink.

5.2 Power Losses Calculation :

5.2.1 Switch(main mosfet) Losses :

The different losses which can be seen in the FET of a power supply are conducted losses, switching losses, Coss losses, and body diode losses. Reverse recovery losses are neglected, but can become significant at high switching frequencies.

$P_{cond} = I_{FET(rms)}^{2} * R_{ds(on)} = 6.07 * 0.012\ \Omega = 0.44$ W

$P_{sw} = V_{DS} * \frac{fsw}{2} * (t_{rise} * I_{FET,min} + t_{fall} * I_{FET,max})$

$P_{sw} = 300V * \frac{20*10\text{^}3}{2} *(11ns* 0 + 82ns* 6) = 1.476$ W

$P_{Coss} = Coss * V_{DS} * \frac{fsw}{2} = 413pF* 300V * 10kHz = 1.24$ mW

$Ptotal = 0.44 + 1.476 + 1.24*10^{-3} = 1.916$ W

5.2.2 Diode Power Loss :

$P_{Diode} = Io * V_F *(1-D)= 6.07*0.7*(1-0.625) = 1.6$ W

5.3 Output Voltage Feedback Control Loop :

Since the switching frequency of switching regulators is at range ten to hundered kHz , there are overshoot at the output voltage and current. To reduce this overshoots i.e to set the output voltage or current at fixed value, voltage control or current control techniques are used. In this project, our specification is speed control of dc motor. Since the speed of dc motor is proportional with its armature voltage (buck output voltage) a voltage control loop is designed.

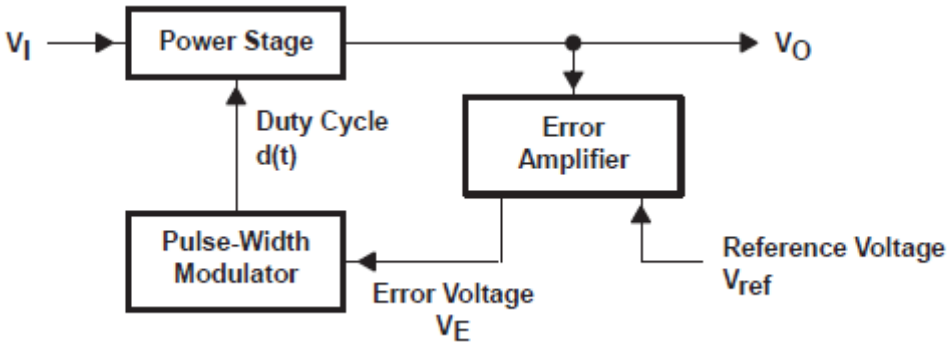


Figure 5.5 Control Loop Components

Control Stage :

As shown below, output voltage is sampled with a resistor divider and compared with the reference voltage of error amplifier positive input. Then, the output of error amplifier is compared with a sawtooth waveform with period frequency of switching frequency. The comparator is then produce a pwm signal. This pwm signal is the input of isolated gate driver.

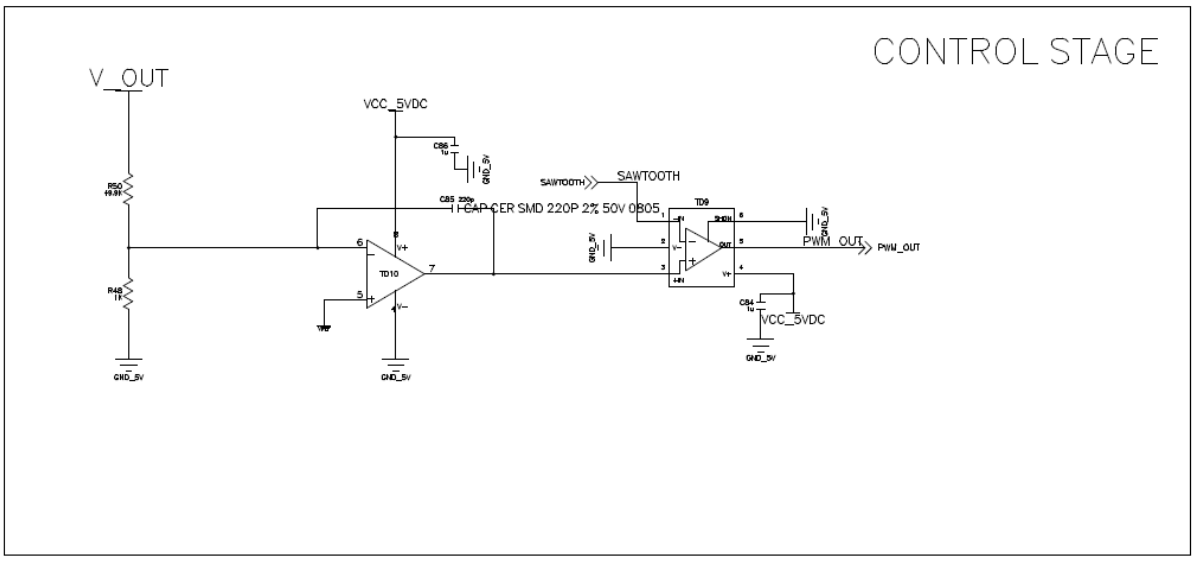


Figure 5.6 Control stage schematic

As shown below, whenever error amplifier output is greater than sawtooth wavefrom, the gate signal goes high. Similarly, whenever error amplifier output is greater than sawtooth wavefrom, the gate signal goes low. The error amplifier output changes it's states when input voltage greater or less than reference voltage (scaled set voltage). In summarize, this circuits is changes the duty cycle of gate signal of switch to keep output voltage constant. TLV3501 comparator with 4.5 ns propogation delay is used.

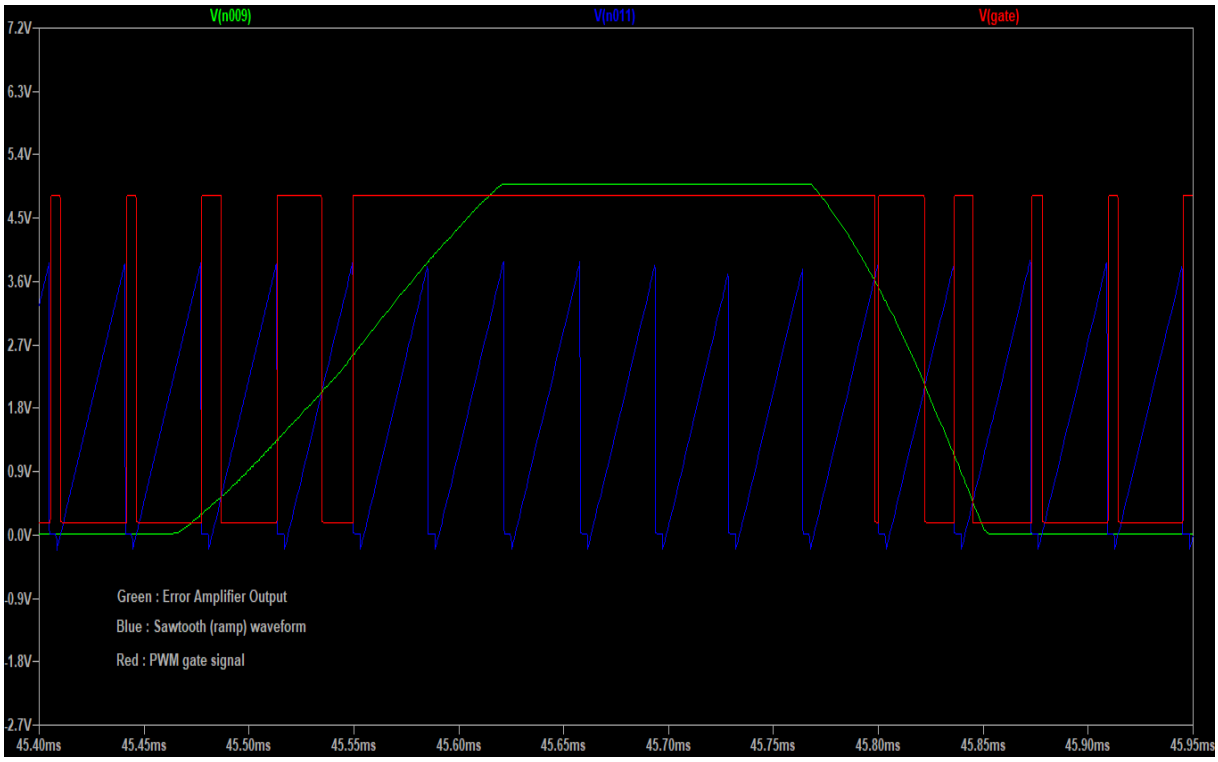


Figure 5.7 Control stage waveforms

Sawtooth wavefrom generation :

A sawtooth(ramp) waveform generator circuit is given below. The left side pnp transistor is acts as a current source and charges the C5 capacitor. Whenever the voltage across this capacitor is greater than the U3 positive input capacitor is discharge through npn transistor Q5. The charge period of this capacitor is much larger than the discharge period. The total period of this waveform is almost same with the period of the converter. The output(voltage across C5) of this circuit given below.

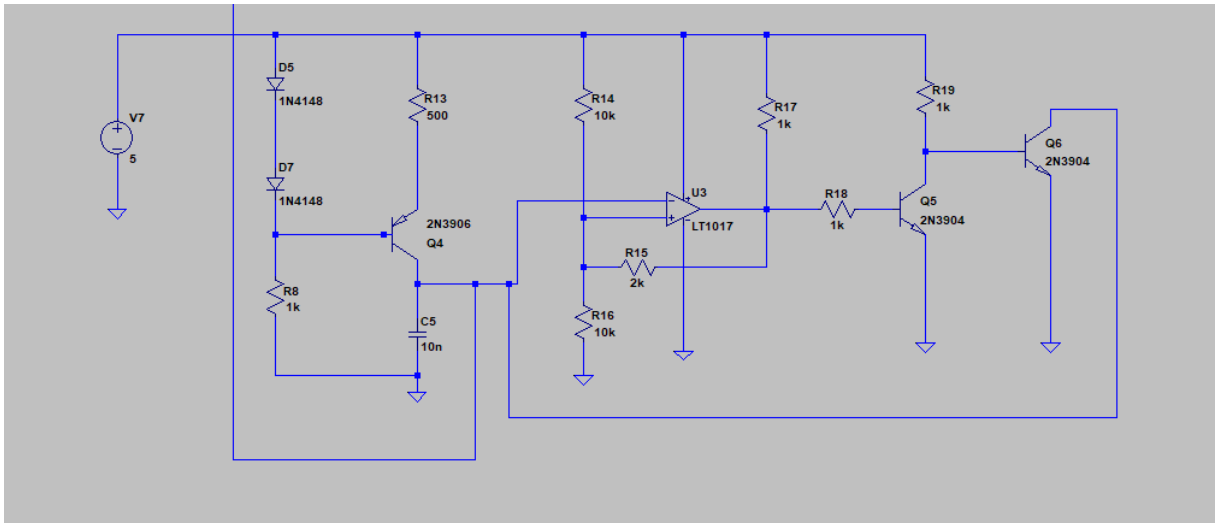


Figure 5.8 Sawtooth waveform generator schematic

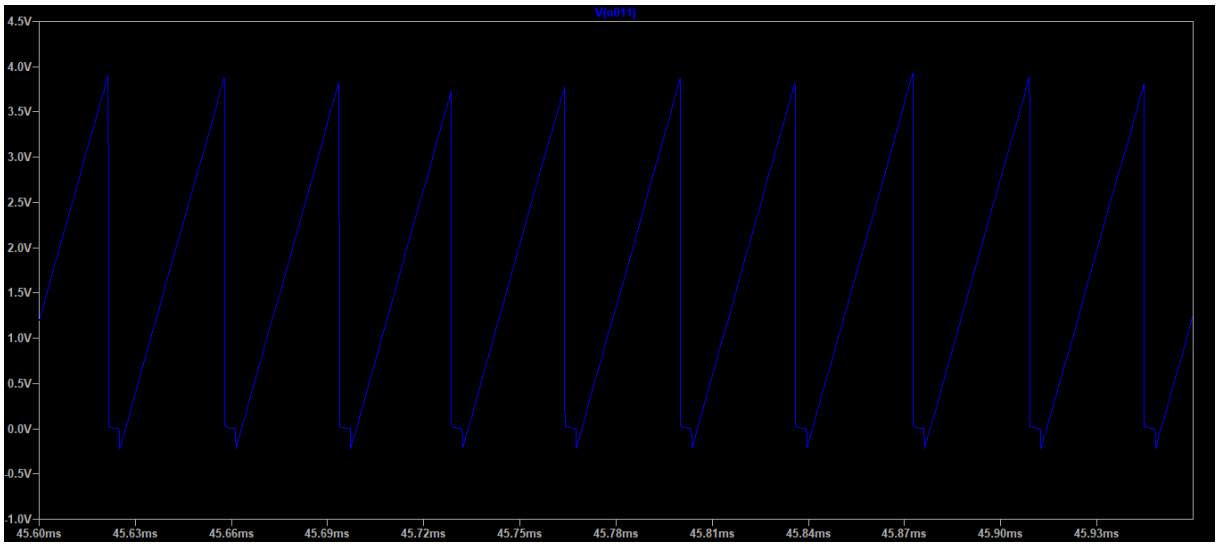


Figure 5.9 Sawtooth waveform with period of switch

5V DC voltage generation for IC's supply pins :

A 5V DC voltage is generated by using linear voltage regulator MIC29502BU is used as shown below.

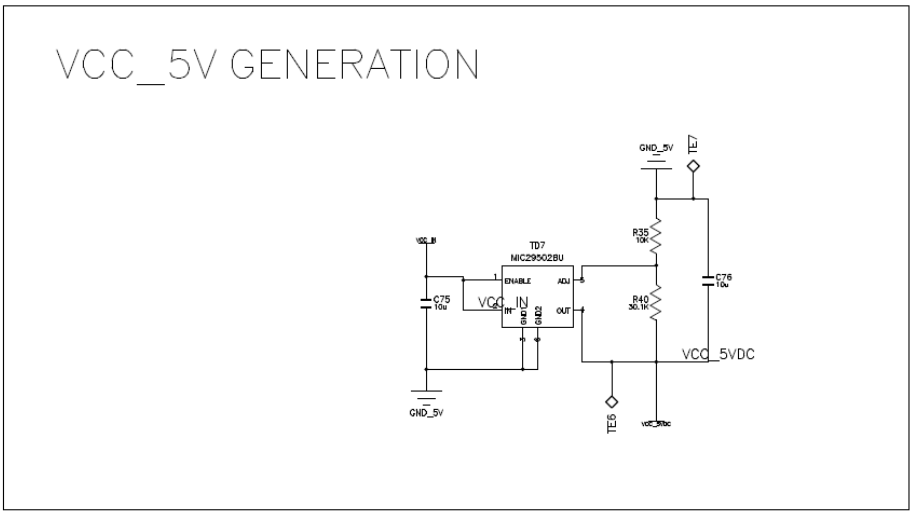


Figure 5.10 5V DC voltage generation

5.4 Gate Drive of Mosfet :

Isolated gate drivers are essential components for high side mosfet driver. ACNW3190 is used for gate driver. It has input, ouput and supply pins. Its minus supply pins connected to source of mosfet. And its positive supply pins are connected to the 15V + Vsource. To produce this source referenced isolated 15V, as shown below Figure 5.11, an isolated DC/DC converter is used. It is input is 5V and its output is 15V. They are isolated each other its output ground is connected to source of mosfet.

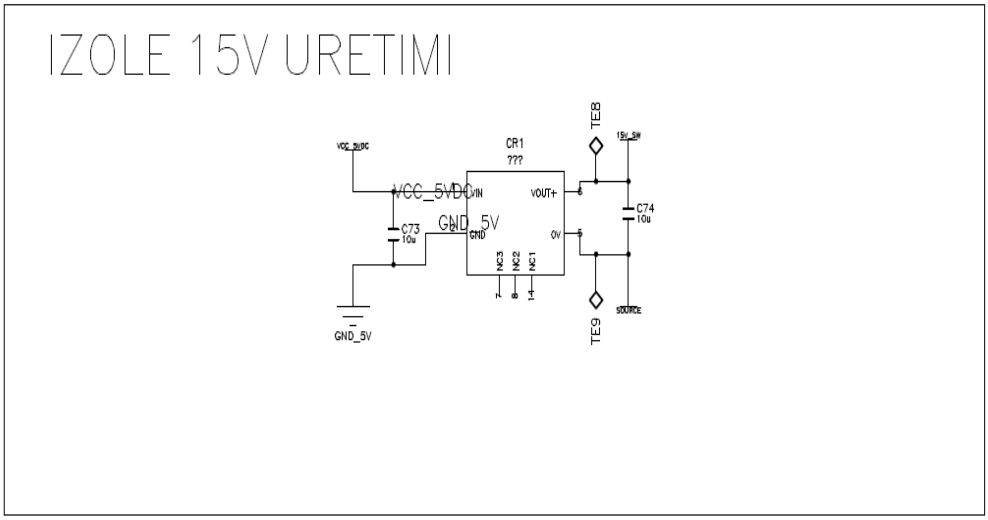


Figure 5.11 Isolated 15V generation for gate driver

The gate driver uses pwm signal as an input and gives 15V output referenced to source voltage i.e V_{GS} . It has output resistance to limit the current on the gate of mosfet. The schematic of gate driver shown below Figure 5.12 . The "PWM_OUT" signal is the output of output voltage control circuit. "PWM_OFF" signal is the output of output high voltage comparator.

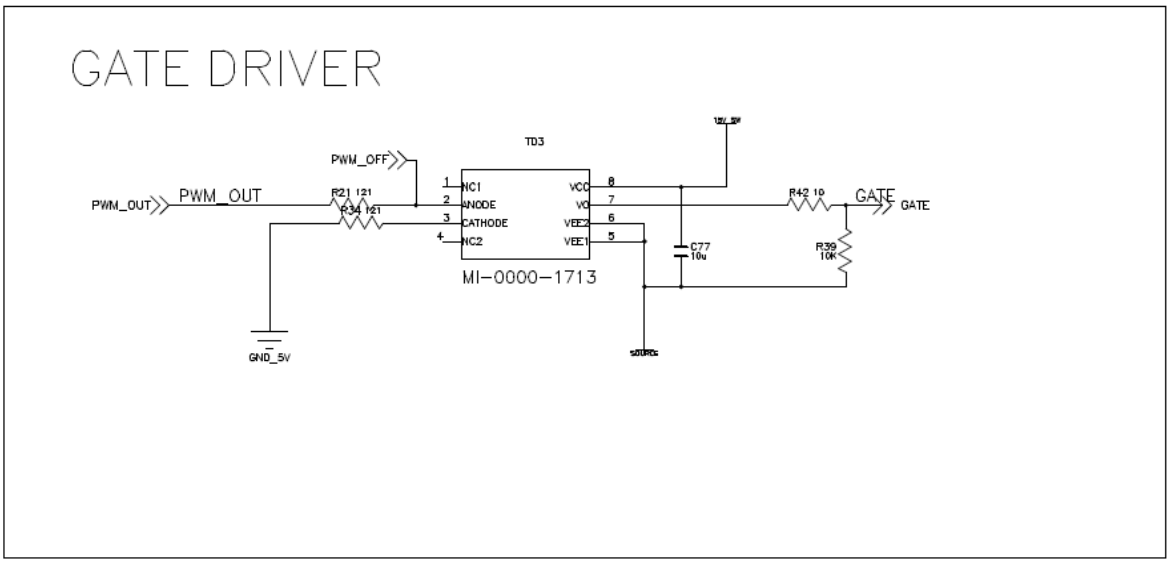


Figure 5.12 Gate driver schematic

6. SIMULATIONS

Computer simulation of the project is done using LTspice. Each part of project such as bridge rectifier, buck converter, output voltage controller, output high voltage protection are simulated seperately. The effect of output voltage controller to output voltage, output voltage set value's variations with changing potantiometer value, effect of the output high voltage comparator to output voltage are investigated.

6.1 Single Phase Full-Bridge Rectifier

The single phase full bridge rectifier circuit is shown below simulated in LTspice.

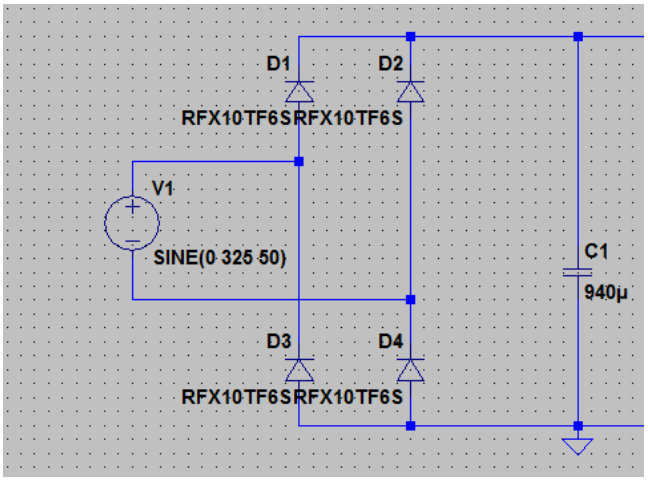


Figure 6.1 Circuit Schematic of Single-pase bridge rectifier

The output capacitors is charged to 325V initially and makes the output voltage constant DC as shown below.

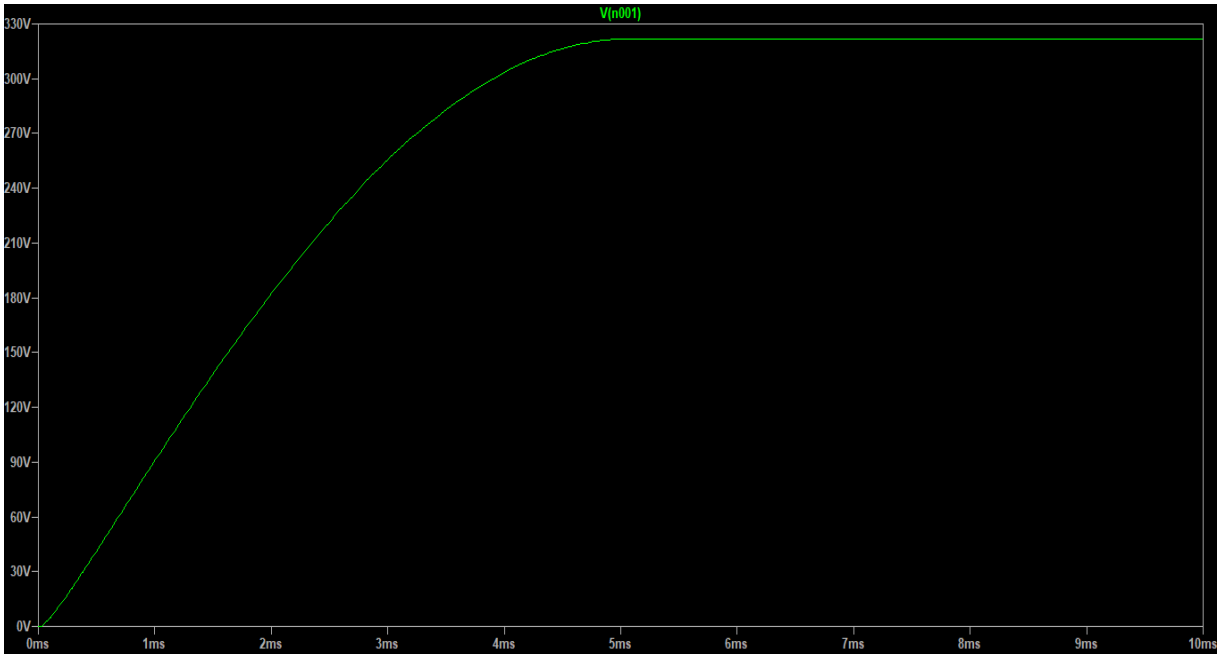


Figure 6.2 Output voltage waveform of bridge rectifier

6.2 Buck Converter

The overall circuit schematic is shown below Figure 6.2.1.

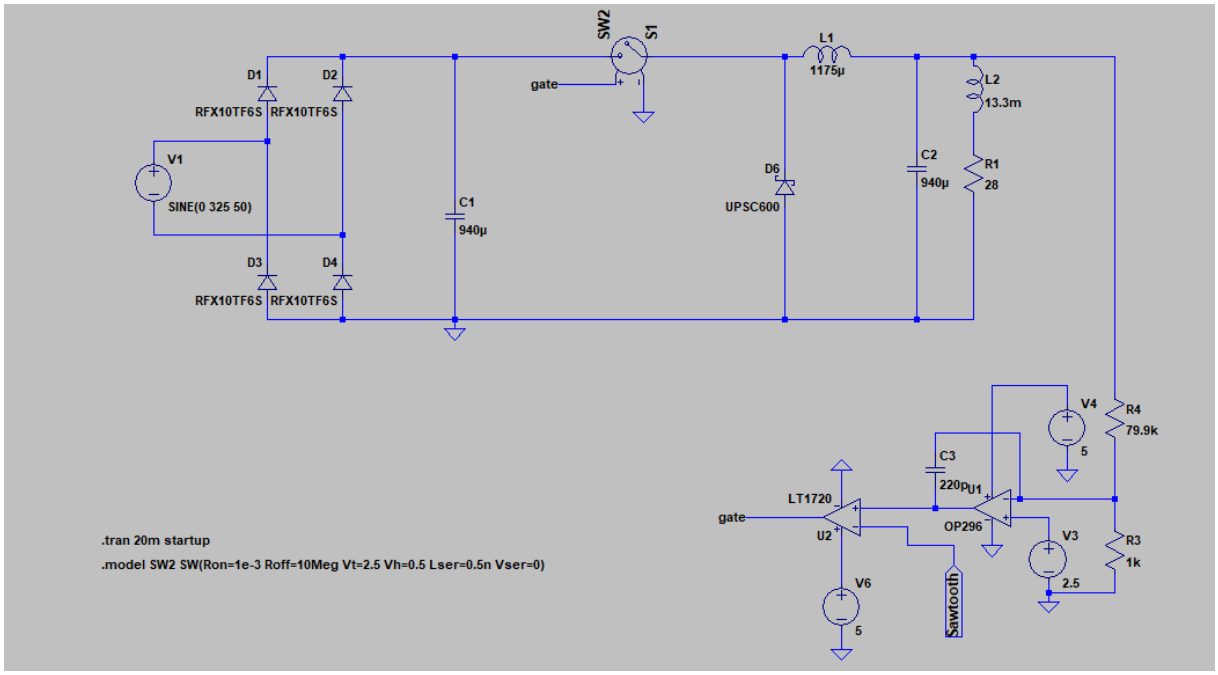


Figure 6.3 Overall circuit schematic of project

The output voltage of buck converter is shown below. Thanks to feedback loop, output voltage ripple is only 5V (%2.5) . The first overshoot is the due to start up. Initially, output capacitor is discharged and they are charged to 200V. Since the charged voltage is too high, they sinks large current and overshoot occurs.

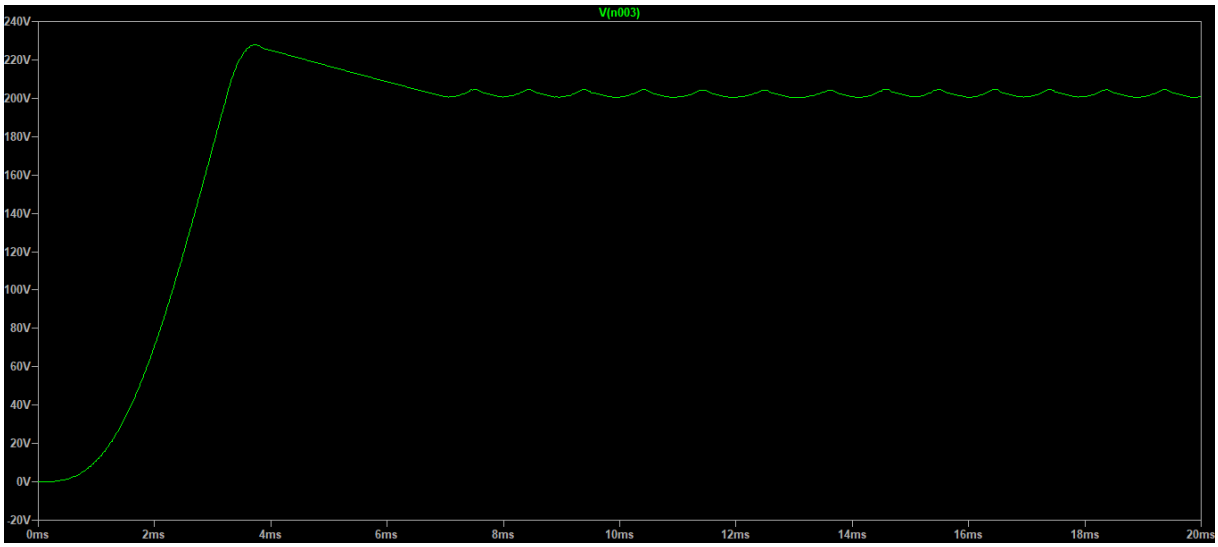


Figure 6.4 Output voltage waveform with feedback loop

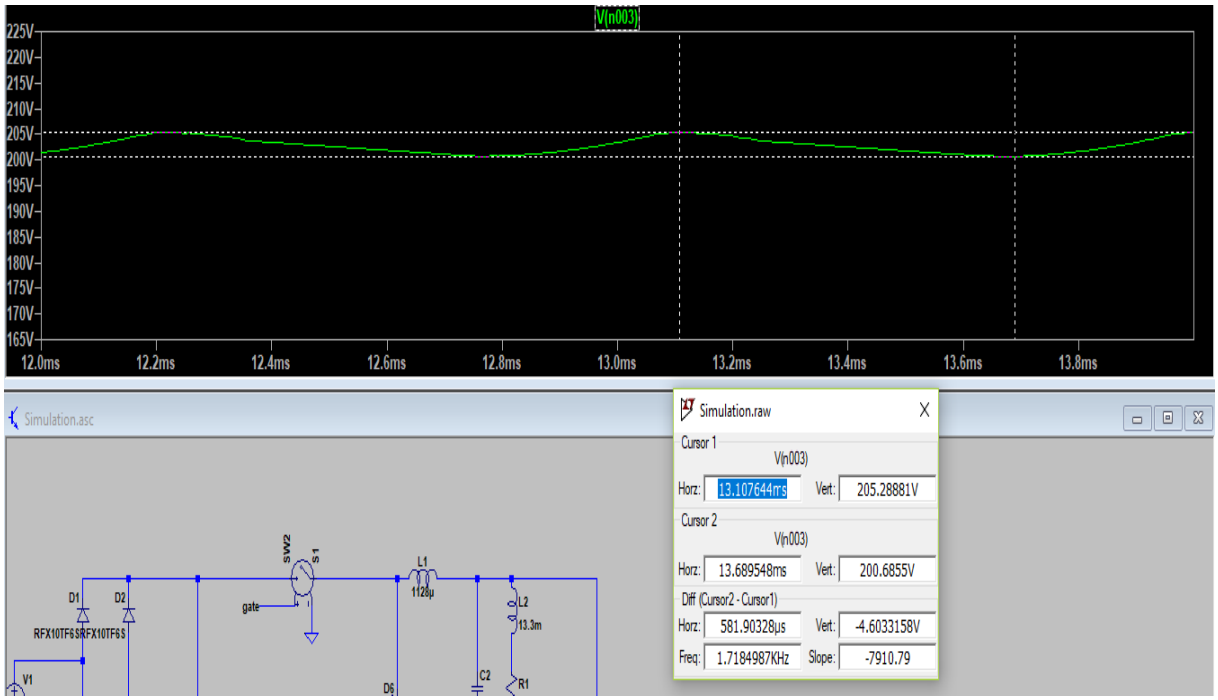


Figure 6.5 Output voltage ripple with feedback loop

6.2.1 Changing Reference Voltage V3

The reference voltage changes with potantiometer. As shown below, Vref is generated from below circuit. The voltage regulator TLVH413B is used to make the reference voltage constant.

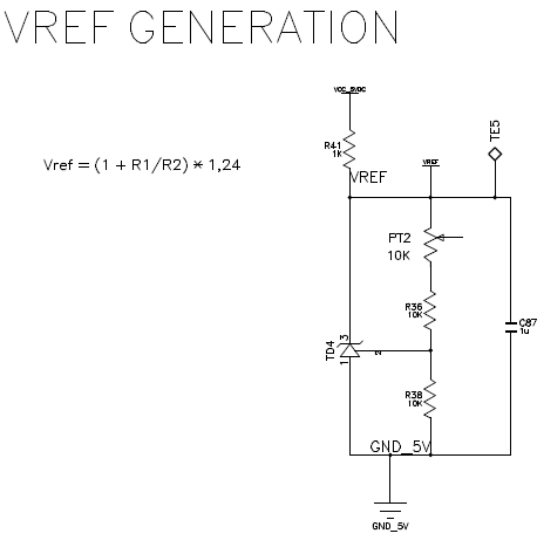


Figure 6.6 Reference voltage generation with potantiometer

Now, the set value of output voltage is reduced to 120V. Motor speed can be changed by this way.

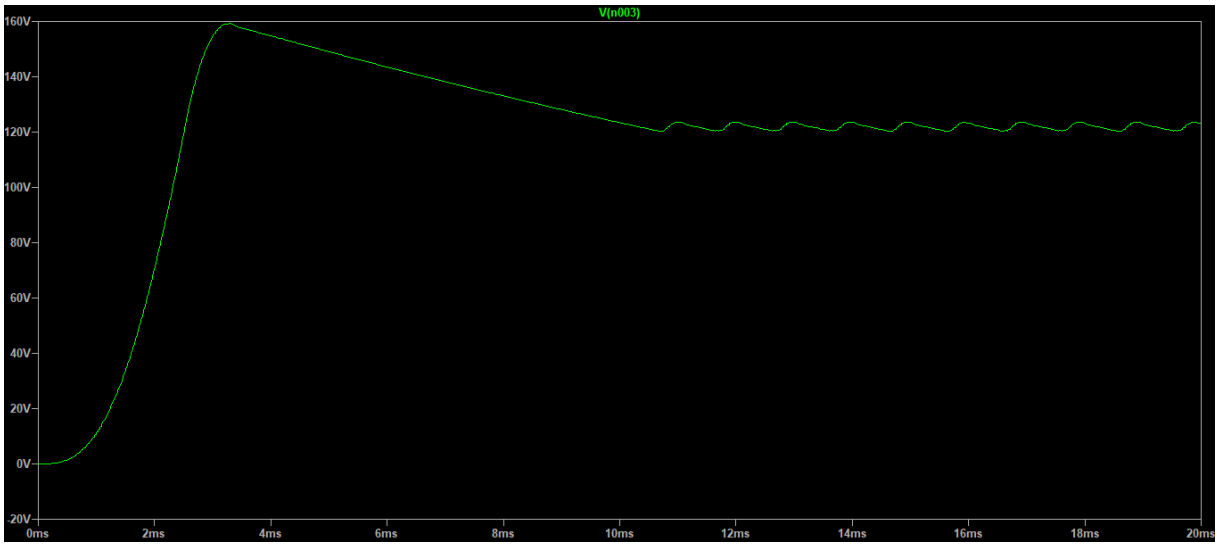


Figure 6.7 : Output voltage with different Vref

6.2.2 Output Voltage Control

The circuit shown below is a simple voltage control loop.

As seen from figure 6.9, output voltage is sampled with a resister divider and compared with a reference voltage then a waveform called error amplifier output is produced.

The output is error amplifier is compared with a sawtooth(ramp) waveform then a pwm signal is produced. Whenever, error amplifier output is greater than sawtooth waveform the output pwm signal is high(5V). Similarly, whenever error amplifier output is less than sawtooth waveform the output pwm signal is low(0V). This can be seen from figure 6.10 . This PWM signal is used as an input of gate driver to drive mosfet.

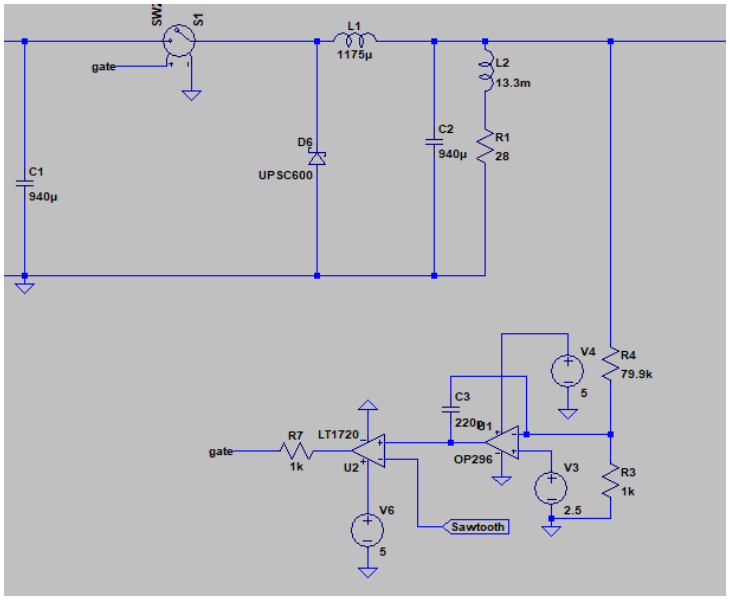


Figure 6.8 Ouput voltage control loop

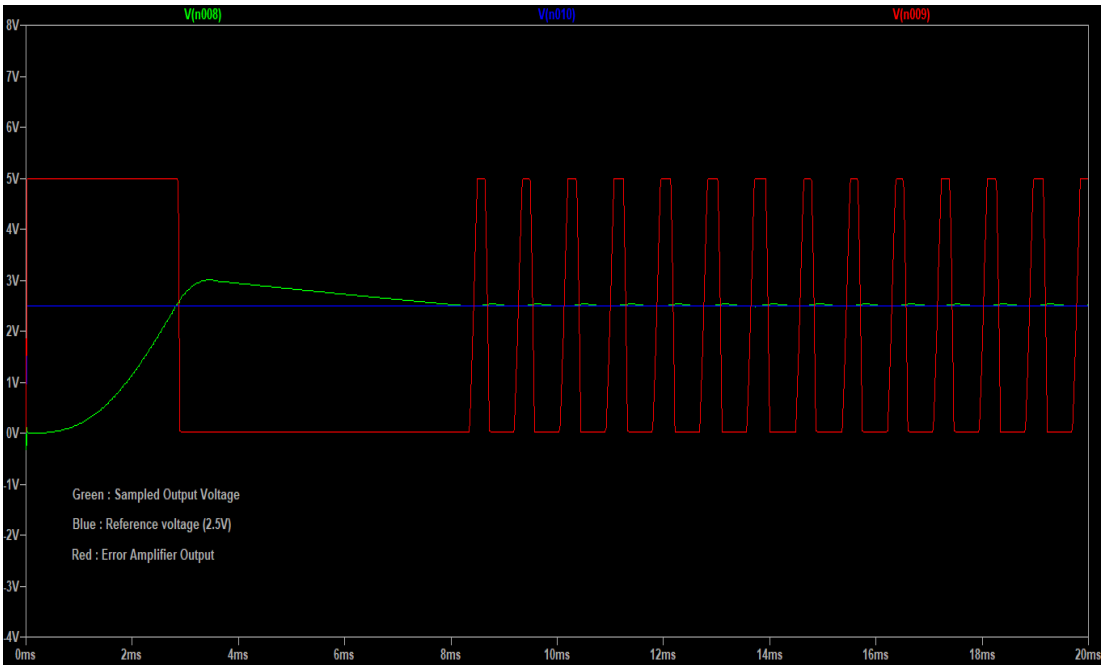


Figure 6.9 Opamp(U1) inputs and output waveforms

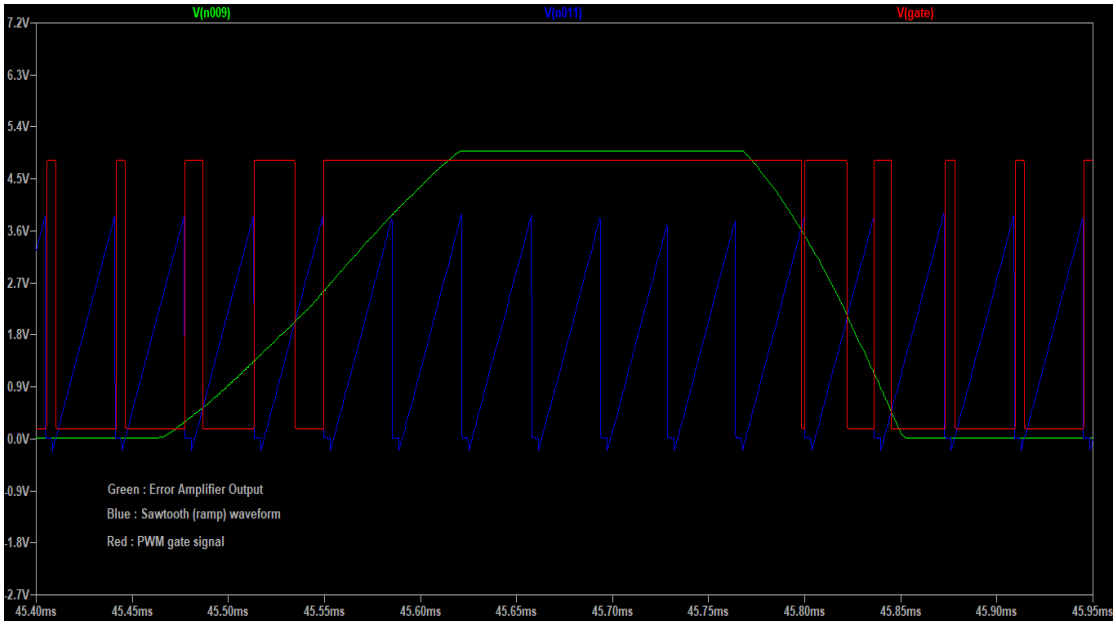


Figure 6.10 Comparator (U2) inputs and output waveforms

6.2.3 Output High Voltage Protection

To protect motor from high voltage, a high voltage comparator circuit is implemented. When output voltage exceeds the set voltage 225 V, comparator output (the pwm signal) goes zero i.e switch turns off.

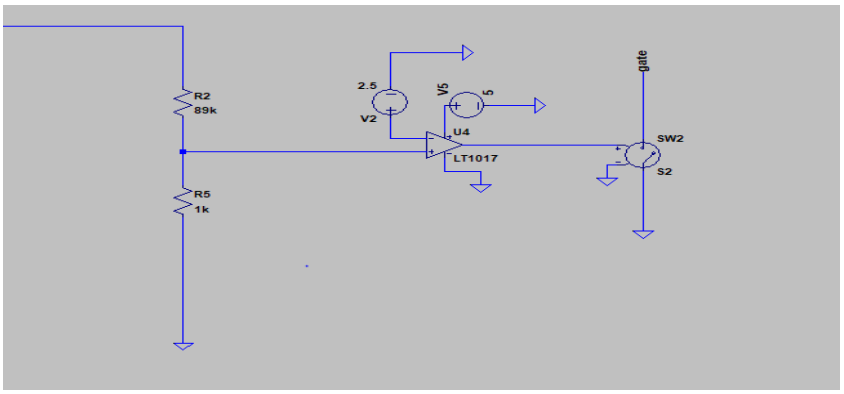


Figure 6.11 Output High Voltage Comparator

Without output high voltage protection the output voltage is shown below. As seen, it reaches to 240V. This voltage may be dangerous for motor.

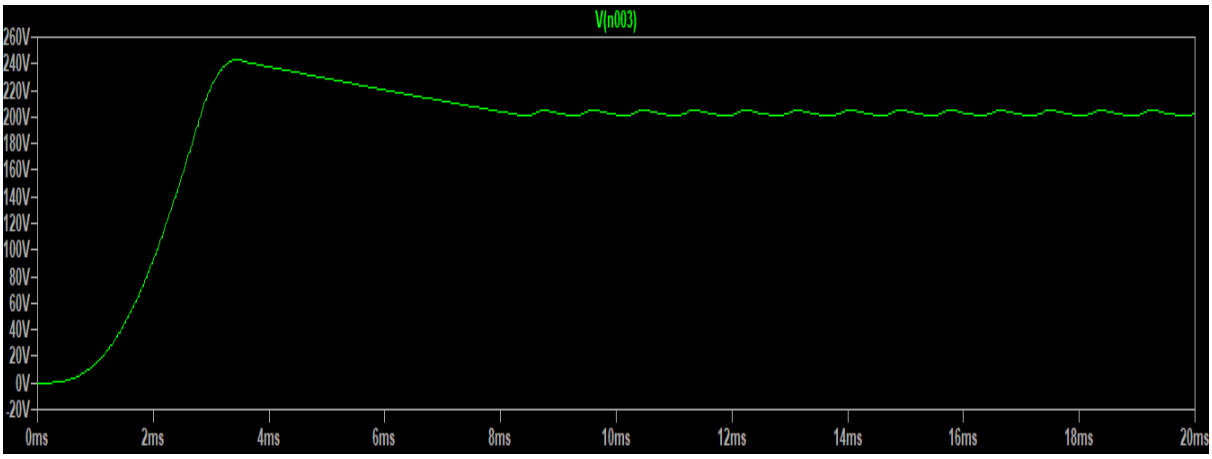


Figure 6.12 Output voltage waveform without high voltage comparator

By using output high voltage comparator, output voltage is limited below 230V as shown blow Figure 6.13 .

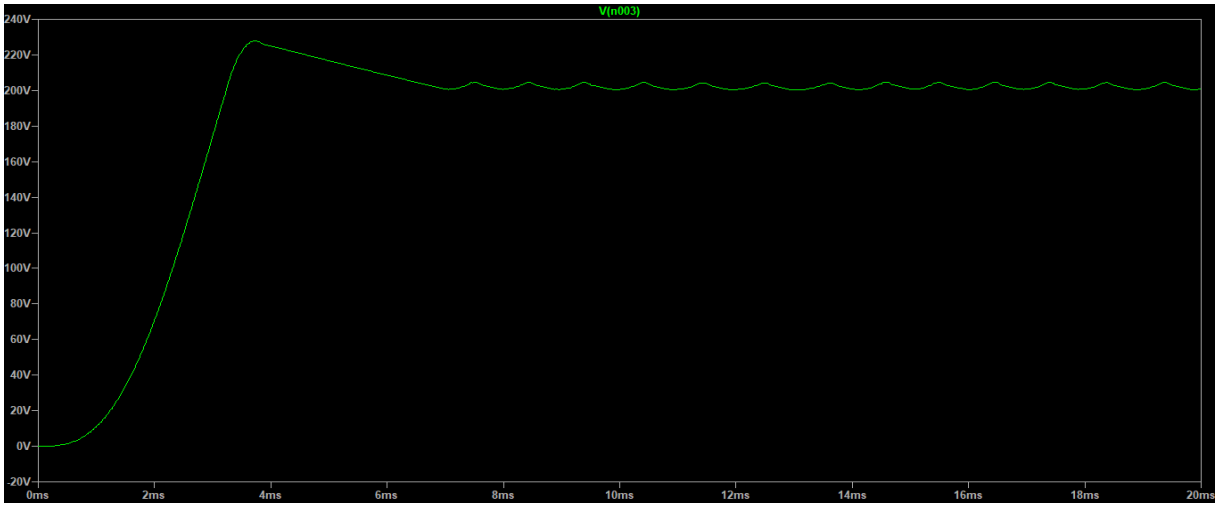


Figure 6.13 Output voltage waveform with high voltage comparator

When output voltage is higher than 225V, the PWM signal of gate driver is pulled down by this circuit. The output voltage and pwm signal of gate driver is given in same graph shown below Figure 6.14 .

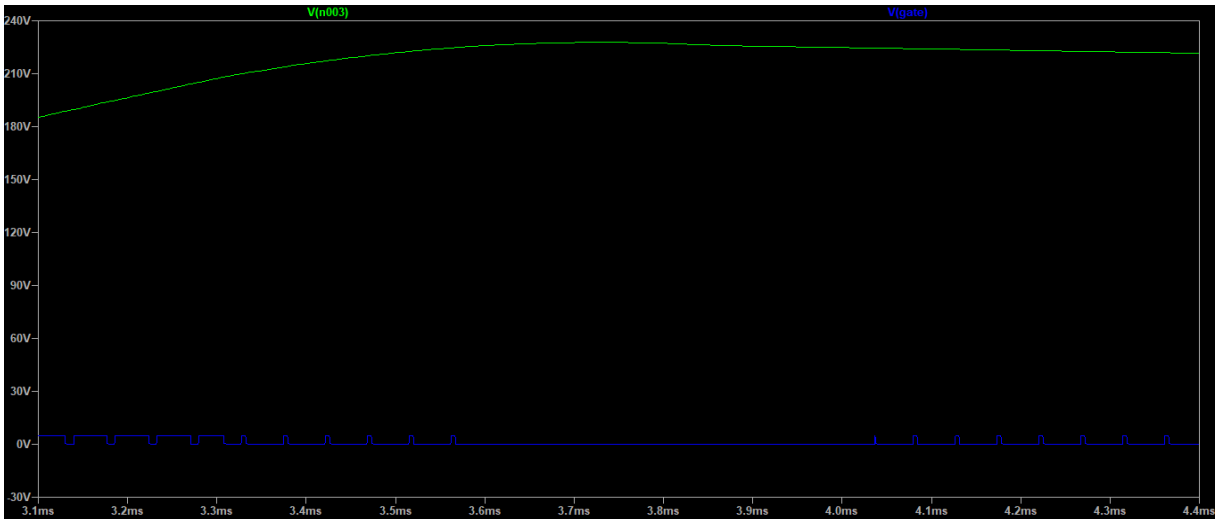


Figure 6.14 Output voltage waveform and pwm signal of gate driver

7. TEST RESULTS

The printed circuit design of this converter is implemented. The photos of this card shown below :

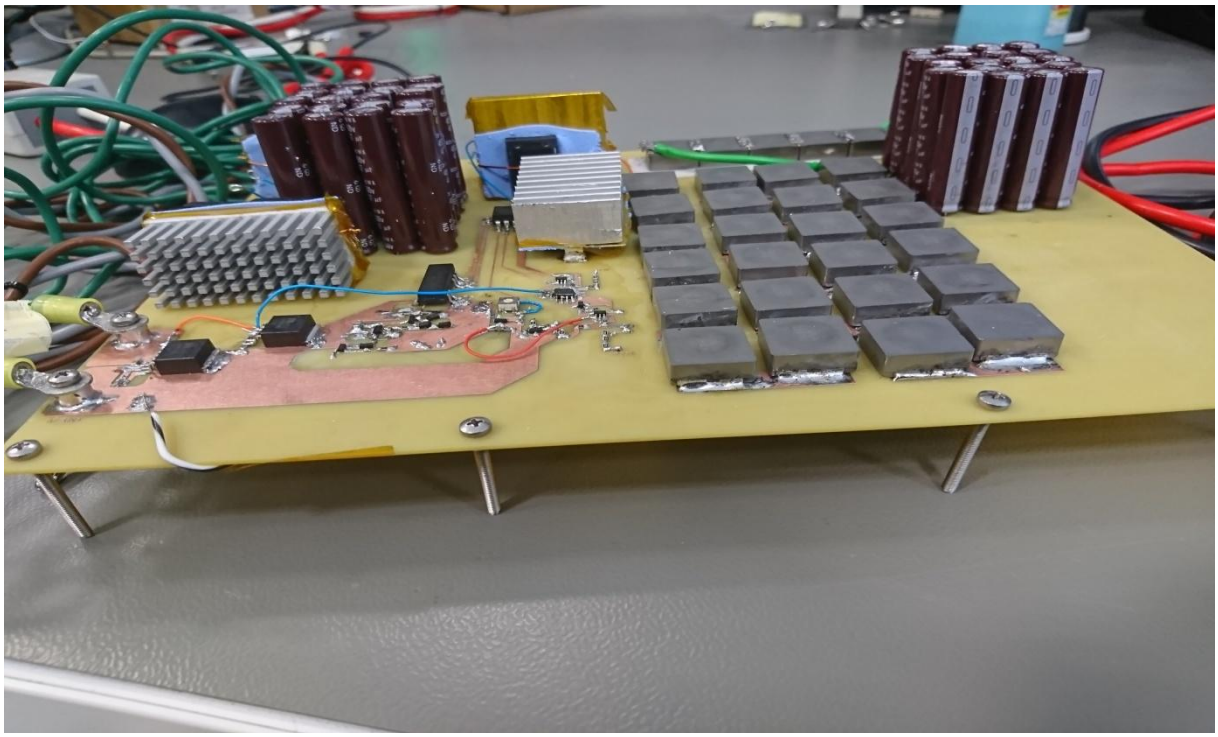


Figure 7.1 AC/DC Converter PCB

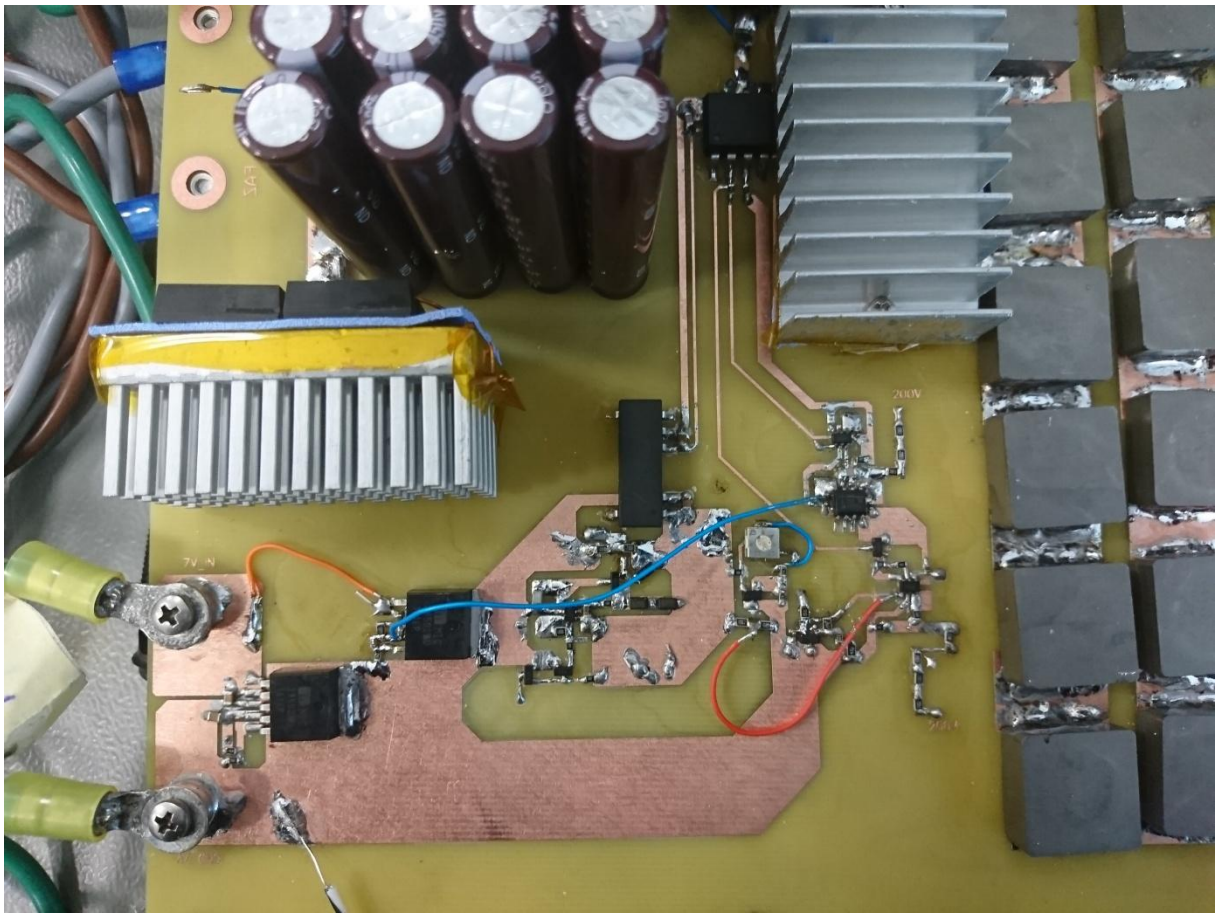


Figure 7.2 Control stage of converter

7.1 Without Input Power Maximum Duty Cycle Test :

In this test, input of this converted is not connected to source and only 7V DC input is connected. Then duty cycle of the converter is observed. As it can be seen from below Figure 7.3 ;

duty cycle is equal to 37/57.27 = 0,65 %

The yellow waveform (CH1) is the sawtooth waveform and its generated inside the converter. The blue waveform (CH2) is the output of error amplifier. Since, there is not output voltage i.e it is equal to zero, the error amplifier output is always logically high. The green waveform (CH4) is the V_{GS} voltage of the switch. When the sawtooth is greater than error amplifier output, the V_{GS} is 15V, otherwise it is 0V.

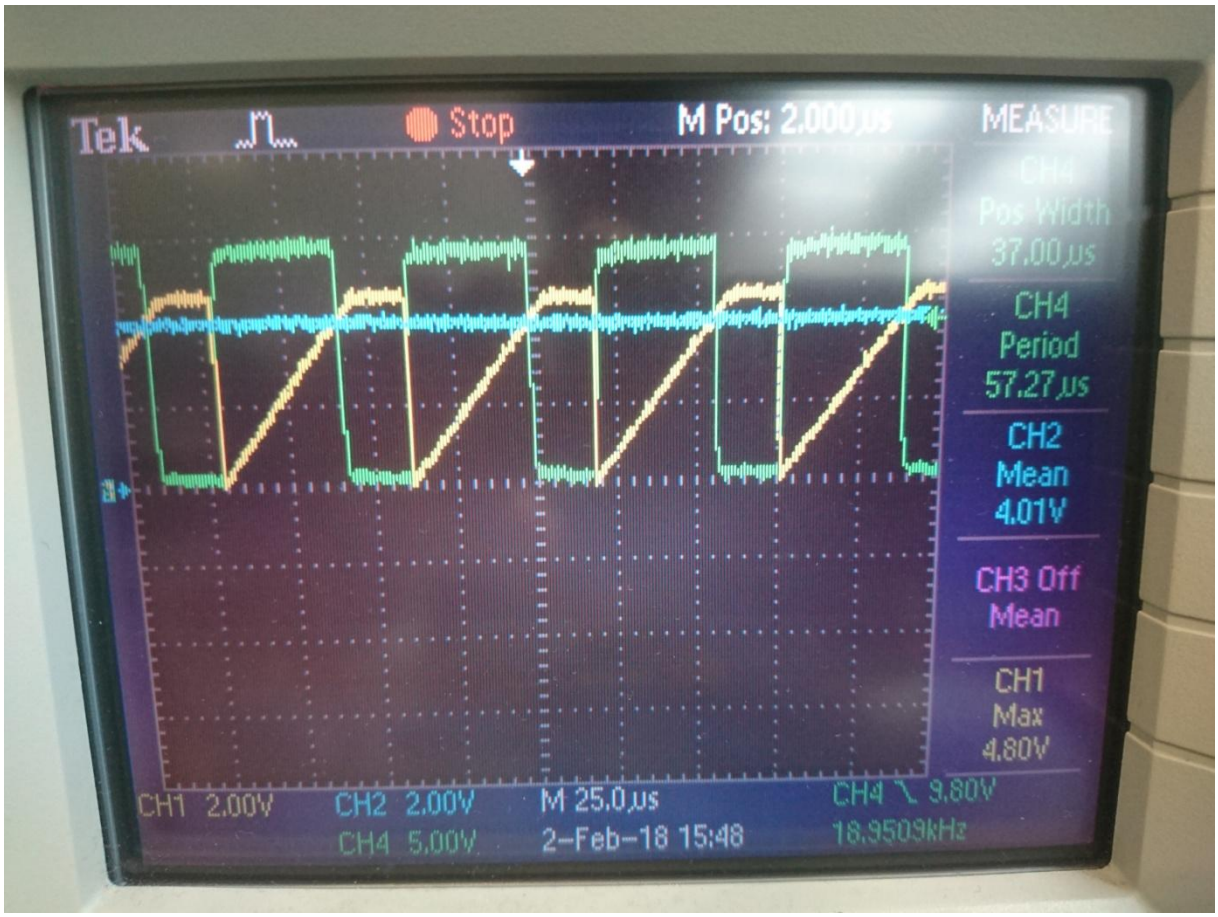


Figure 7.3 Duty cycle when output is disconnected

7.2 Load Test With Load Bank, Constant Load Current :

<u>For 50Vrms input voltage :</u>

For 50Vrms input voltage the output voltage is observed and duty cycle is calculated. This test is conducted for 1A,2A and 3A output current.

The duty cycle is equal to 80% for 50Vrms input and 1A load current, the oscilloscope screenshot is shown below in Figure 7.4 .

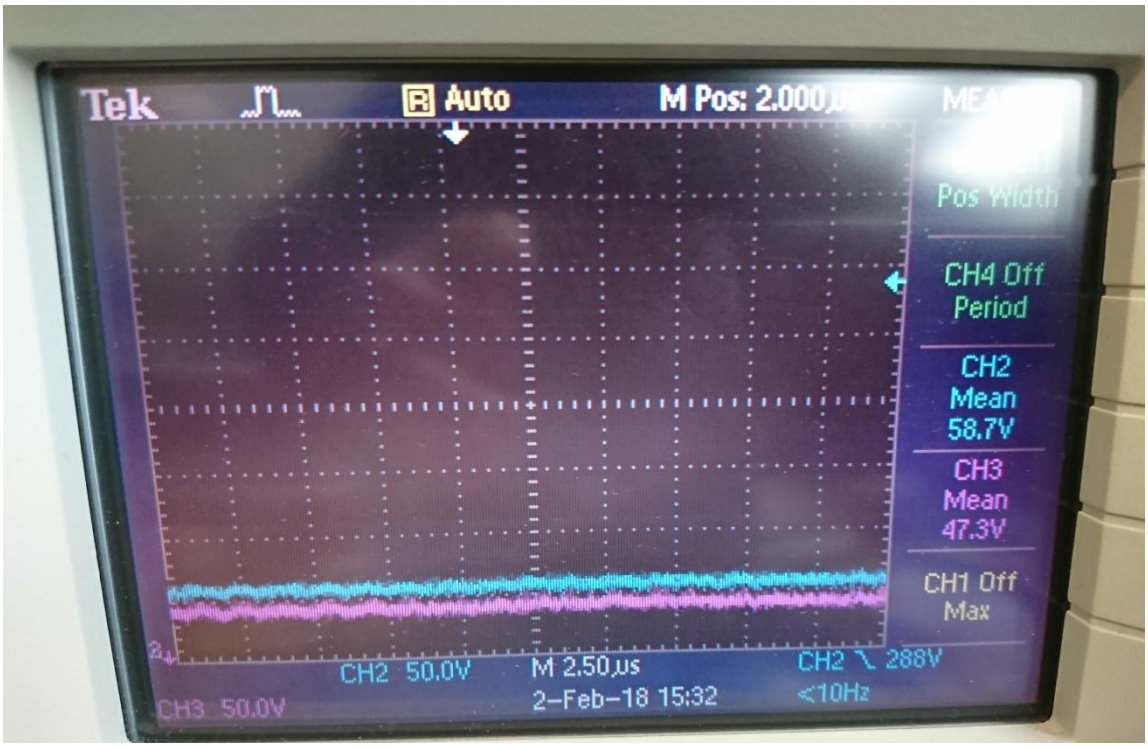


Figure 7.4 Input(CH2) and output voltage waveforms(CH3) for 50Vrms input and 1A load current

The duty cycle is equal to 82% for 50Vrms input and 2A load current, the oscilloscope screenshot is shown below in Figure 7.5 .

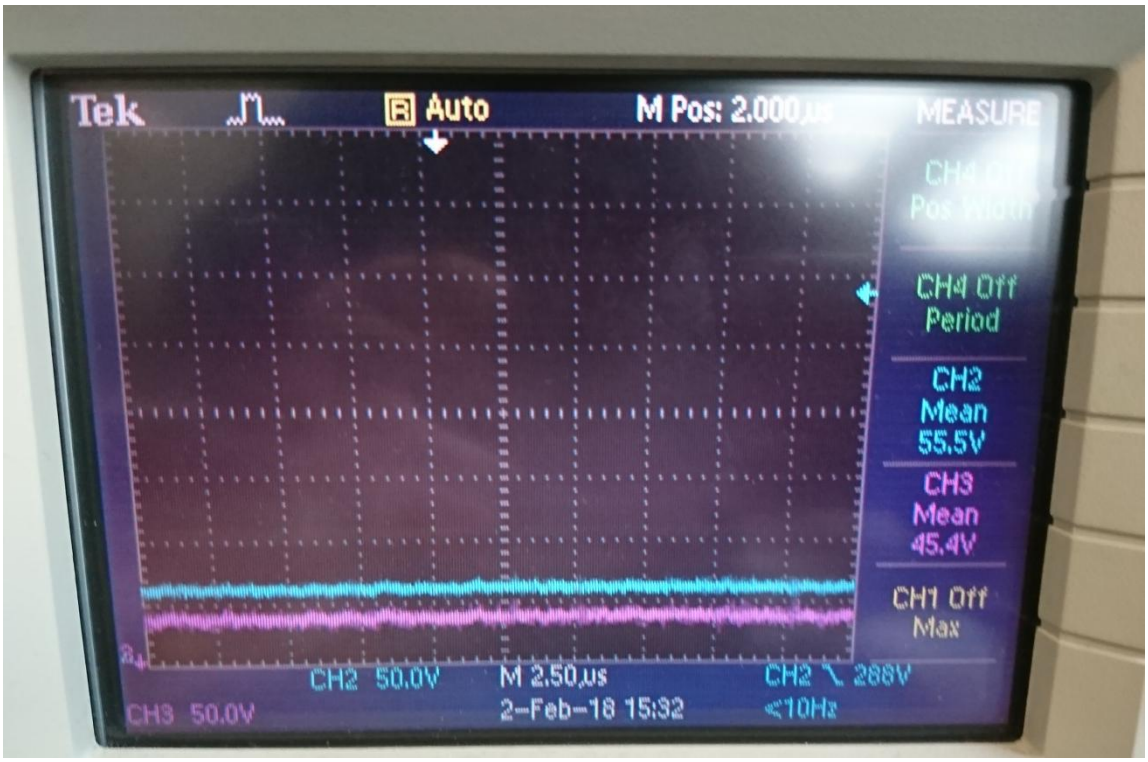


Figure 7.5 Input(CH2) and output voltage waveforms(CH3) for 50Vrms input and 2A load current

The duty cycle is equal to 81% for 50Vrms input and 3A load current, the oscilloscope screenshot is shown below in figure 7.6 .

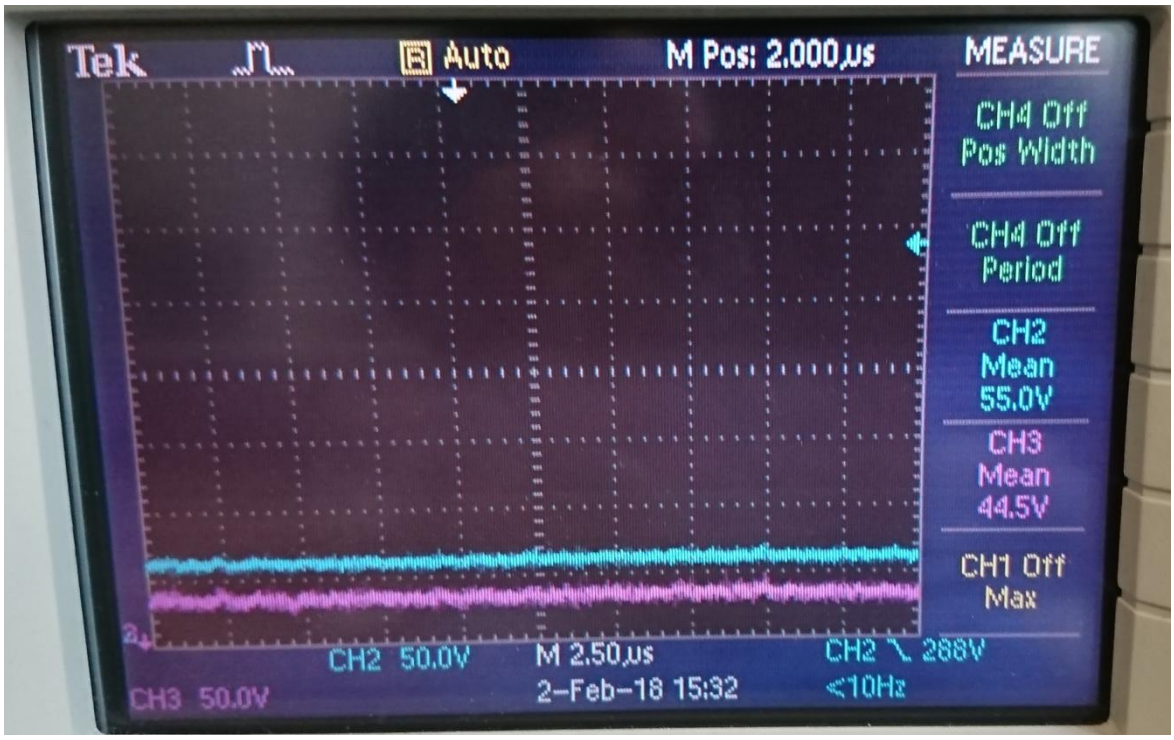


Figure 7.6 Input(CH2) and output voltage waveforms(CH3) for 50Vrms input and 3A load current

For 150Vrms input voltage :

For 150Vrms input voltage the output voltage is observed and duty cycle is calculated. This test is conducted for 1A,2A and 3A output current.

The duty cycle is equal to 71% for 150Vrms input and 1A load current, the oscilloscope screenshot is shown below in Figure 7.7 .

Figure 7.7 Input(CH2) and output voltage waveforms(CH3) for 150Vrms input and 1A load current

The duty cycle is equal to 72% for 150Vrms input and 2A load current, the oscilloscope screenshot is shown below in Figure 7.8 .

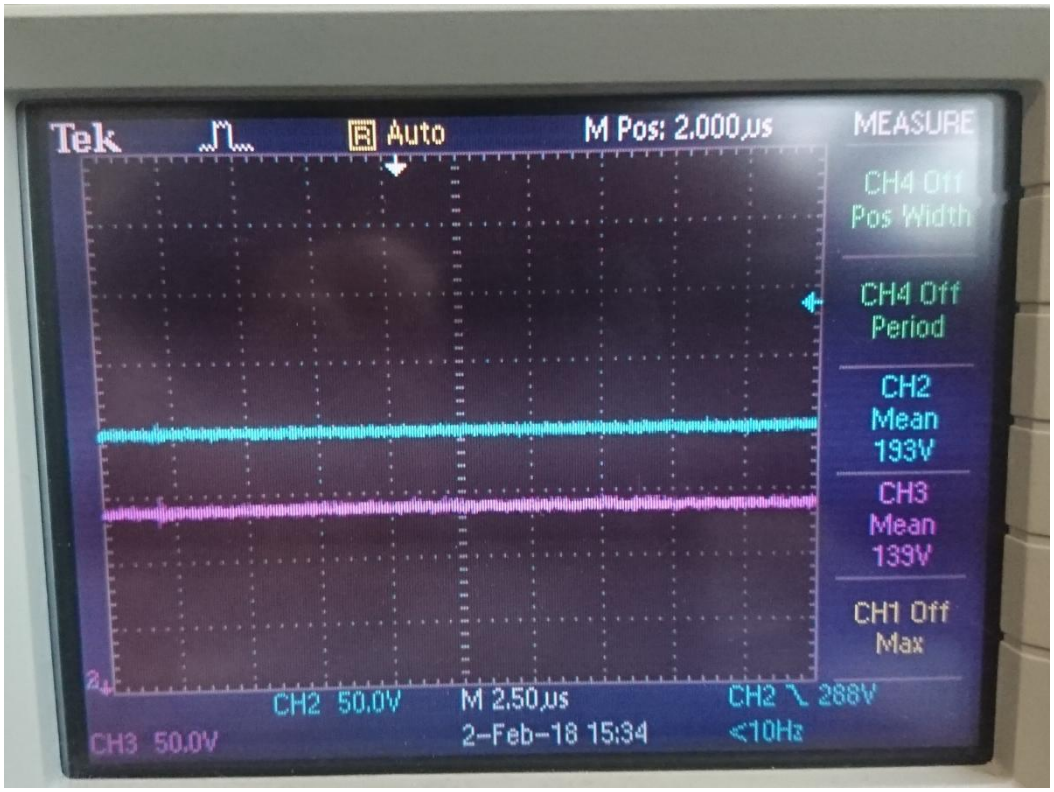


Figure 7.8 Input(CH2) and output voltage waveforms(CH3) for 150Vrms input and 2A load current

The duty cycle is equal to 69% for 150Vrms input and 3A load current, the oscilloscope screenshot is shown below in Figure 7.9 .

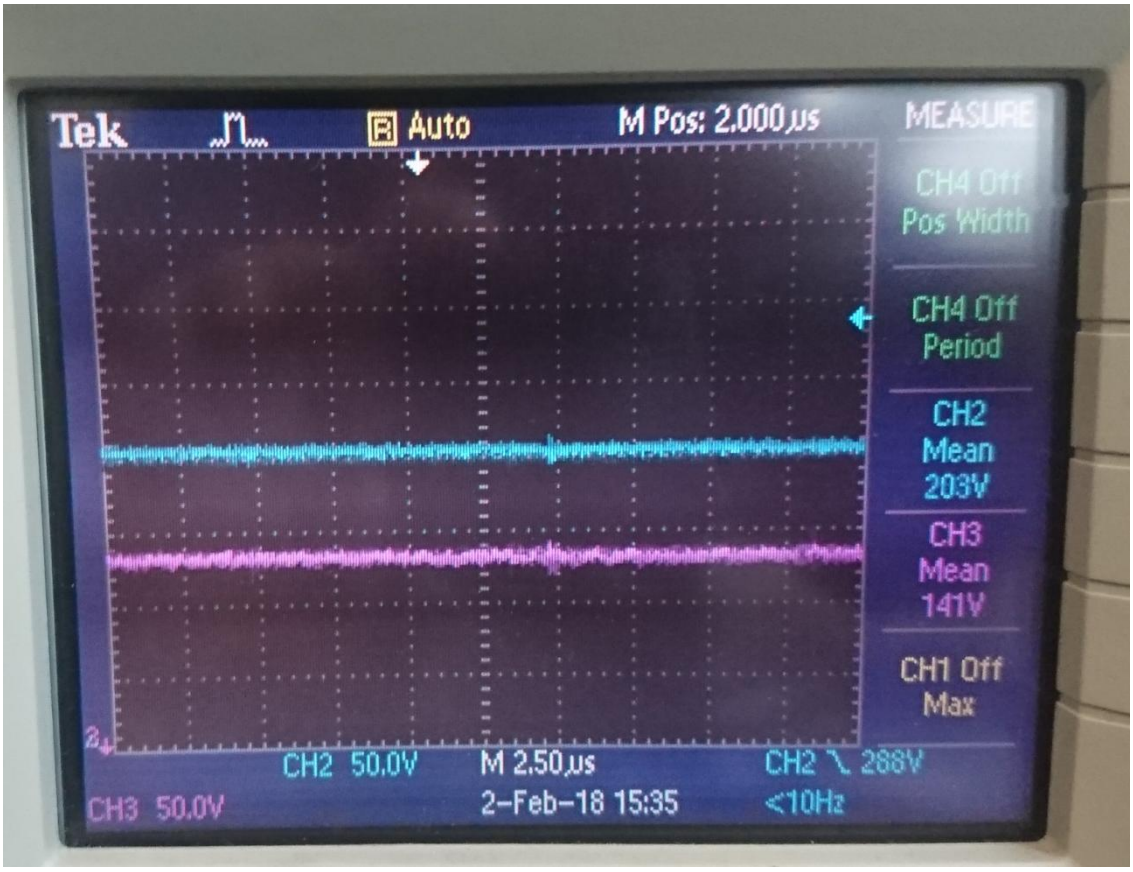


Figure 7.9 Input(CH2) and output voltage waveforms(CH3) for 150Vrms input and 3A load current

<u>For 230Vrms input voltage :</u>

For 230Vrms input voltage the output voltage is observed and duty cycle is calculated. This test is conducted for 1A,2A and 3A output current.

The duty cycle is equal to 72% for 230Vrms input and 1A load current, the oscilloscope screenshot is shown below in Figure 7.10 .

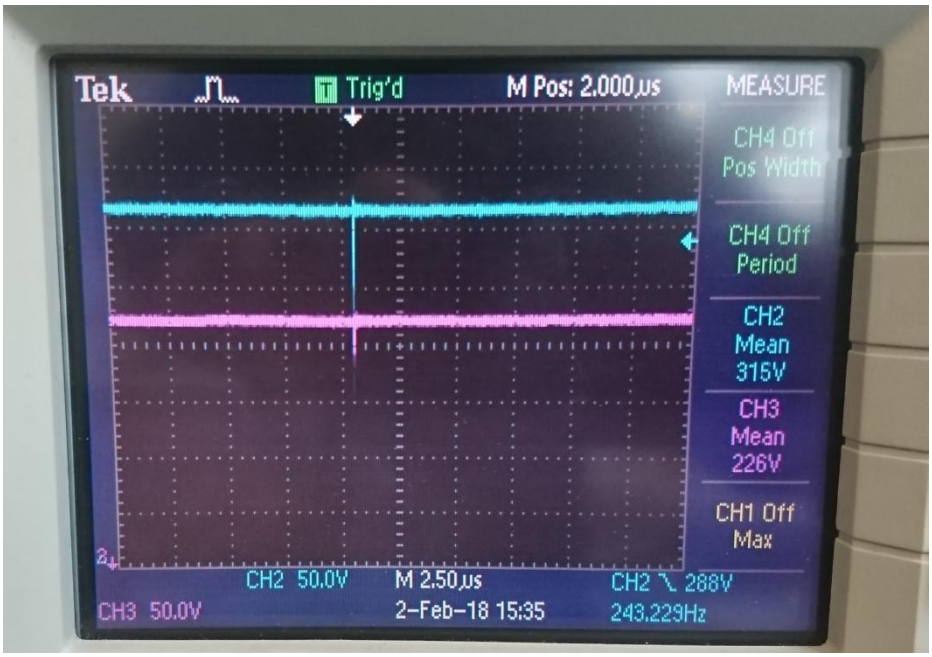


Figure 7.10 Input(CH2) and output voltage waveforms(CH3) for 230Vrms input and 1A load current

The duty cycle is equal to 71% for 230Vrms input and 2A load current, the oscilloscope screenshot is shown below in Figure 7.11 .

Figure 7.11 Input(CH2) and output voltage waveforms(CH3) for 230Vrms input and 2A load current

The duty cycle is equal to 71% for 230Vrms input and 3A load current, the oscilloscope screenshot is shown below in Figure 7.12 .

Figure 7.12 Input(CH2) and output voltage waveforms(CH3) for 230Vrms input and 3A load current

7.3 Motor Test Under Noload For Maximum Duty Cycle :

In this test the motor shown below in Figure 7.13 is connected to output of converter. Then duty cycle of switch, motor voltage and motor current are observed.

Figure 7.13 2.8 kW DC Motor

The output voltage is adjusted to motor rating voltage motor is not connected to any load. The motor voltage and motor current given below are 200V and 2.5A respectively.

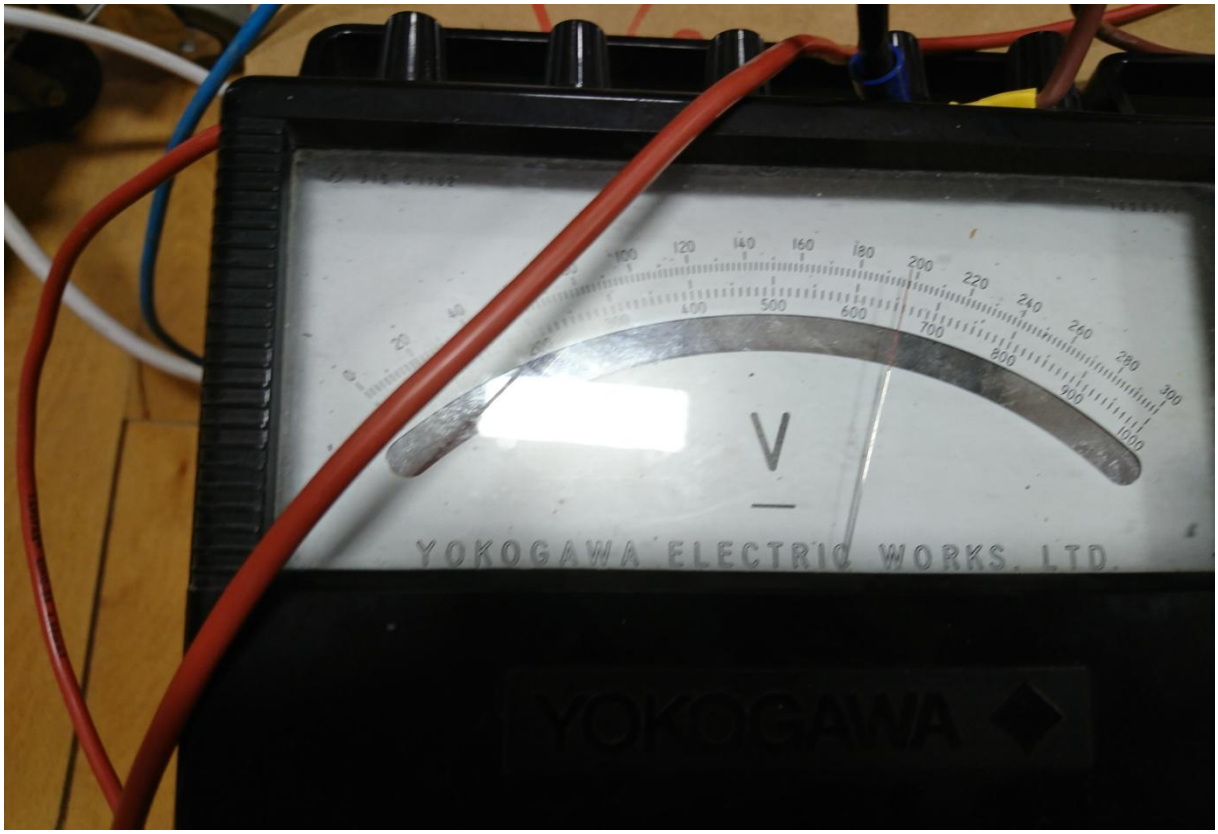


Figure 7.14 Motor voltage : 200V

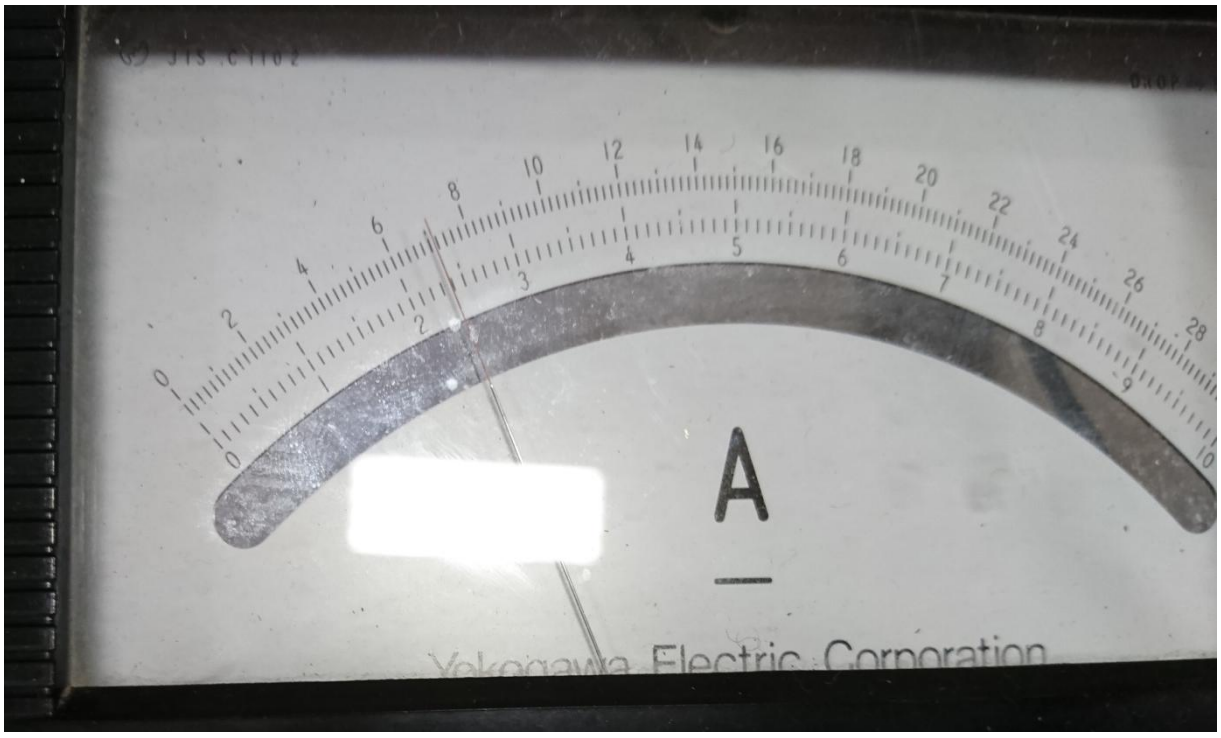


Figure 7.15 Motor current : 2.5A under noload

The duty cycle of the switch is observed on oscilloscope screen given below. It is 60.97%.

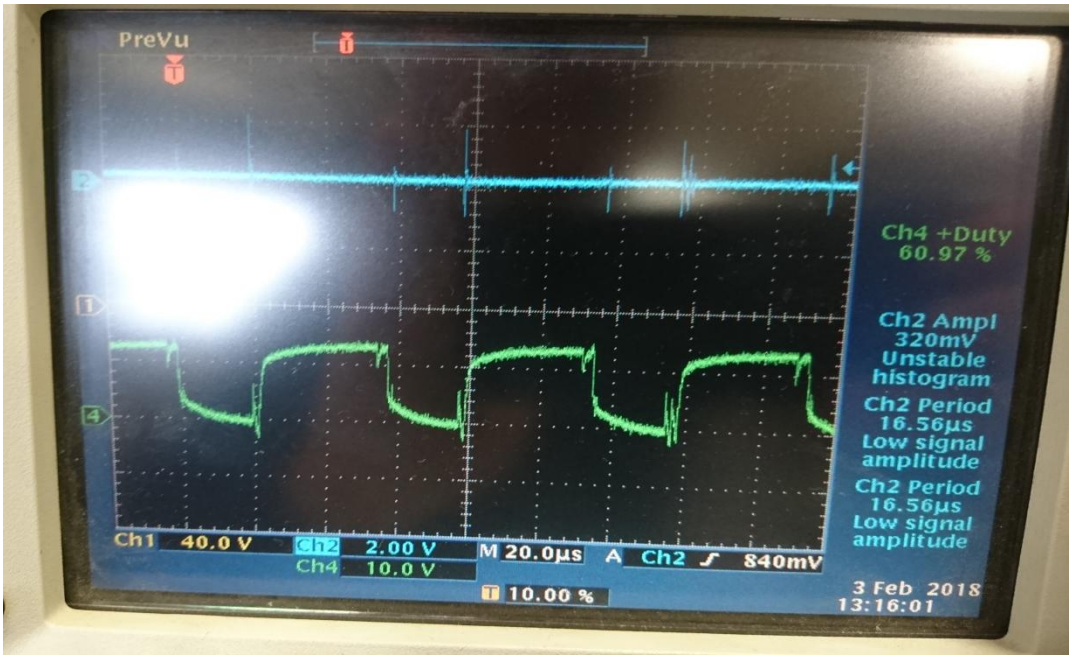


Figure 7.16 Duty cycle of switch under noload.

7.4 Motor Test Under Noload For Minimum Duty Cycle :

The duty cycle is adjusted to minimum value by changing potantiometer value. For this case, the motor voltage is 150V and motor current is 2A.

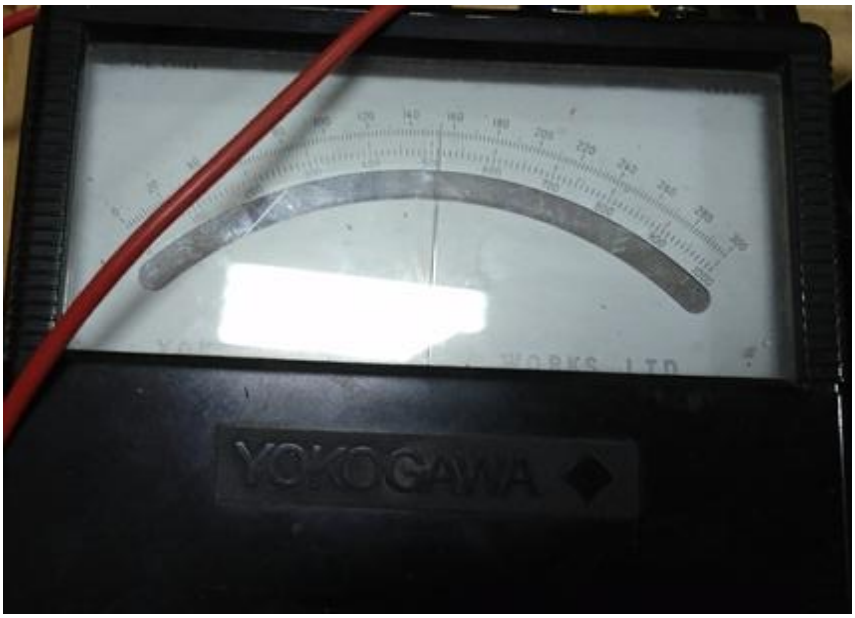


Figure 7.17 Motor voltage : 150V for minimum duty cycle

Figure 7.18 Motor current : 2A for minimum duty cycle

8. CONCLUSION

In this project, a AC/DC converter is implemented. As an input, phase voltage of grid used. To convert AC to DC full bridge rectifier is impelemented. As an switching DC/DC converter, buck converter is implemented. Buck converter components such as inductor,capactior are calculated. Also, other components are selected appropriate with project specifications.

In buck converter, input supplies current to both the inductor and load when the switch is on. When the switch is off, inductor supplies the current to load. So, there will be ripple in the inductor current. This ripple should not exceeds inductor saturation current otherwise inductance may be degrade. The FWD diodes conducts when switch is off and carries inductor current. So, it must be selected appropriate for continuous current carrying capability.

Without voltage control loop, the output of buck converter may be unstable. Even, there will be overshoot when the switch turning on and off. The control loop consist of error amplifier and pulse width modulator. The error amplifier compares output voltage with reference voltage. Pulse width modulator compares error amplifier output with sawtooth waveform then produce pwm signal to the gate driver input.

Isolated gate drivers are essential components for high side mosfet driver. It has input, ouput and supply pins. Its minus supply pins connected to source of mosfet. And its positive supply pins are connected to the 15V + Vsource. To produce this 15V, source referenced isolated voltage an isolated DC/DC converter is used. It is input is 5V and its output is 15V. They are isolated each other its output ground is connected to source of mosfet.

A PCB is designed. In PCB design, there are some points which are important. One of them is that by pass capacitor should be connected as close as possible to the corresponding IC. The another one, plane or trace should be large to carry high current. And also, output voltage traces connected to output voltage controller circuit should be as far as possible to switching node since there will be noise in the switching node.

9. APPENDICES

1. Power Stage Designer User's Guide - Texas Instruments from

   www.ti.com/lit/pdf/slvubb4

2. Understanding Buck Power Stages In Switchmode Power Supplies from

   www.ti.com/lit/an/slva057/slva057.pdf

3. ACNW3190 Gate Driver from www.farnell.com/datasheets/76300.pdf
4. TLV3501 ultrafast comparator from www.ti.com/lit/ds/sbos533b/sbos533b.pdf
5. ISJ0515A DC/DC converter from www.xppower.com/Portals/0/SF_ISJ.pdf
6. MIC29502BU Linear Voltage Regulator from
   ww1.microchip.com/downloads/en/.../20005685A.pdf
7. STY145N65M5 Power mosfet 650V-139A from
   www.st.com/resource/en/datasheet/sty145n65m5.pdf