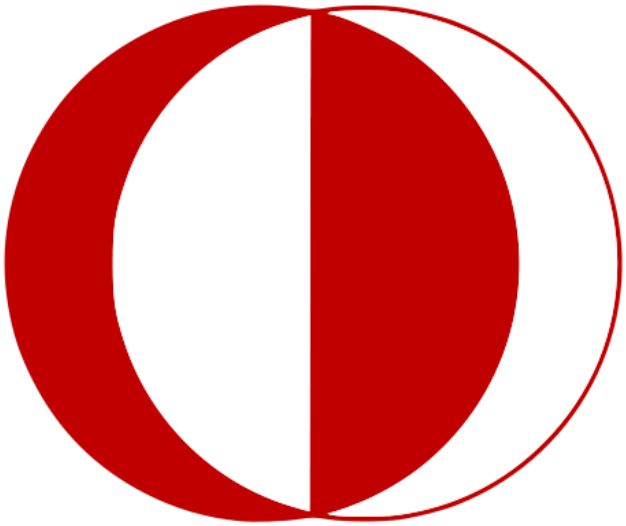

MIDDLE EAST TECHNICAL UNIVERSITY

2018

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EE464 Static Power Conversion-II

Hardware Project Report

Forward Converter Design

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1 INDEX

2 INTRODUCTION

Converters are used for changing the DC voltage level to another one and they are used widely in electronic applications. For example, voltage level of batteries in the cellphones are changed via using DC/DC converters in order to obtain different voltage levels. The other example is that line voltages in the commercial areas are converted via using AC/DC converters in order to obtain desired voltage levels. Since these converters are generally used before electronic circuits, some specific features of these converting circuits must be well designed such as efficiency, voltage ripples, harmonic component generations.

The one−transistor forward converter is the most elementary form of transformer−isolated buck converter. It is typically used in off−line applications in the 100 W − 300 W region. This report note illustrates the approach one would take to design a 48V input 28V/100W output, one−transistor forward converter. Since there is always possibility of fluctuations on the input voltage level and change in the load, a control circuit can be implemented to check whether the output voltage level is applicable. Because of this reason in addition to forward converter, a controller from Texas Instruments named uc1845 is used.

Moreover, after deciding circuit elements and performing necessary tests, we design a PCB circuit. It enables us to obtain more robust and stable product. In the last step we add a cooling fan and heatsink in case of any heating problems. Cooling fan and heatsinks lead our product to work longer time periods.

3 FORWARD CONVERTER

3.1 Theoretical Calculations

Schematic of the forward converter is on the following figure 1. One can see a transformer has been placed between the input voltage and a buck converter output stage. The power switch (SW) is used to create a rectangular voltage waveform whose amplitude is the input voltage and its duty cycle is the controllable variable. The transformer provides both a step−up or down function and a safety dielectric isolation between the input line and the output load. The major restriction of this topology is the maximum duty cycle must be about 50%. Whenever a core is driven in a unidirectional fashion, that is, current only being driven from one direction into the primary, the core must be reset. Magnetization energy which serves only to reorient the magnetic domains within the core must be emptied, or else the core will “walk−up” to saturation after a few cycles. To do this, one needs to reset the core. Resetting is done by drawing current from a winding during the period when the transformer is unloaded, that is, when the power switch and rectifiers are not conducting. Any winding can provide the reset function, but the higher the voltage on the winding, the quicker the core will reset. Typically, this is the primary winding or a separate reset winding of equal turns to the primary. Current from the reset winding can then be returned to the input capacitor and reused during the next cycle of operation.

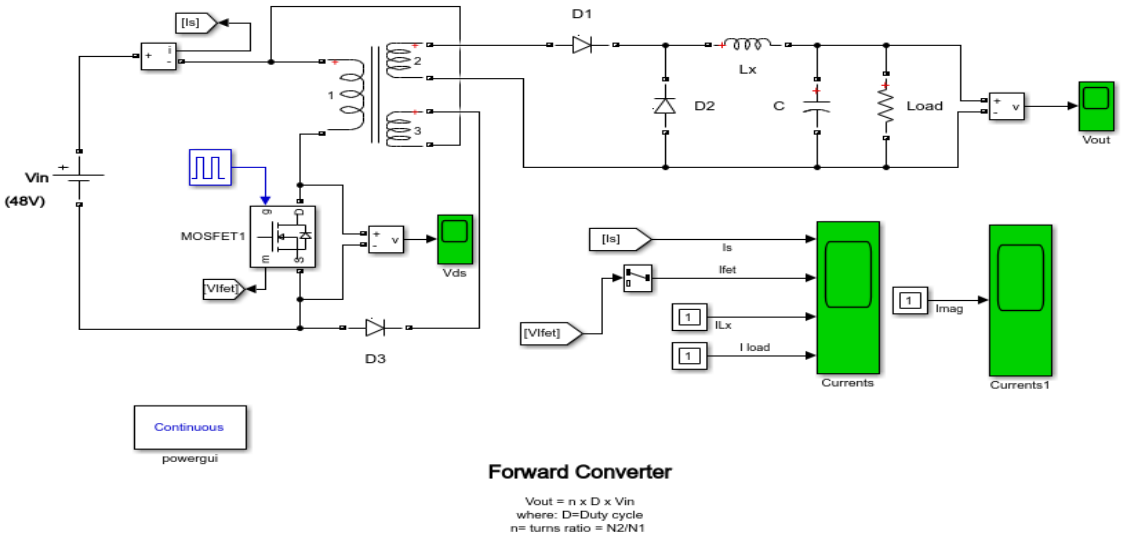


Figure 1. Single Switch Forward Converter

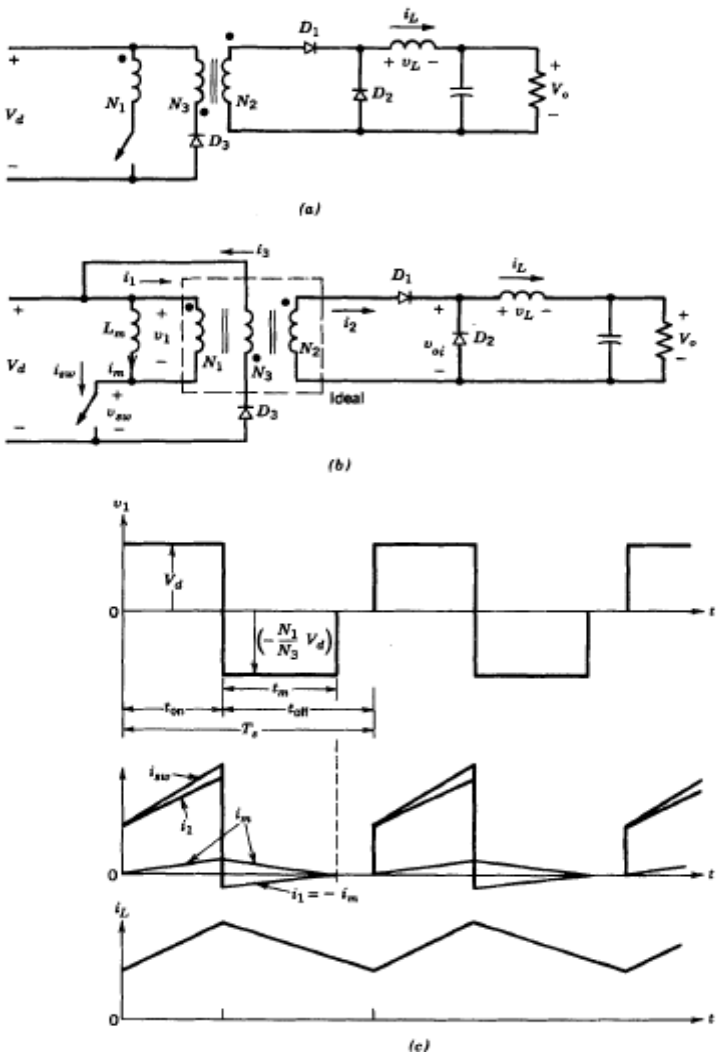


Figure 2. Forward converter and it's corresponding waveforms

When switch is on D1 becomes forward biased D2 becomes reverse biased. Voltage on the inductor, therefore, is

$$Vl = \frac{N2}{N1} Vd - Vo$$

When the switch is off,

$$Vl = -Vo$$

In a one period average inductor voltage is zero, yields

$$\frac{Vo}{Vd} = \frac{N2}{N1} D$$

For the forward converter, magnetizing current of the transformer should be taken into account in order to obtain proper operation. One should prevent the magnetic saturation of the core in the transformer. One way to transfer the stored energy back to the supply voltage is to use practical forward converter topology which can be seen on the figure 2.

When the switch is on:

$$V1 = -Vd$$

When the switch is turned off:

$$i1 = -im$$

$$N1i1 + N3i3 = N2i2$$

$$i2 = 0$$

$$i3 = \frac{N1}{N3} im$$

One needs to completely demagnetize the core which means $im = 0$, minimum required of time is;

$$tm = \frac{N3}{N1} DTs$$

3.2 Simulation Results & Equipment Selection

Simulations are created via using Matlab Simulink. Figure 1 represents forward converter. In the following figure 3, input current above, switch current,output current and inductor current are shown. As seen, output current is constant and inductor current has some ripple. Input current and switch current are same. Figure 4 represents mosfet drain source voltage. This waveform has 3 steps. When the power switch is ON, the switch sees the output filter inductor's current reflected by through the transformer. The amplitude of the primary current is the output rectifier current times turns ratio of the transformer (N1/N2) plus a small

amount of magnetization current. During the power switch OFF time, the switch voltage "flys" up to about twice the input voltage. During this time, the reset winding begins to output magnetization current back to the input capacitor. The output rectification and filter section works identically to the buck converter. The voltage waveform of secondary looks like an inverted primary winding waveform except the zero voltage point is the input voltage point on the primary waveform. The waveform goes positive when the power switch is conducting. The output rectifier also conducts during this time. This presents a unipolar, PWM rectangular voltage signal to the inductor. The catch diode then operates when the power switch and the output rectifier are OFF. Continuous current is then maintained through the output filter inductor.

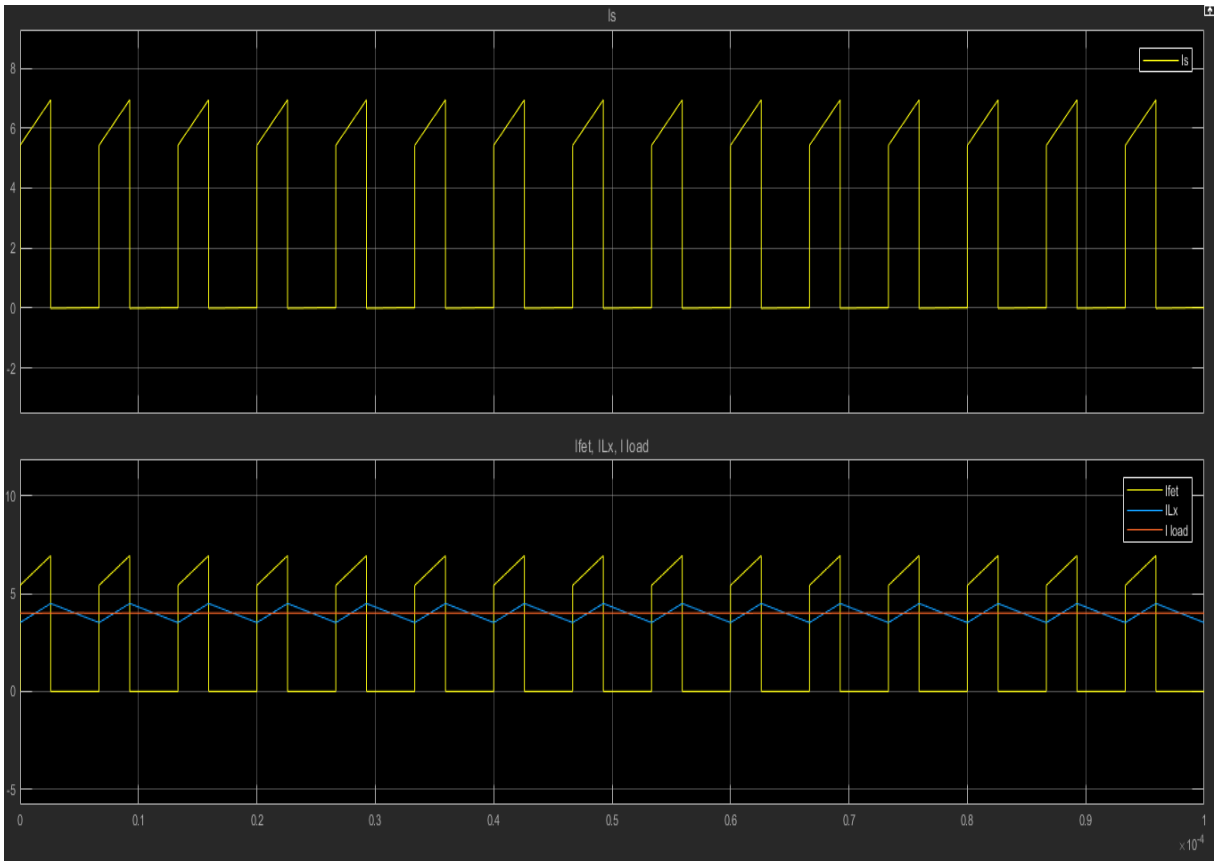


Figure 3. Input,Output, Output inductor and switch currents.

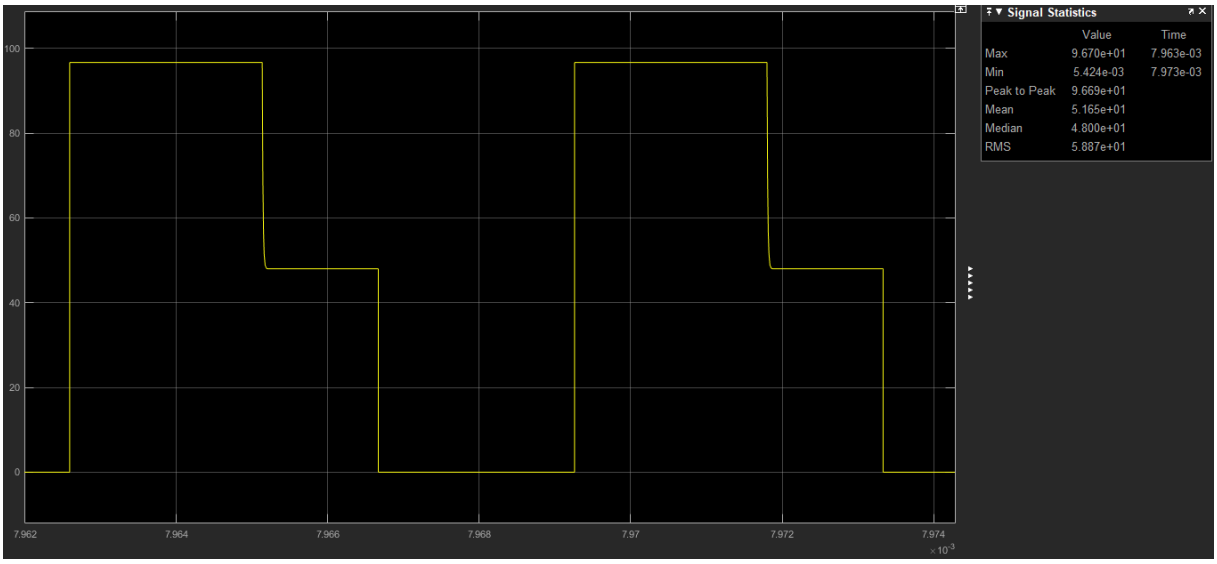


Figure 4. Mosfet drain source voltage.

3.3 Transformer design:

First select a core family that will house the transformer. A ferrite core N87 with ETD39 coil former from TDK company is selected.

The transformer turns ratio N1/N2 is calculated 0.67. The turns ratio selected 0.6.

Primary turns ratio is selected to be 6 secondary turns ratio is 10.

The core is un-gapped and its parameters given in figure 5.

Core **B66363**

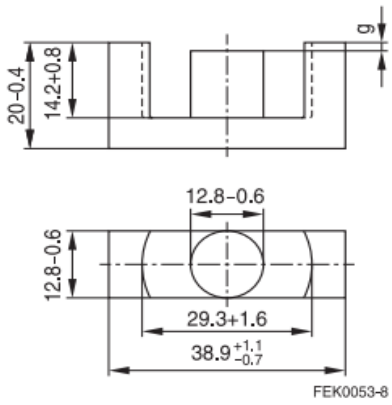
- To IEC 62317-6
- For SMPS transformers with optimum weight/performance ratio at small volume
- Delivery mode: single units

Magnetic characteristics (per set)

$\Sigma l/A$ = 0.74 mm^{-1}
l_e = 92.2 mm
A_e = 125 mm^2
A_{min} = 123 mm^2
V_e = 11500 mm^3

Approx. weight 60 g/set

Ungapped



Material	A_L value nH	μ_e	B_S* mT	P_V W/set	Ordering code
N27	2550 +30/–20%	1500	320	< 2.22 (200 mT, 25 kHz, 100 °C)	B66363G0000X127
N87	2700 +30/–20%	1600	320	< 6.00 (200 mT, 100 kHz, 100 °C)	B66363G0000X187
N97	2800 +30/–20%	1650	320	< 5.10 (200 mT, 100 kHz, 100 °C)	B66363G0000X197

* H = 250 A/m; f = 10 kHz; T = 100 °C

Figure 5. EDT39 N87 core parameters [1]

Primary magnetizing inductance :

$$Lm = 2700 * 62 = 97.2\,uH.$$

Minimum primary turns ratio in order to guarantee saturation:

n1 $> \frac{Vinmax*Dmax*T}{Bsat*Ae}$, $n1 = 3.77$ (our selection is 6)

For $Vimax = 53V$

$Dmax = 0.4$

$Fs = 150\,kHz$

$Bsat = 0.3\,T$ (max allowed core flux density for ferrites to guarantee non-saturation)

$Ae = 125\,mm2$

The turn ratio is wounded with litz wire which has small resistance compared with copper.

The wire is compound of 270x0.05 wire. It has 32.9 ohm/km resistance.

The mean length of one turn for our coil former is 69mm.

At primary:

$N1 = 6\,turn$

$Wire\ length = 6 * 69\,mm = 414\,mm = 41.4\,cm$

$Wire\ resistance = 0.414 * 32.9 * 10^{-3} = 13.6 * 10^{-3}\ ohm$

At secondary:

$N2 = 10\,turn$

$Wire\ length = 10 * 69\,mm = 690\,mm = 69\,cm$

$Wire\ resistance = 0.69 * 32.9 * 10^{-3} = 22 * 10^{-3}\ ohm$

At primary:

$N3 = 6\,turn$

$Wire\ length = 6 * 69\,mm = 414\,mm = 41.4\,cm$

$Wire\ resistance = 0.414 * 32.9 * 10^{-3} = 13.6 * 10^{-3}\ ohm.$

L_{lk} is assumed %5 of Lmag .

L_{lk} = 0.05*97.2 = 4.86 uH

$L_{lk1} = L_{lk\,/\,3}$ = 1.62 uH

$L_{lk2} = L_{lk\,/\,3}$ = 1.62 uH

$L_{lk3} = L_{lk/3} = 1.62$ uH

Minimum load current to ensure CCM operation:

At boundary Io = $\frac{\Delta ILo}{2}$

output inductor current rises during on period. The min outpur inductor current ripple hence output current is occured at min ton.

$\Delta ILo = \frac{VL}{Lo} * ton$

$VL = \frac{N2}{N1} Vinmax - Vo - Vdiode$

where ton(min) = $\frac{Vo - Vdiode}{Vin\ max} * \frac{N1}{N2} * \frac{1}{fs}$ = 2,25 us.

where $\frac{N1}{N2} = 0.65$

fs = 150kHz

Vinmax = 52.8 V

Vdiode = 0.7V

Vo = 28V

substuting ton value in above equation :

$\Delta ILo = [\ \frac{N2}{N1} Vinmax - Vo - Vdiode\ ] * \frac{tonmin}{Lo}$

ΔILo = 0.98 A

where Lo = 120uH

Io = $\frac{\Delta ILo}{2} = \frac{0.98}{2}$ = 0.49 A which is minimum load current with 120uH output inductor to ensure CCM mode of operation.

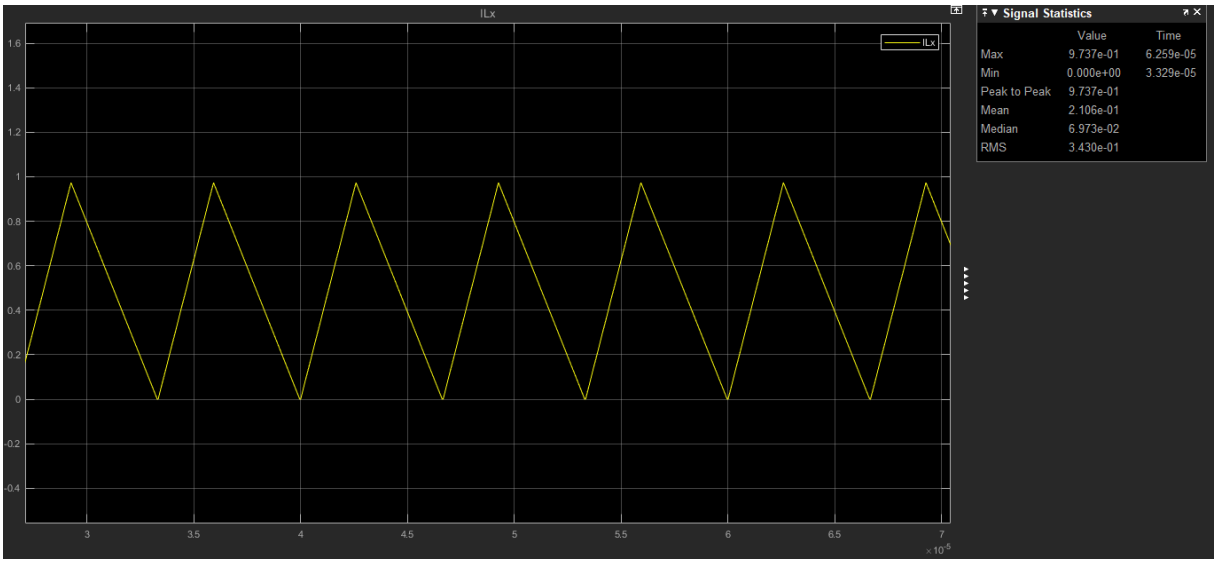
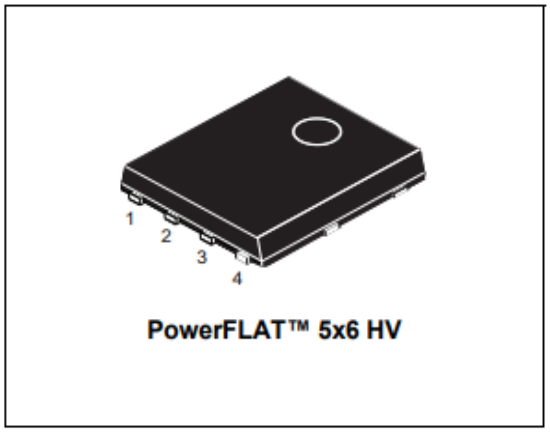


Figure 6**.** Output inductor current at boundary

Main switch: As a main switch STL18N65M5 is selected. It has low on resistance. It is features are given below:



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D
STL18N65M5	710 V	0.240 Ω	15 A(1)

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package.

- Outstanding $R_{DS(on)}$*area
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitance
- 100% avalanche tested

Figure 7. Main switch properties

Finally, as an output inductor, 47uH inductor with 8.6A saturation current from Vishay company.

STANDARD ELECTRICAL SPECIFICATIONS					
L_0 INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) (1)	SATURATION CURRENT DC TYP. (A) (2)	SRF TYP. (MHz)
0.33	0.67	0.73	75.5	55	78
0.47	0.78	0.87	72	57	60
0.56	0.83	0.91	61	66	40
0.82	0.98	1.08	56.5	45	36
1.0	1.21	1.27	55.5	32	34
1.5	1.54	1.62	48	31	26
2.2	1.85	1.98	43.5	28	19
3.3	2.79	2.93	35	27	16
4.7	3.98	4.18	30	21	10.7
5.6	4.23	4.44	28	21	11.8
6.8	5.86	6.15	22.5	18.5	10.0
8.2	7.71	8.10	21	18	10.0
10.0	8.89	9.33	19	17	8.0
15.0	13.7	14.4	14	12	7.5
22.0	20.0	21.0	12	9.5	4.3
33.0	35.1	37.0	10.7	9	4.8
47.0	40.7	42.7	8.7	8.6	4.1
56.0	55	57.8	7.2	4.2	2.9
68.0	72.1	75.7	6.1	4.5	3.0
82.0	87.3	91.7	5.5	4.5	2.6
100.0	105	110	5.0	4.0	2.1

Figure 8. Output inductor characteristic

3.4 Efficiency Calculation:

At %100 Load :

At %100 load load current is 4A.

Diode1 loss :

$V_f = 0.7$ V

$I_{diode} = 2.54$A

$P_{loss} = 0.7*2.54 = 1.778$ W

Diode2 loss :

$V_f = 0.7$ V

$I_{diode} = 3.10$A

$P_{loss} = 0.7*3.10 = 2.17$ W

Inductor loss :

$I_{rms} = 4$A

$R_{ind} = 42$ mohm

$P_{loss} = 4* 0.042 = 0.0168$ W

Main mosfet loss :

$I_{rms} = 4.52$ A

$R_{on} = 0.24$ ohm

$P_{loss} = 4.52*0.24 = 1.0848$ W

Transformer loss:

$P_{loss} = 22m * 4.52 + 16m * 2.54 + 16m * 0.3 = 0.145$ W

Total P_{loss} = 5.05 W

Efficiency = $\frac{Pout}{Ploss+Pout} = \frac{112}{112+5.05}$ =0.96 = 96%

At %75 Load :

At %75 load load current is 3A.

Diode1 loss :

V_f = 0.7 V

I_{diode} = 1.91 A

P_{loss} = 0.7*1.91 =1.34 W

Diode2 loss :

V_f = 0.7 V

I_{diode} = 2.34 A

P_{loss} = 0.7*2.34= 1.64 W

Inductor loss :

I_{rms} = 3A

R_{ind} = 42 mohm

P_{loss} = 3* 0.042 = 0.126 W

Main mosfet loss :

I_{rms} = 3.48 A

R_{on} = 0.24 ohm

P_{loss} = 3.48*0.24 = 0.835 W

Transformer loss:

P_{loss} = 22m * 1.91 + 16m * 3.48 + 16m * 0.3 = 0.1 W

Total P_{loss} = 4 W

Efficiency = $\frac{Pout}{Ploss+Pout} = \frac{84}{84+4}$ =0.95 = 95%

At %50 Load :

At %50 load load current is 2A.

Diode1 loss :

V_f = 0.7 V

I_{diode} = 1.29 A

P_{loss} = 0.7*1.29 =0.9 W

Diode2 loss :

V_f = 0.7 V

I_{diode} = 1.58 A

P_{loss} = 0.7*1.58= 1.1 W

Inductor loss :

I_{rms} = 2A

R_{ind} = 42 mohm

P_{loss} = 2* 0.042 = 0.084 W

Main mosfet loss :

I_{rms} = 2.45 A

R_{on} = 0.24 ohm

P_{loss} = 2.45*0.24 = 0.59 W

Transformer loss:

P_{loss} = 22m * 1.29 + 16m * 2.45 + 16m * 0.3 = 0.7 W

Total P_{loss} = 3.37 W

Efficiency = $\frac{Pout}{Ploss+Pout} = \frac{56}{56+3.37}$ =0.94 = 94%

<u>At %25 Load :</u>

At %25 load load current is 1A.

Diode1 loss :

V_f = 0.7 V

I_{diode} = 0.65 A

P_{loss} = 0.7*0.65 =0.455 W

Diode2 loss :

V_f = 0.7 V

I_{diode} = 0.79 A

P_{loss} = 0.7*0.79= 0.553 W

Inductor loss :

I_{rms} = 1A

R_{ind} = 42 mohm

P_{loss} = 1* 0.042 = 0.042 W

Main mosfet loss :

I_{rms} = 1.40 A

R_{on} = 0.24 ohm

P_{loss} = 1.40*0.24 = 0.336 W

Transformer loss:

P_{loss} = 22m * 0.65 + 16m * 1.4 + 16m * 0.3 = 0.4 W

Total P_{loss} = 1.79 W

Efficiency = $\frac{Pout}{Ploss+Pout} = \frac{28}{28+1.79}$ =0.94 = 94%

3.5 Controller Design

2.5.1 Theoretical Calculations

Small signal analysis of the forward converter is as follows.

State equations are as follows:

On state	Off state
$\dot{x} = A_1 + B_1u$	$\dot{x} = A_2x + B_2u$
$y= C_1x$	$y= C_2x$

where u is input.

Averaging them:

$\dot{x} = [A_1d + A_2(1-d)]\ x + [B_1d + B_2(1-d)]\ u$

$y=C_1d+C_2(1-d)]\ x$

Introducing small perturbations as follows (assuming perturbations in input is equal to zero):

$x=X+\underline{x}$ $y=Y+\underline{y}$ $d=D+\underline{d}$

in steady state $\dot{x}=0$ and neglecting products of $\underline{x}$ and $\underline{d}$;

$\dot{\underline{x}}=AX+Bu+A\underline{x}+[(A_1-A_2)X+(B_1-B_2)u]\underline{d}$

$A = A_1D + A_2(1-D)$

$B= B_1D + B_2(1-D)$

In steady state

$AX+Bu= 0$

Equation 10-50 becomes

$\dot{\underline{x}}= A\underline{x}+[(A_1-A_2)X+(B_1-B_2)u]\underline{d}$ and

$Y+\underline{y}=CX+C\underline{x}+[(C_1-C_2)X]\underline{d}$

Where

$C=C_1D+C_2(1-D)$

$Y=CX$

$\underline{y}=C\underline{x}+[(C1-C2)X]\underline{d}$

$Y/U=-CA^{-1}B$

Taking lap lace transform of small signal eqn. (10-58)

$\underline{Y}(s)/\underline{d}(s)=C[sI-A]^{-1}[(A_1-A_2)X + (B_1-B_2)U] + (C_1-C_2)X$

Let's apply the formula to the forward converter state variables are defined as inductor current and capacitor voltage.

$A_1=$ [-(R*rc + R*rl + rc*rl)/(L*(R + rc)), -R/(L*(R + rc))]

[R/(C*(R + rc)) , -1/(C*(R + rc))]

$A_1=A_2=A$;

$B_1=$ [1/L]

[0]

$B_2=0$;

$B=B_1*D$

For the sake of simplicity assuming R is much greater than (rc+rl);

$A=A_1=A_2=$ [-(rc + rl)/L, -1/L]

[1/C , -1/(C*R)]

$C=C_1=C_2=$[rc 1];

B remains same.

A^{-1}=1/det(A)* [-1/(C*R) , 1/L]

[-1/C , -(rc + rl)/L]

Small signal transfer function is as follows

$$\frac{U(s)}{d(s)} = \frac{1 + sCrc}{LC(s^2 + s\left(\frac{1}{CR} + \frac{rc + rl}{L}\right) + \frac{1}{LC})}U$$

Gain crossover frequency is 70 000 (rad/s). Corresponding phase margin is relatively low. We need to design lead compensator here.

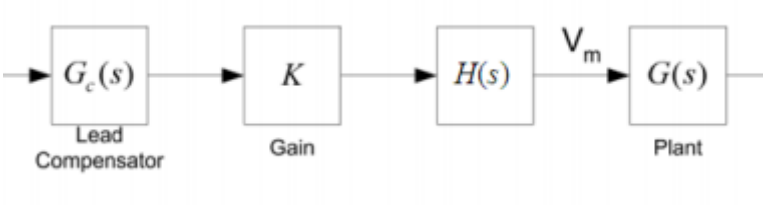


Figure 9. Lead Compensator design

H(s) is standing for elimination of steady state error and will be 1/s. K is gain.G(s) is lead compensator which has unity gain. It has a form of

$$Gc(s) = \frac{a\left(s + \frac{w}{a}\right)}{s + wa}$$

We obtained characteristic of $Gc(s) * \frac{1}{s} * K$ via using type 2 controller circuit. Overall open loop characteristic is

$$\frac{U(s)}{d(s)} * \ Gc(s) * \frac{1}{s} * K$$

2.5.2 Simulation Results

Let's choose;

Vd=48V

Vo=28V

rL=0.085ohm

L=94uH

Cout1 = 100uF

rc1=1.2 Ohm

C=30uF

R=1.66 mOhm

fs=200 kHz

$$\frac{U(s)}{d(s)} = \frac{1 + sCrc}{LC(s^2 + s\left(\frac{1}{CR} + \frac{rc + rl}{L}\right) + \frac{1}{LC})} U$$

Bode diagram is in following figure 10. Gain crossover frequency $wc = 8.88 * 10^3$

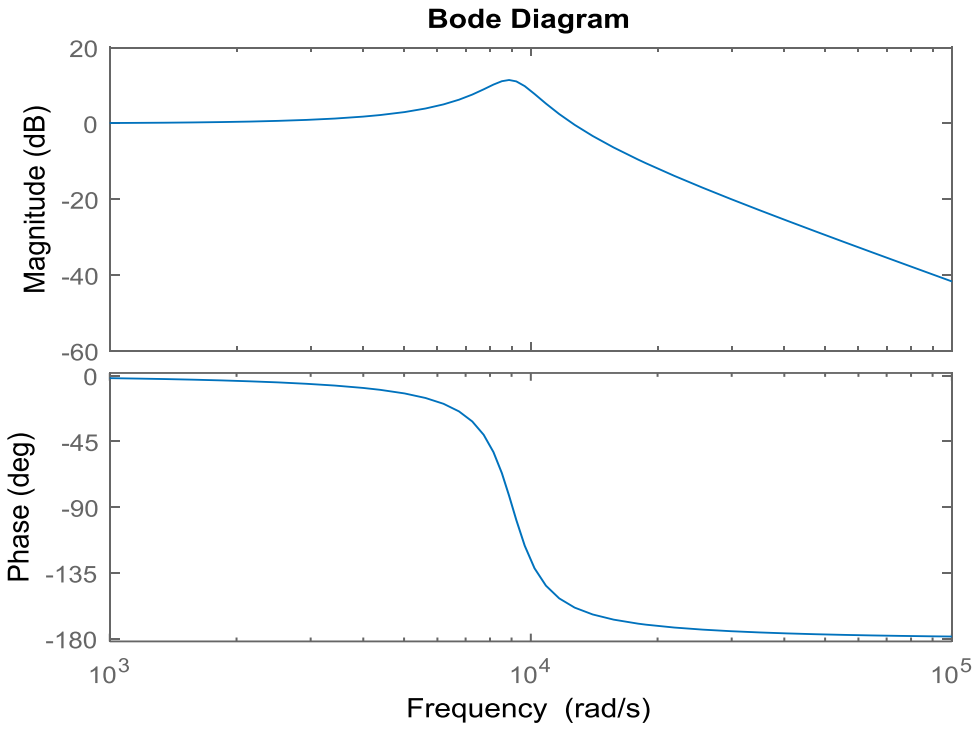


Figure 10. Bode plot characteristic of open loop system.

We designed lead compensator unit here. Let's start with integrator term in order to eliminate steady state error. Bode plot with H(s)=1/s is following figure 11.

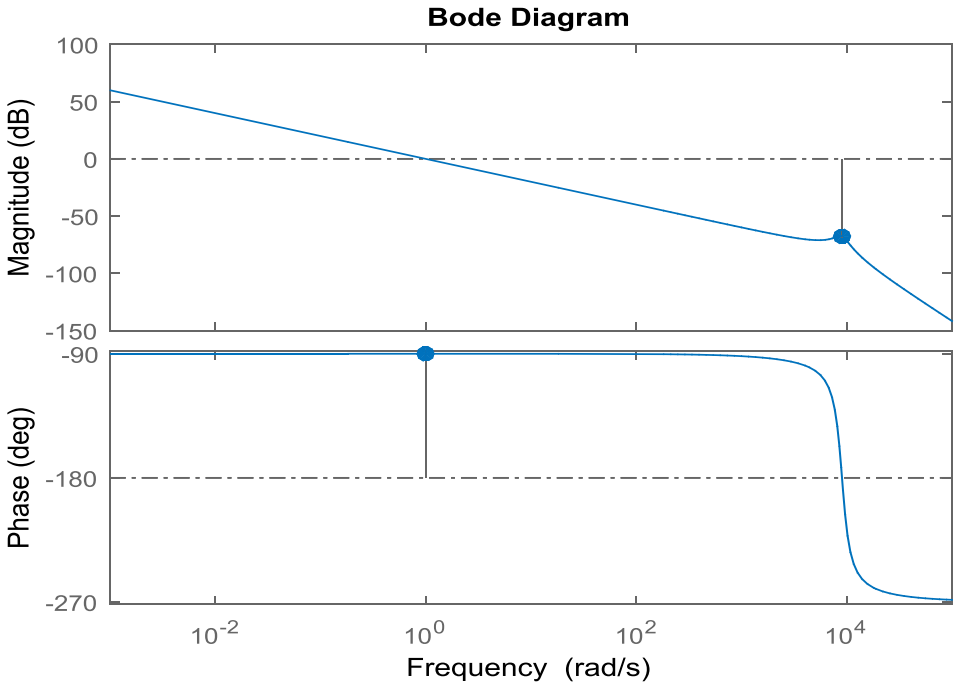


Figure 11. Bode diagram of $\frac{1}{s}G(s)$

Choose K=4000; bode plot of K*H(s)*G(s) is in figure 12.

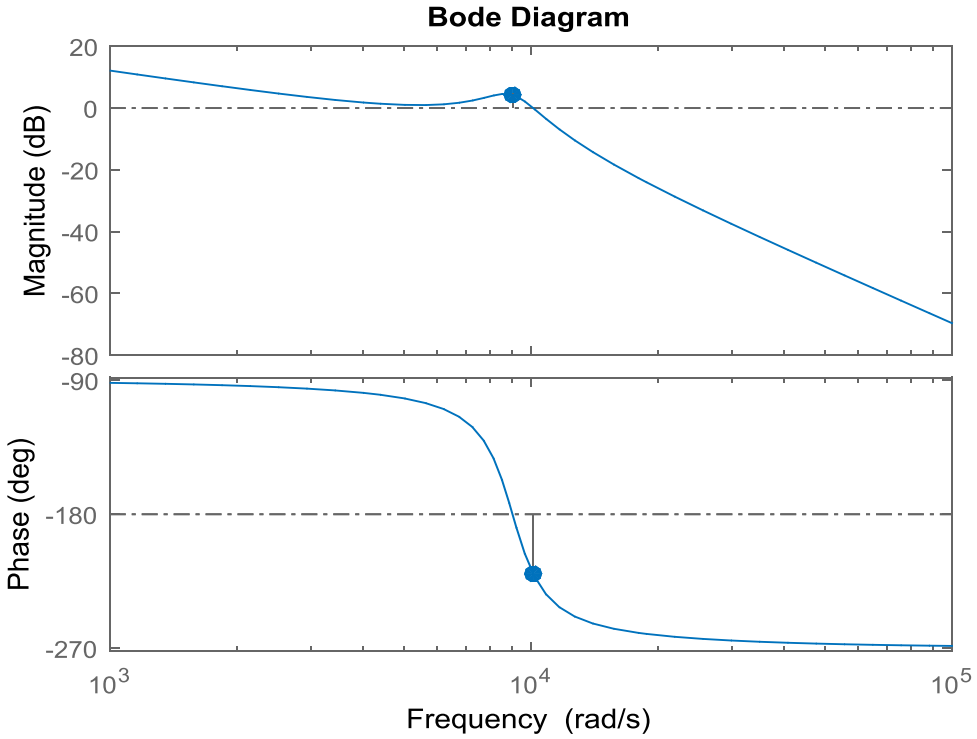


Figure 12. bode plot of K*H(s)*G(s)

Let's design unity gain lead compensator at gain crossover frequency. Bode plot of single compensator is in following figure 13.

$wc = 1 * 10^4$rad/s

a=11;

which means we add 80 degrees phase at gain crossover frequency. Our lead compensator has a form of

$$Gc(s) = \frac{a(s + \frac{w}{a})}{s + wa}$$

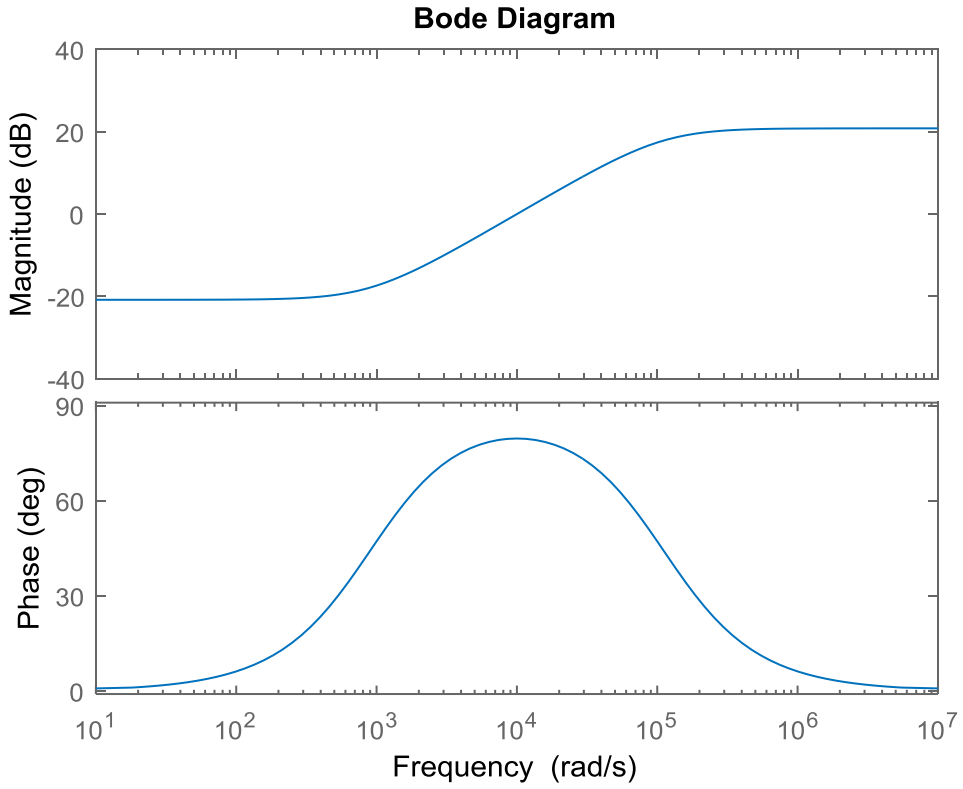


Figure 13. Characteristic of lead compensator

Overall open loop system characteristic is in following figure 14.

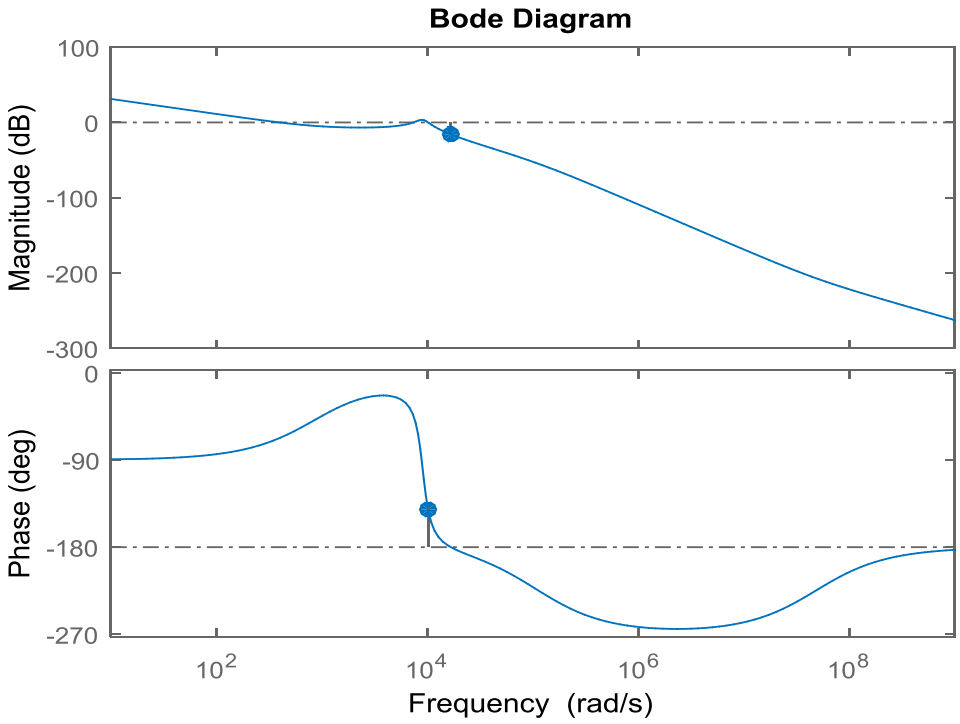


Figure 14. Overall open loop characteristic

Figure 14 shows our closed loop system will be stable. As a result we have 39 degrees of phase margin which is enough for proper operation.

In order to control our DC/DC converter we are decided to use UC1845 Current mode PWM controller it has also current limiter. Block diagram of controller is in following figure 15.

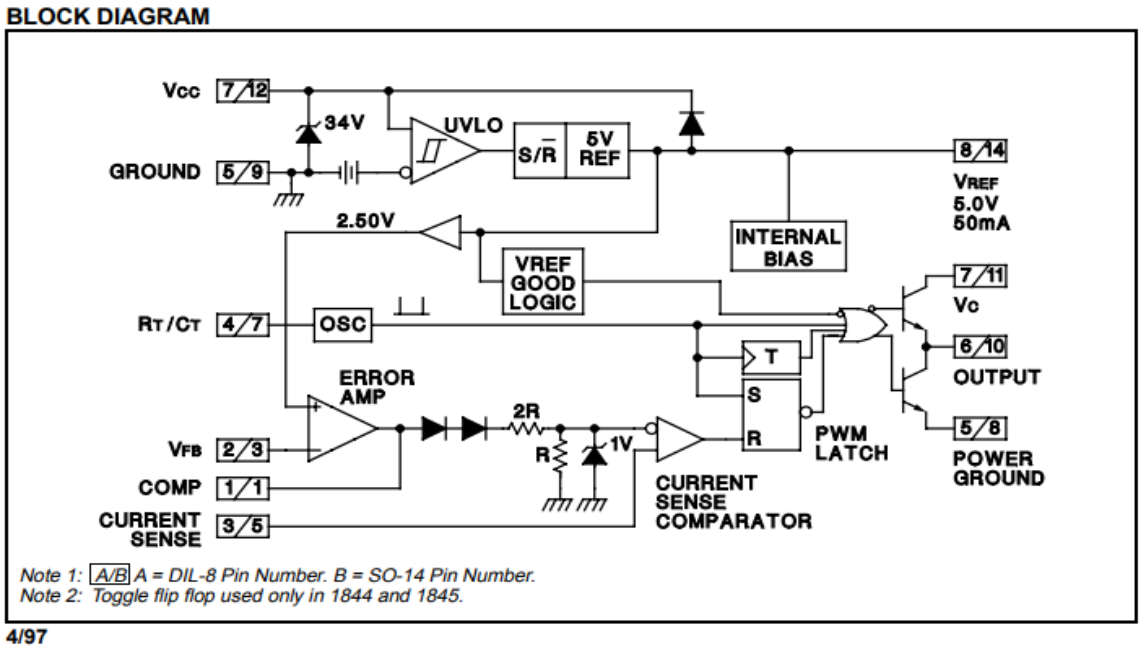


Figure 15. UC1845 Current mode PWM controller [3]

Simulation results of closed loop system are in following figure 16, 17, 18 19.

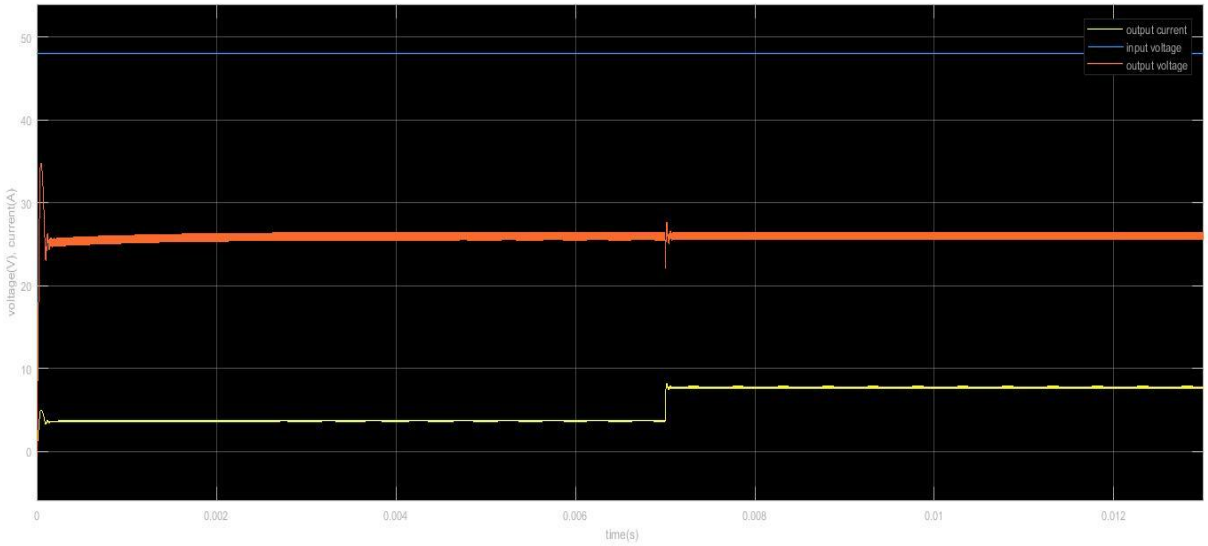


Figure 16. Response of the system when load is decreased two times

Control effort is in following figure 17.

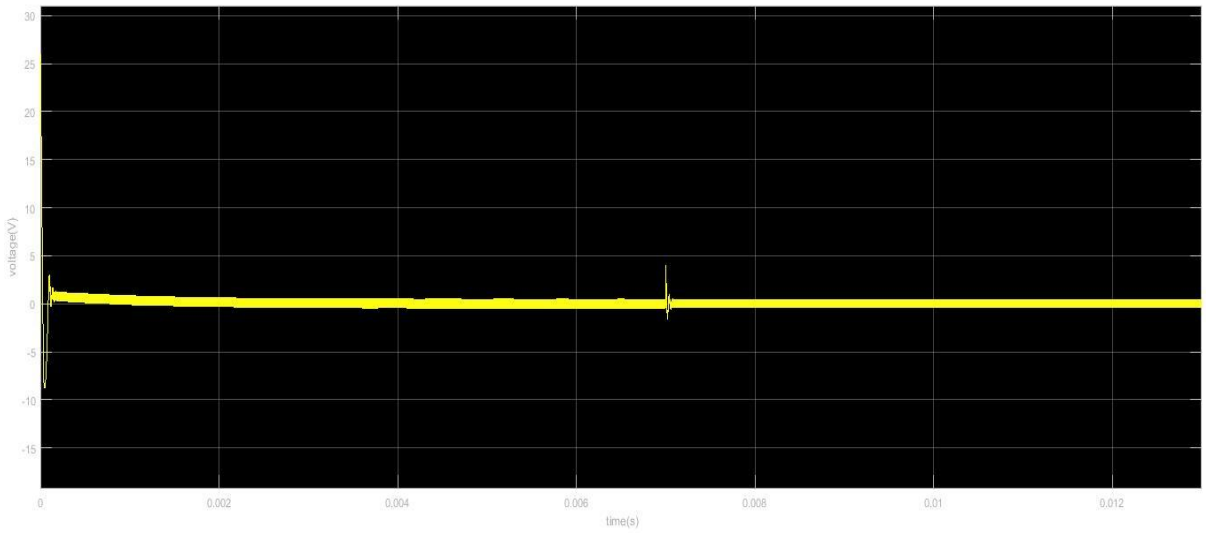


Figure 17. Control effort

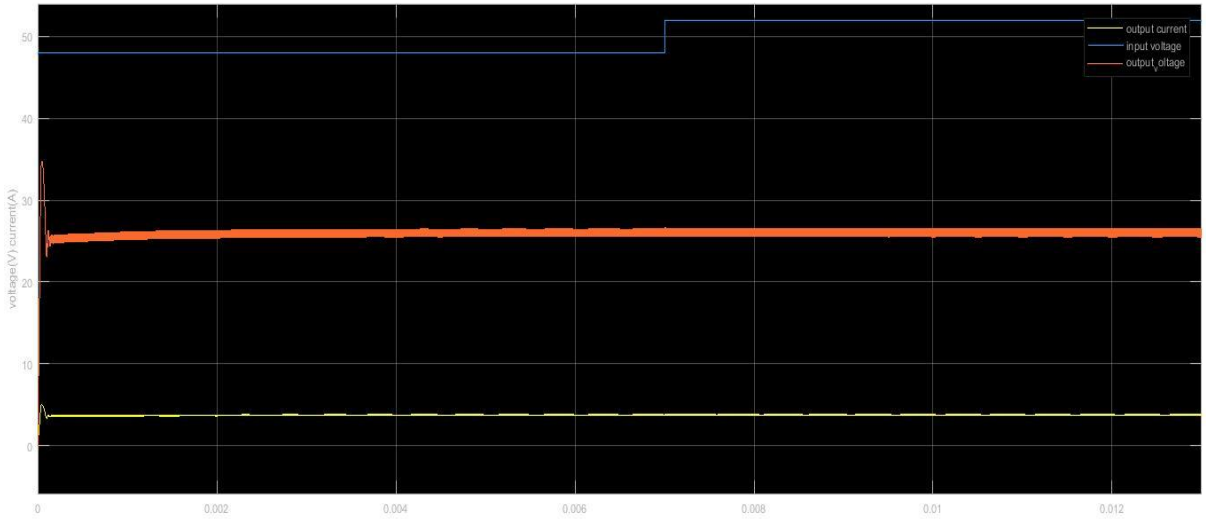


Figure 18. İnput voltage is increased %10

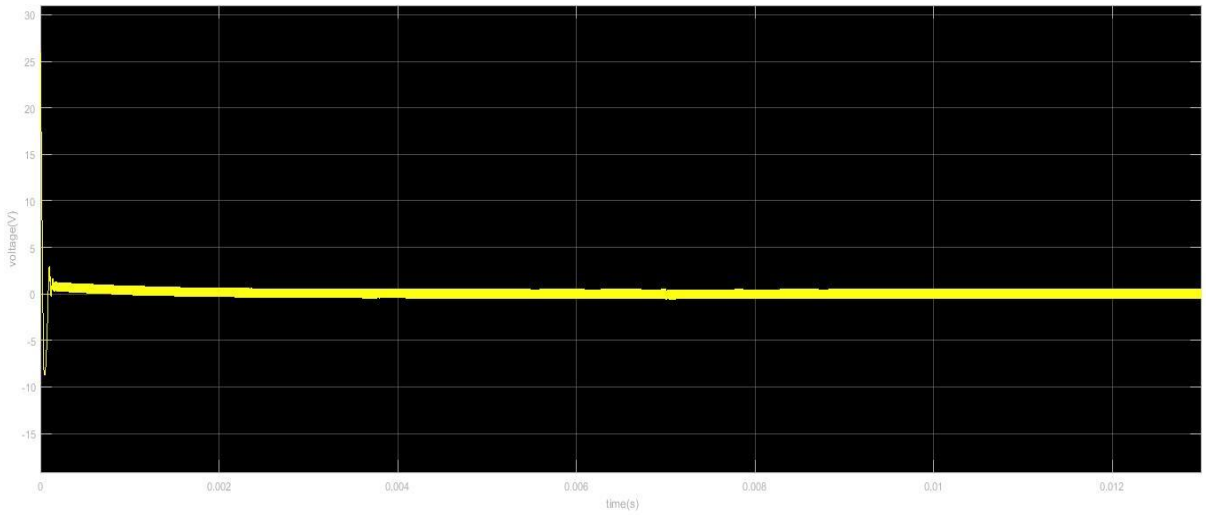


Figure 19. Corresponding control effort

Figure 16,17,18 & 19 show us our controller works efficiently and control effort voltage is in the applicable levels.

4 DEMONSTRATİON

As stated above section 2, uc1845 current mode controller and uc27525 gate driver is used to drive switch. The UC1845 control integrated circuit provides the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. The internally implemented circuits include an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage that is designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state. The converter is implemented on a printed circuit board given below in figure 20.

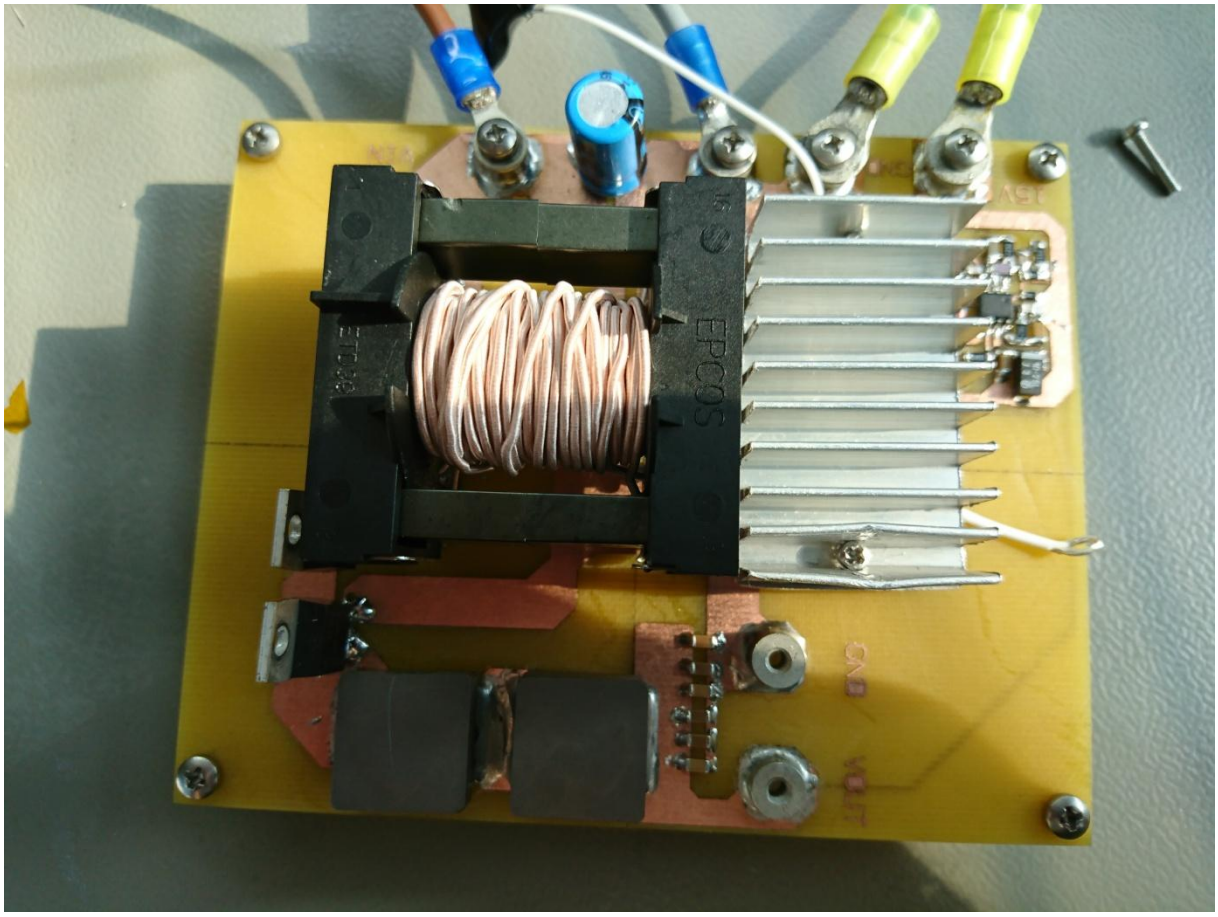


Figure 20. Forward Converter on Printed Circuit Board

The circuit is tested by loaded the output 1A,2A and 3A. The gate signal of switch, output waveform and efficiency is observed. As can be seen in below figures the output voltage and duty ratios are nearly same for increased load current which can be interpreted as the converter is stable.

4.1 No load test:

The test is conducted under no input voltage and no output load. As expected the controller set the duty ratio of switch to maximum to make the output at desired voltage. Because, it has feedback from output to set its the nominal value 28V. As seen below in figure 21, the duty ratio of switch is nearly %50 which is the controller maximum duty cycle.

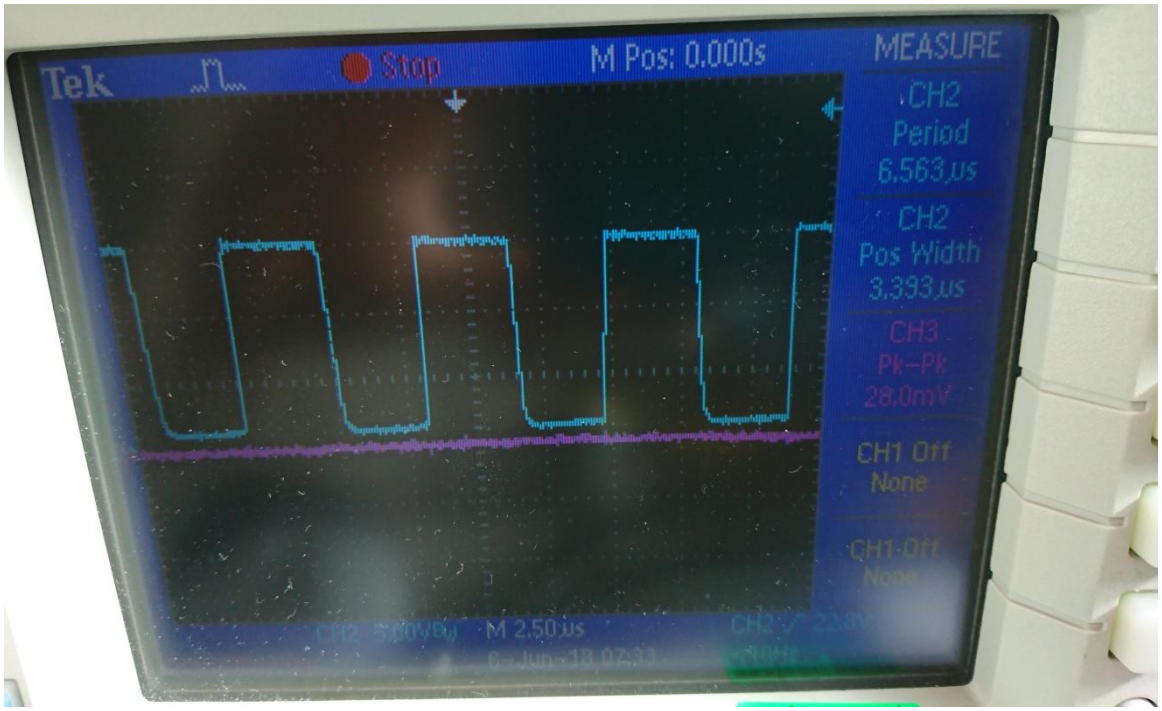


Figure 21. Gate-source voltage waveform of switch whit no-input and no-load

Current sense voltage and pwm signal relation under no-load:

As seen below in figure 22, a sense resistor 100mohm is used to sense the primary current. The primary current is sensed and converted a voltage signal.The PWM uses this signal to terminate the OUTPUT switch conduction. In figure 23, the pwm signal and current sense signal are observed in same graph. Also, to prevent false triggering due to leading edge noises, an RC current sense filter is connect to the Isense pin of controller. The controller switch off when the current sense signal reached to threshold level. This threshold level changes with load. This current sense feature also provides a overcurrent production.

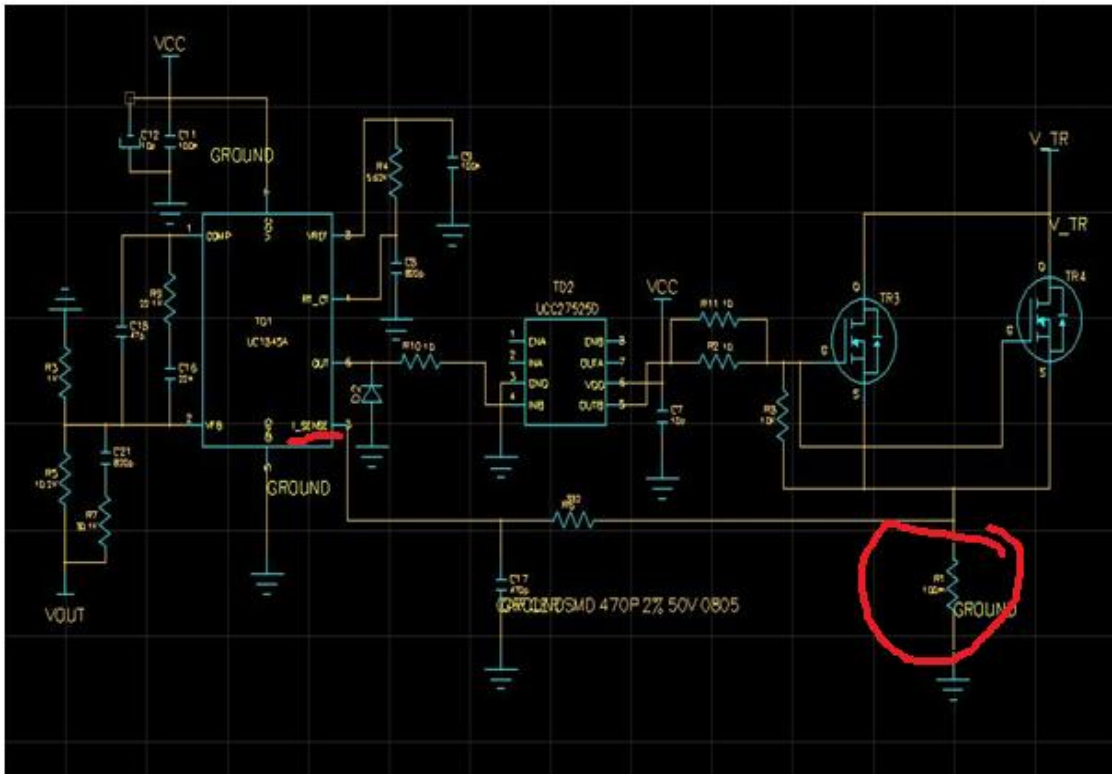


Figure 22. UC1845 with external components and current sense

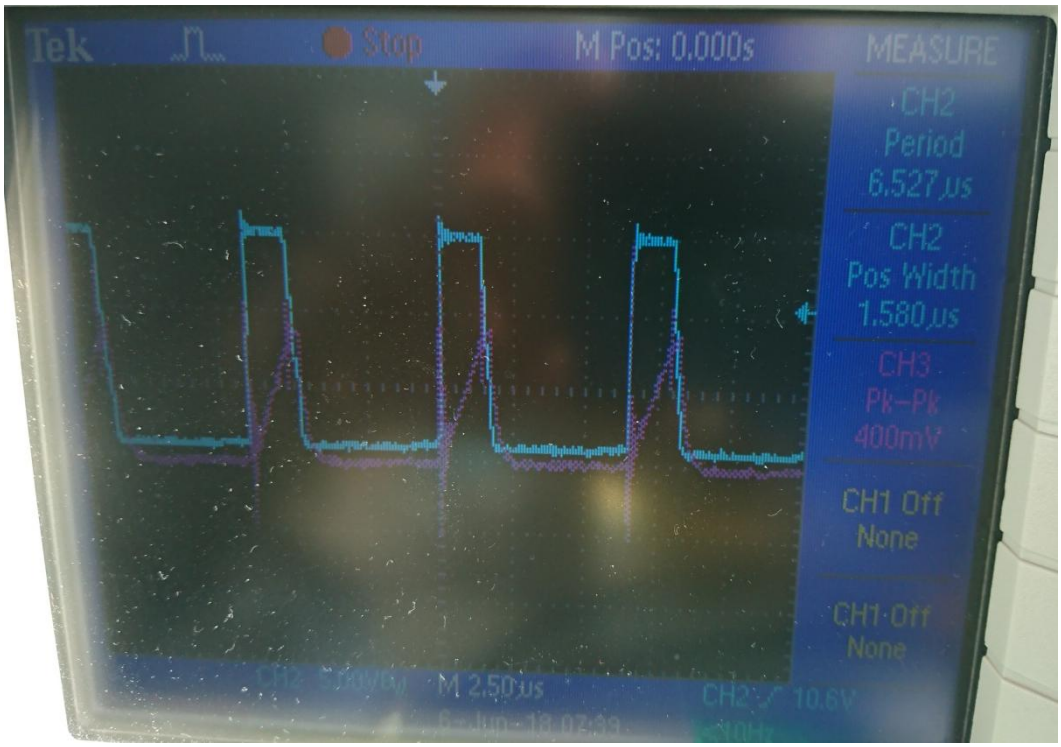


Figure 23. Current sense signal and pwm signal on same screen

4.2 1A Load test:

A load which draw constant 1A current is connected to the output of converter. Pwm signal and output voltage are observed with different input voltage 40V,48V and 52V.

For 40V input voltage, which is minimum input voltage, the duty cycle is maximum and equal to 43%. The output voltage is equal to 28.5V. The controller increase the duty ratio of switch to keep output voltage at its nominal value.

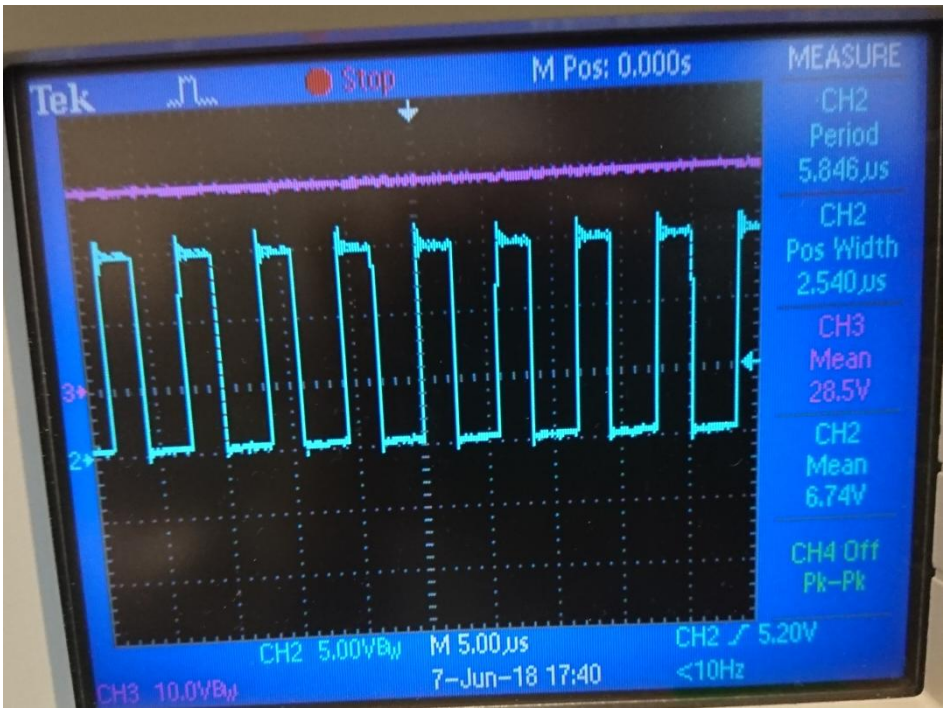


Figure 24. PWM signal and output voltage waveforms with 40V input and 1A load current

For 48V input voltage, which is nominal input voltage, the duty cycle is equal to 35%. The output voltage is still equal to 28.5V. As the input voltage increased, the duty ratio is reduced.

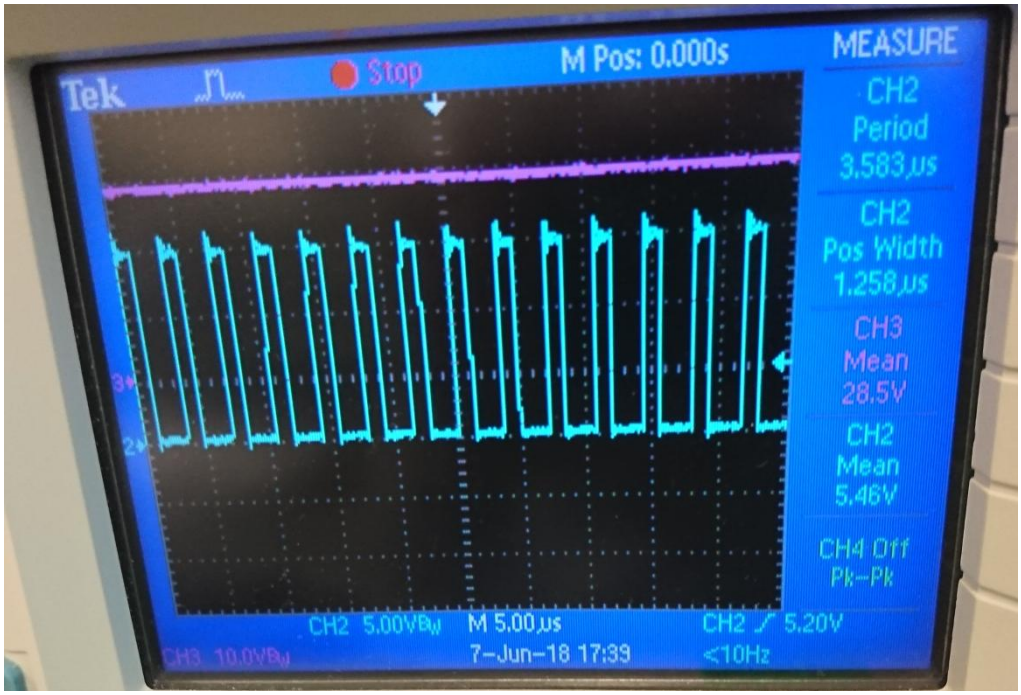


Figure 25. PWM signal and output voltage waveforms with 48V input and 1A load current

For 52V input voltage, which is maximum input voltage, the duty cycle is minimum and equal to 32%. The output voltage is still equal to 28.5V. As the input voltage increased, the duty ratio is reduced.

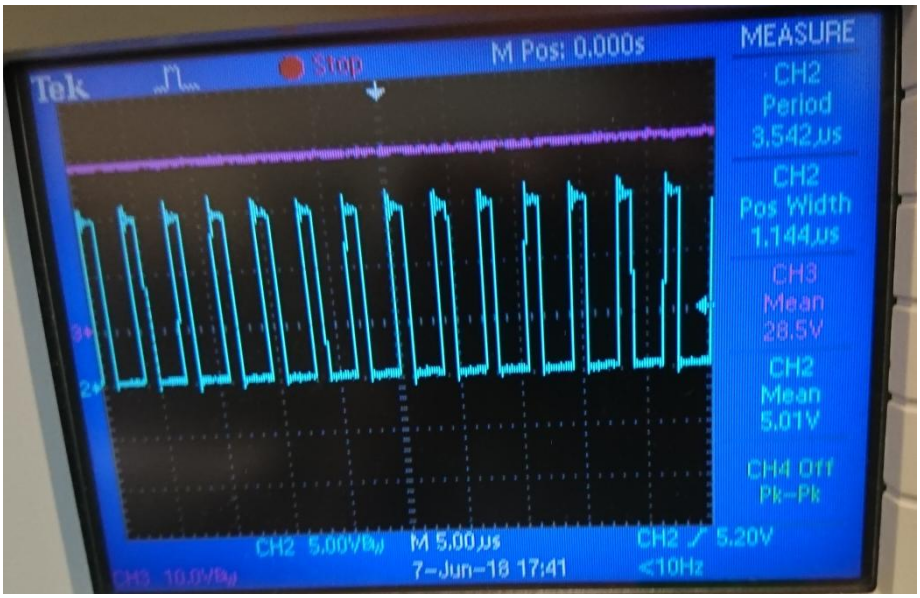


Figure 25. PWM signal and output voltage waveforms with 52V input and 1A load current

4.3 2A Load test:

A load which draw constant 2A current is connected to the output of converter. Pwm signal and output voltage are observed with different input voltage 40V,48V and 52V.

For 40V input voltage, which is minimum input voltage, the duty cycle is maximum and equal to 45%. The output voltage is equal to 28.7V. The controller increase the duty ratio of switch to keep output voltage at its nominal value.

Figure 26. PWM signal and output voltage waveforms with 40V input and 2A load current

For 48V input voltage, which is nominal input voltage, the duty cycle is equal to 36%. The output voltage is equal to 28.5V. As the input voltage increased, the duty ratio is reduced.

Figure 27. PWM signal and output voltage waveforms with 48V input and 2A load current

For 52V input voltage, which is maximum input voltage, the duty cycle is minimum and equal to 33%. The output voltage is equal to 28.4V. As the input voltage increased, the duty ratio is reduced.

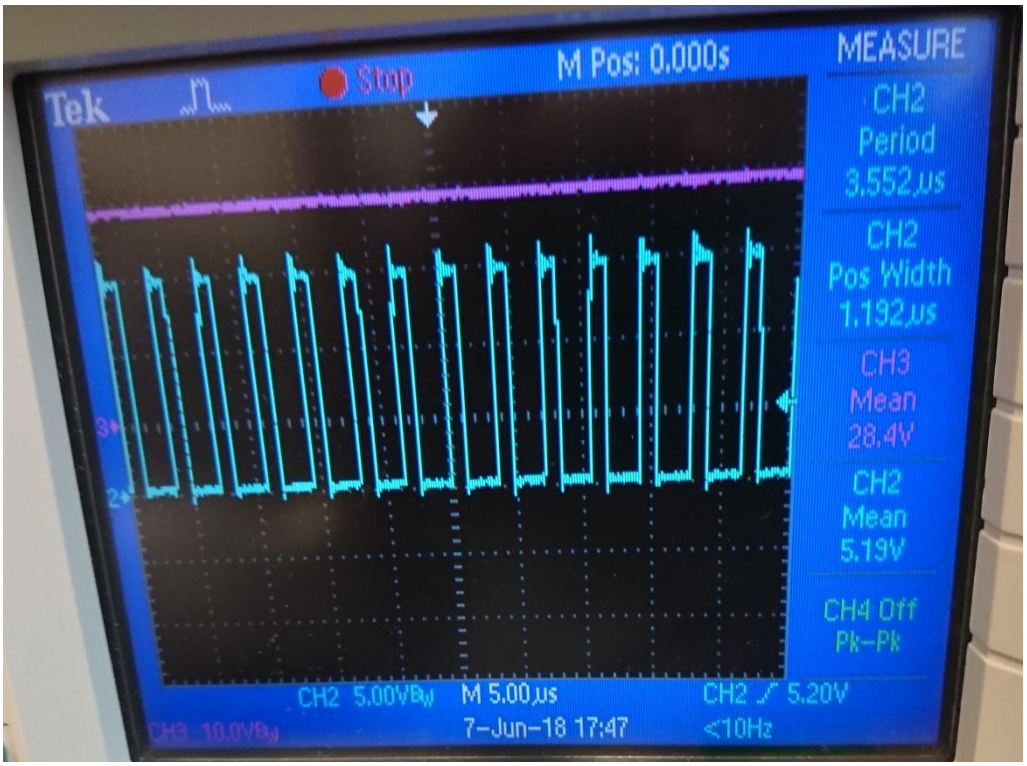


Figure 28. PWM signal and output voltage waveforms with 52V input and 2A load current

4.4 3A Load test:

A load which draw constant 3A current is connected to the output of converter. Pwm signal and output voltage are observed with different input voltage 40V,48V and 52V.

For 40V input voltage, which is minimum input voltage, the duty cycle is maximum and equal to 44%. The output voltage is equal to 28.6V. The controller increase the duty ratio of switch to keep output voltage at its nominal value.

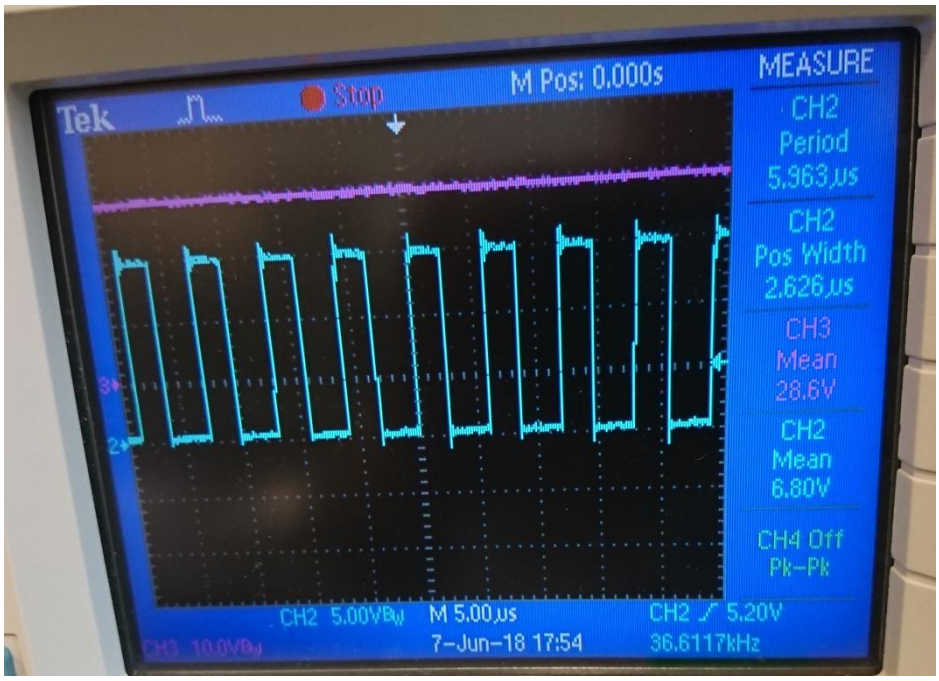


Figure 29. PWM signal and output voltage waveforms with 40V input and 3A load current

For 48V input voltage, which is nominal input voltage, the duty cycle is equal to 37%. The output voltage is still equal to 28.6V. As the input voltage increased, the duty ratio is reduced.

Figure 30. PWM signal and output voltage waveforms with 48V input and 3A load current

For 52V input voltage, which is maximum input voltage, the duty cycle is minimum and equal to 35%. The output voltage is equal to 28.5V. As the input voltage increased, the duty ratio is reduced.

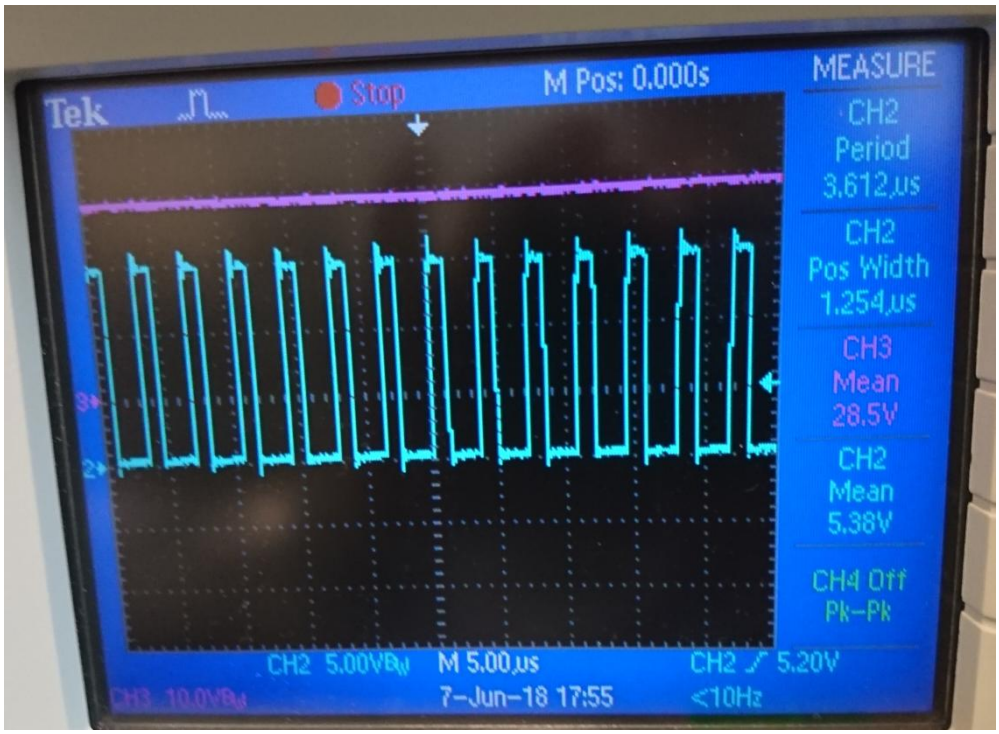


Figure 31. PWM signal and output voltage waveforms with 52V input and 3A load current

4.5 Efficiency test:

The efficiency of converter is tested under various load current 1A,2A and 3A with nominal input voltage 48V and given below in table. The converter has a efficiency which admitted very high for forward converter.

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Ploss (W)	Efficiency (%)
48	0,66	28	1	31,68	28,00	3,68	88,00
48	1,30	28	2	62,40	56,00	6,40	90,00
48	1,96	28	3	94,08	84,00	10,08	89,00

5 CONCLUSION

This project was a good opportunity to apply our knowledge which we gain from the course to real problem. We designed a Forward Converter with a analog controller. We observed that in real life applications, it is not enough to have well theoretical backgrounds, there is always a possibility to encounter unexpected problems during design process. We overcome these problems by making some research on the internet (by asking people who worked on similar projects) and making some library researches. For example, the switching frequency and pwm waveform was not regular since the output voltage oscillated. If output voltage oscillates, the error amplifier output and hence pwm signal oscillate with same frequency. We solved this problem by adding more capacitor to the output to make way with this oscillation. In addition to Forward converter we designed a controller circuit to stabilize the output voltage level in case of any fluctuations.

To conclude, this project was a good opportunity to check our knowledge before encountering the engineering life and we hope that solution methods and design process in this project will find an echo in the field of power electronics area.

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