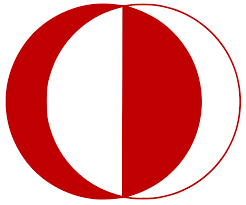
****

**MIDDLE EAST TECHNICAL UNIVERSITY**

**ELECTRICAL AND ELECTRONICS DEPARTMENT**

**EE464**

**Static Power Conversion - II**

**Simulation Project 2 Report**

**Isolated Converters & Controller Design**

**Prepared by:**

**Raşit GÖKMEN - 2339760**

**Asım Reha Çetin - 1877257**

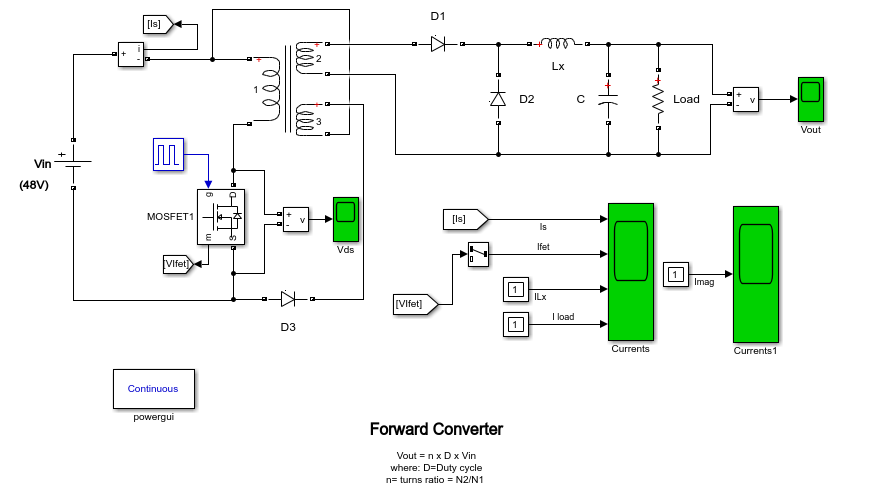
**Alma Piric**

**19/04/2018**

**FORWARD CONVERTER DESIGN**

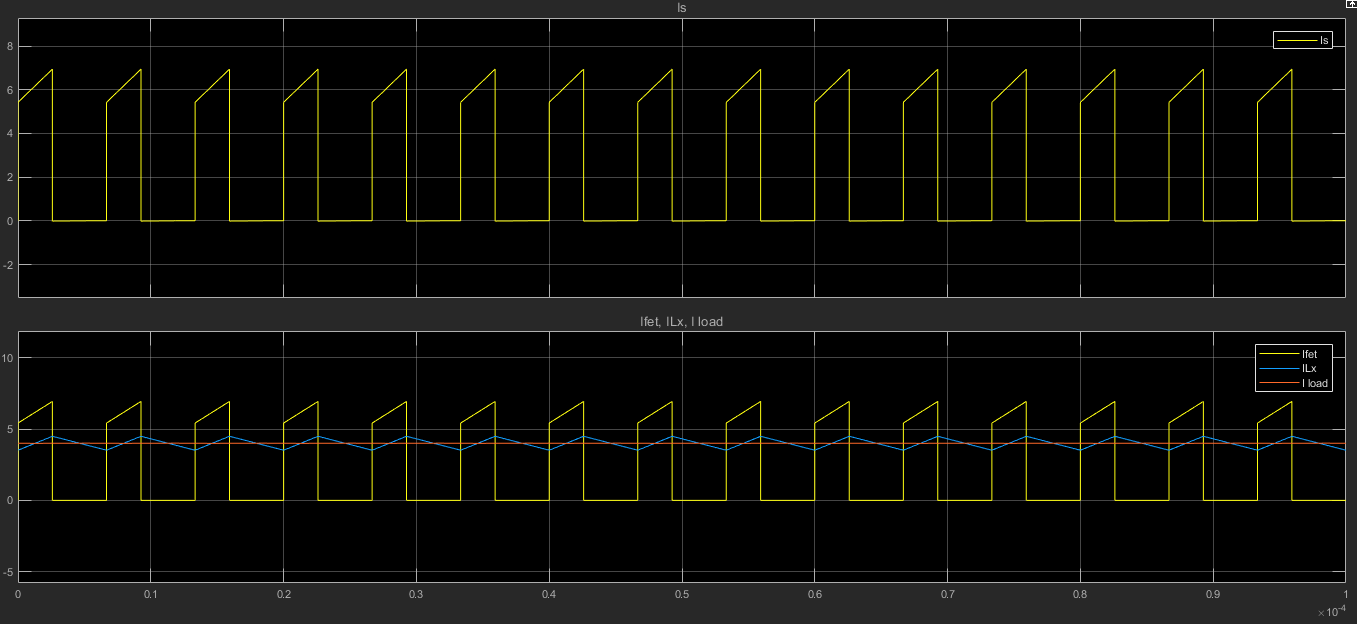
**Simulation:**

A 48V/28V 112W forward converter given below is simulated using simulink.

****

**Figure 1:** Forward Converter Schematic

The input, output, switch, magnetizing and output inductor currents are observed. Also output voltage and mosfet drain-source voltage are observed.



**Figure 2** : Input,Output, Output inductor and switch currents.

Above yellow : Input current

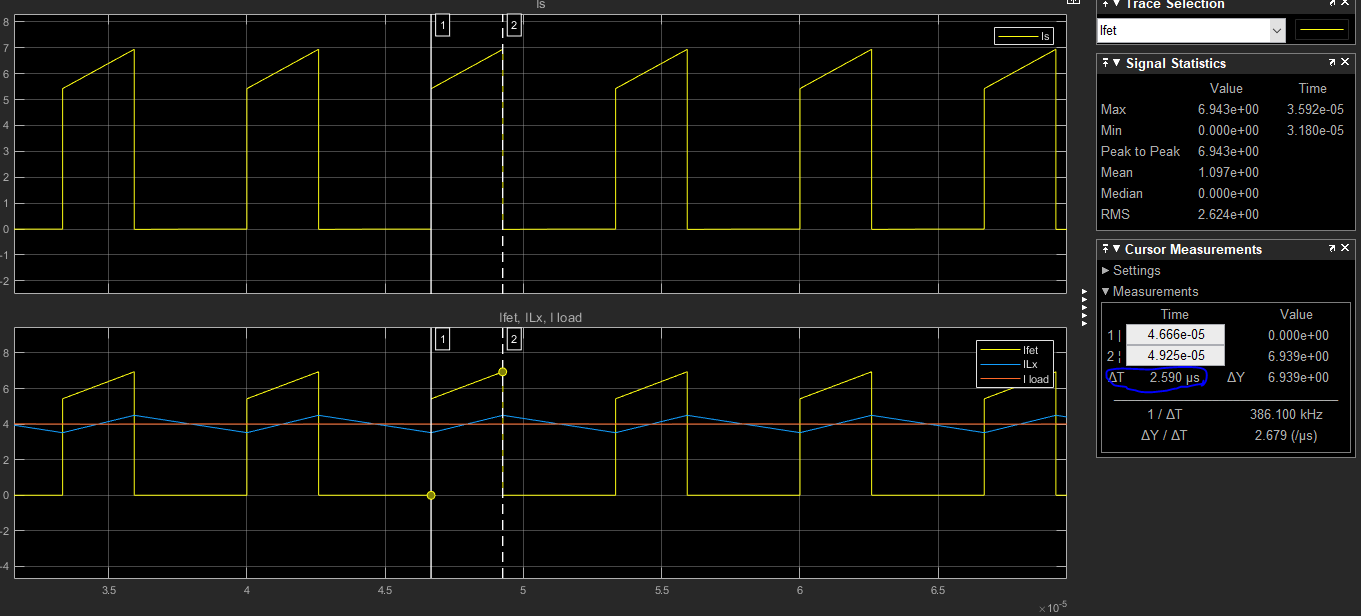
Below yellow : Output current

Orange : Load(112W) current

Blue : Output inductor current

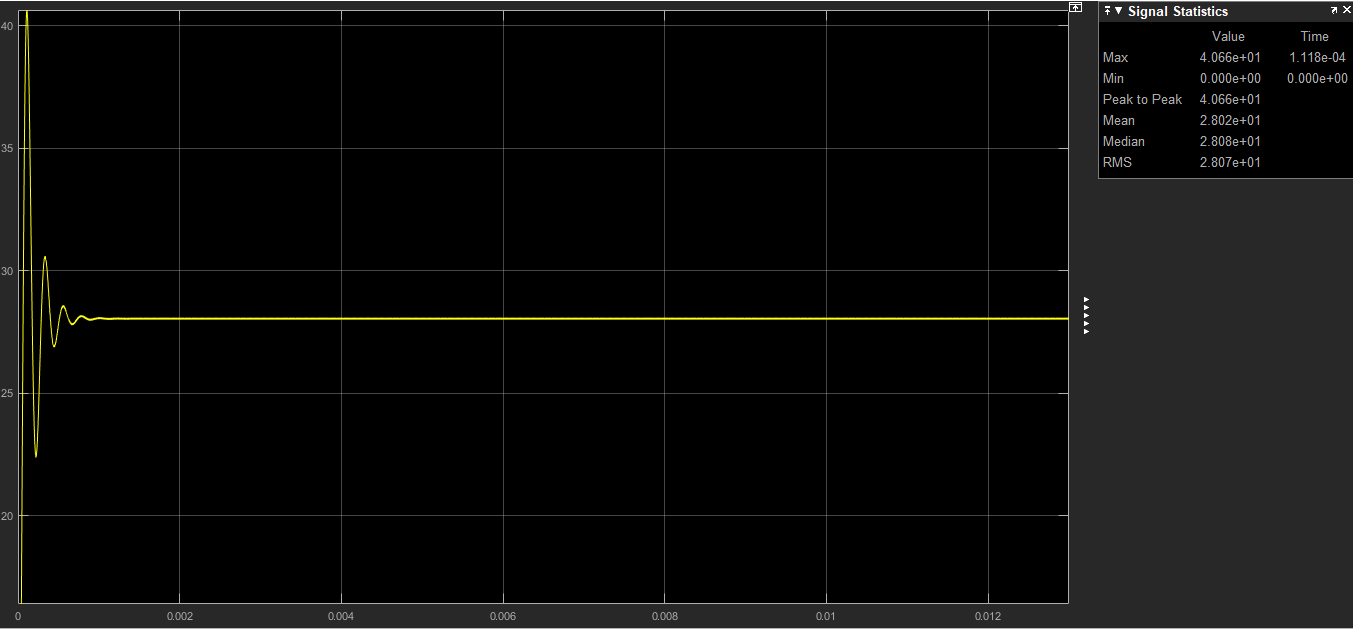
As seen below, the on time of switch is measured. The difference between time cursors found 2.59us. A period of switch pwm is 6.67 us. Thus, the switch duty cycle is calculated:

D = \* 100% = 38.8%



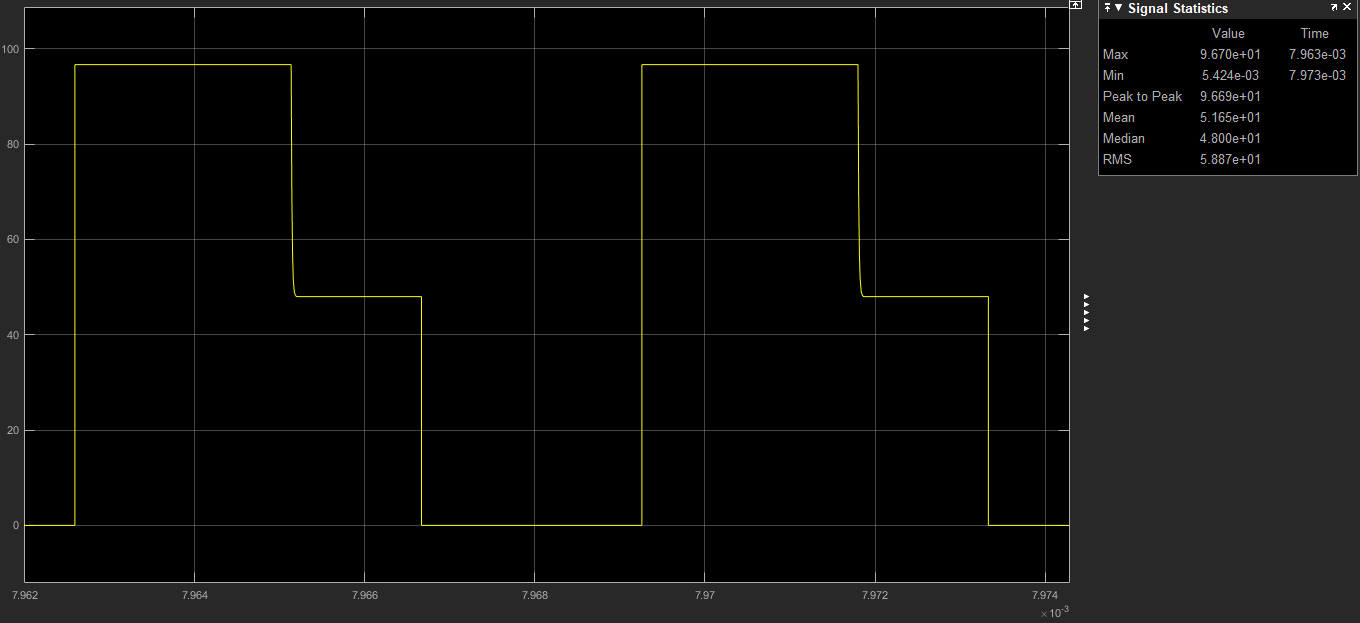
**Figure 3:** Switch duty cycle measurement

The output voltage is given below. As seen, at transient there is overshoot with 40.6V. In steady state it is settled to 28V.



**Figure 4:** Output voltage waveform

The mosfet drain-source voltage is given below.



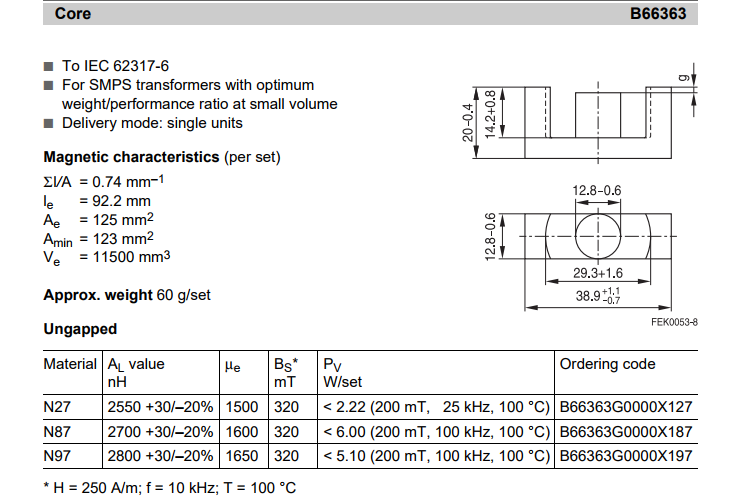
**Figure 5:** Mosfet D-S Voltage

**Transformer design:**

The transformer turns ratio N1/N2 is calculated 0.67. The turns ratio selected 0.6.

A ferrite core N87 with ETD39 coil former from TDK company is selected.

The core is ungapped and its parameters given below:



**Figure 6:** EDT39 N87 core parameters

As seen from figure 6, the AL value of core is 2700nH/n2 . As mentioned the turns ratio is 0.6 . The primary and tertiary winding turns ratio are choosen 6 and secondary winding turn ratio is choosen 10.

Primary magnetizing inductance :

Lm = 2700\*62 = 97.2 uH.

With ETD39 core size, minimum primary turns-count in order to guarantee non saturation:

n1 > , n1 = 3.77

which satifies our assumption n1 = 6.

For Vimax = 53V

Dmax = 0.4

Fs = 150 kHz

Bsat = 0.3 T (max allowed core flux density for ferrites to guarantee non-saturation)

Ae = 125 mm2

The turn ratio is wounded with litz wire which has small resistance compared with copper.

The wire is compound of 270x0.05 wire. It has 32.9 ohm/km resistance.

The mean length of one turn for our coil former is 69mm.

At primary :

N1 = 6 turn

Wire length = 6\*69 mm = 414 mm = 41.4 cm

Wire resistance = 0.414 \* 32.9 \*10-3 = 13.6\*10-3 ohm

At secondary :

N2 = 10 turn

Wire length = 10\*69 mm = 690 mm = 69 cm

Wire resistance = 0.69 \* 32.9 \*10-3 = 22\*10-3 ohm

At primary :

N3 = 6 turn

Wire length = 6\*69 mm = 414 mm = 41.4 cm

Wire resistance = 0.414 \* 32.9 \*10-3 = 13.6\*10-3 ohm

Llk is assumed %5 of Lmag .

Llk = 0.05\*97.2 = 4.86 uH

Llk1 = Llk / 3 = 1.62 uH

Llk2 = Llk / 3 = 1.62 uH

Llk3 = Llk / 3 = 1.62 uH

Minimum load current to ensure CCM operation:

At boundary Io =

output inductor current rises during on period. The min outpur inductor current ripple hence output current is occured at min ton.

= \*ton

VL = Vinmax - Vo - Vdiode

where ton(min) = \*\* = 2,25 us.

where

fs = 150kHz

Vinmax = 52.8 V

Vdiode = 0.7V

Vo = 28V

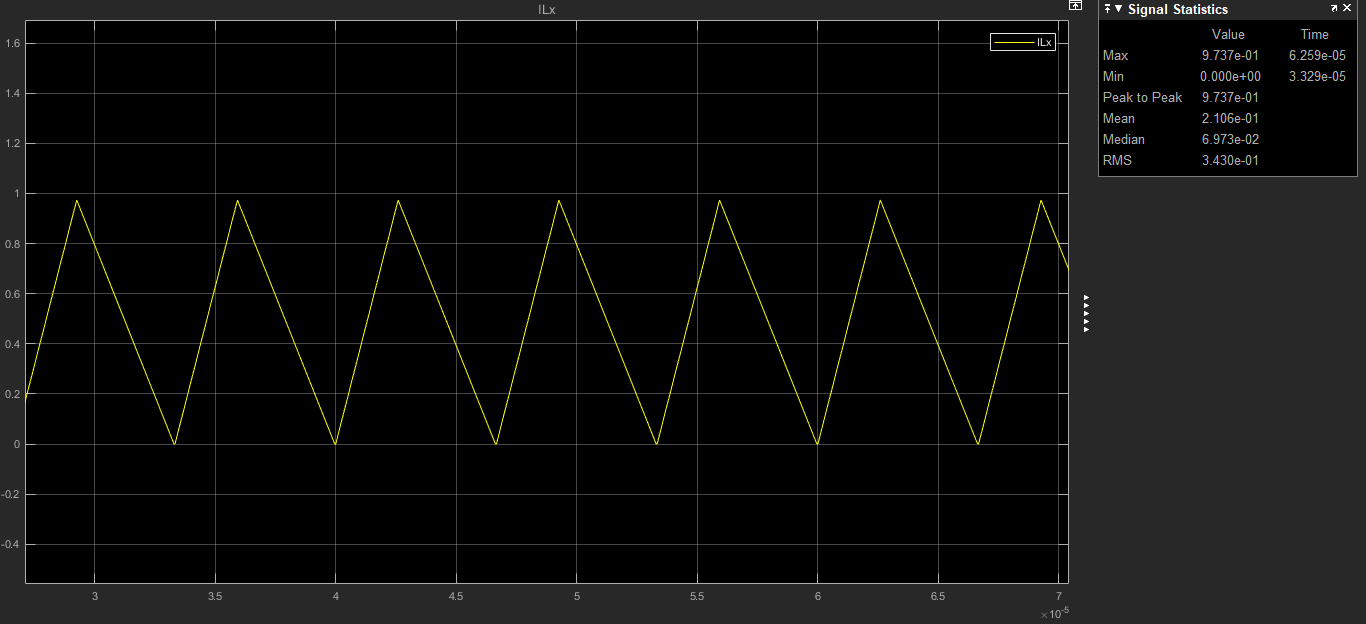
substuting ton value in above equation :

= [ Vinmax - Vo - Vdiode ]\*

= 0.98 A

where Lo = 120uH

Io = = = 0.49 A which is minimum load current with 120uH output inductor to ensure CCM mode of operation.



**Figure 7:** Output inductor current at boundary

**Efficiency Calculation:**

At %100 Load :

At %100 load load current is 4A.

Diode1 loss :

Vf = 0.7 V

Idiode = 2.54A

Ploss = 0.7\*2.54 =1.778 W

Diode2 loss :

Vf = 0.7 V

Idiode = 3.10A

Ploss = 0.7\*3.10 = 2.17 W

Inductor loss :

Irms = 4A

Rind = 42 mohm

Ploss = 4\* 0.042 = 0.0168 W

Main mosfet loss :

Irms = 4.52 A

Ron = 0.24 ohm

Ploss = 4.52\*0.24 = 1.0848 W

Transformer loss:

Ploss = 22m \* 4.52 + 16m \* 2.54 + 16m \* 0.3 = 0.145 W

Total Ploss = 5.05 W

Efficiency = = =0.96 = 96%

At %75 Load :

At %75 load load current is 3A.

Diode1 loss :

Vf = 0.7 V

Idiode = 1.91 A

Ploss = 0.7\*1.91 =1.34 W

Diode2 loss :

Vf = 0.7 V

Idiode = 2.34 A

Ploss = 0.7\*2.34= 1.64 W

Inductor loss :

Irms = 3A

Rind = 42 mohm

Ploss = 3\* 0.042 = 0.126 W

Main mosfet loss :

Irms = 3.48 A

Ron = 0.24 ohm

Ploss = 3.48\*0.24 = 0.835 W

Transformer loss:

Ploss = 22m \* 1.91 + 16m \* 3.48 + 16m \* 0.3 = 0.1 W

Total Ploss = 4 W

Efficiency = = =0.95 = 95%

At %50 Load :

At %50 load load current is 2A.

Diode1 loss :

Vf = 0.7 V

Idiode = 1.29 A

Ploss = 0.7\*1.29 =0.9 W

Diode2 loss :

Vf = 0.7 V

Idiode = 1.58 A

Ploss = 0.7\*1.58= 1.1 W

Inductor loss :

Irms = 2A

Rind = 42 mohm

Ploss = 2\* 0.042 = 0.084 W

Main mosfet loss :

Irms = 2.45 A

Ron = 0.24 ohm

Ploss = 2.45\*0.24 = 0.59 W

Transformer loss:

Ploss = 22m \* 1.29 + 16m \* 2.45 + 16m \* 0.3 = 0.7 W

Total Ploss = 3.37 W

Efficiency = = =0.94 = 94%

At %25 Load :

At %25 load load current is 1A.

Diode1 loss :

Vf = 0.7 V

Idiode = 0.65 A

Ploss = 0.7\*0.65 =0.455 W

Diode2 loss :

Vf = 0.7 V

Idiode = 0.79 A

Ploss = 0.7\*0.79= 0.553 W

Inductor loss :

Irms = 1A

Rind = 42 mohm

Ploss = 1\* 0.042 = 0.042 W

Main mosfet loss :

Irms = 1.40 A

Ron = 0.24 ohm

Ploss = 1.40\*0.24 = 0.336 W

Transformer loss:

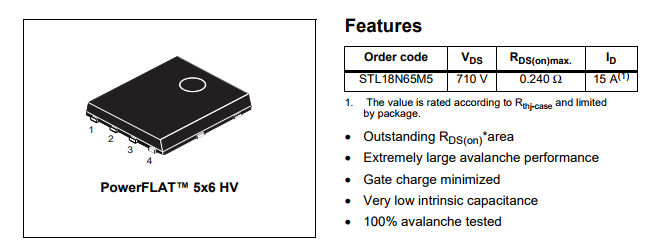
Ploss = 22m \* 0.65 + 16m \* 1.4 + 16m \* 0.3 = 0.4 W

Total Ploss = 1.79 W

Efficiency = = =0.94 = 94%

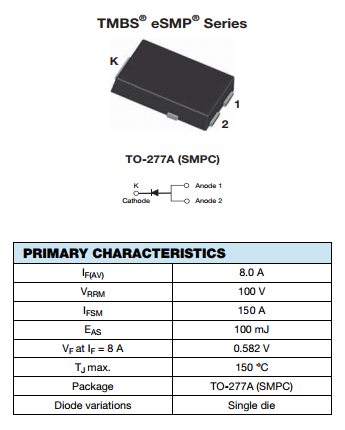
**Component selection:**

Main switch: As a main switch STL18N65M5 is selected. It has low on resistance. It is features are given below:



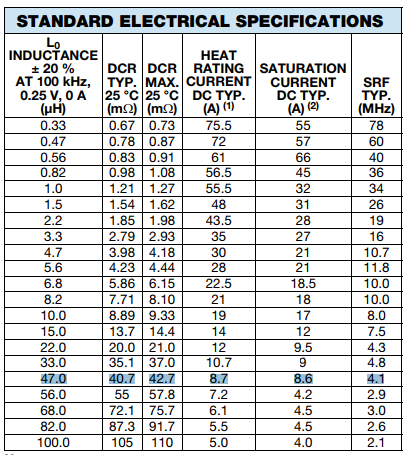
**Figure 8 :** STL18N65M5 features

For secondary diodes V8P10 - M3 from Vishay selected. It has low forward drop voltage with 100V breakdown voltage and 8A forward current which makes it suitable for our project. It is features are given below:



**Figure 9** : V8P10 - M3 features

Finally, as an output inductor, 47uH inductor with 8.6A saturation current from vishay company.

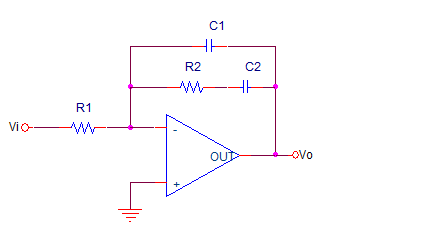


**Figure 10 :** Output inductor features

**2-Controller design**

2-a

In this section, parameters are chosen according to the designed controller in part c.



**Figure11.** Type 2 controller.

Transfer function is C1





Let’s equate this transfer function to the our controller in part c.





Let’s



R2=1.1Kohm

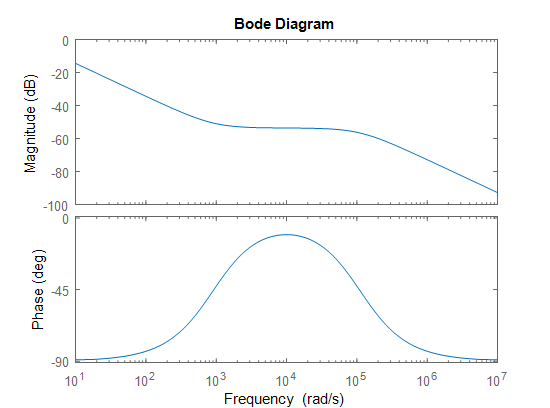


Lets R1=500Kohm

C1=F

In this system we have 2 poles and 1 zero. In addition, one of the poles is on the center of coordinate system other one is on the left side of the imaginary axis. This means open loop system is not stable. However, in order to ensure the stability, we need to use this topology on closed loop systems.

Bode plot of the controller is on following figure.

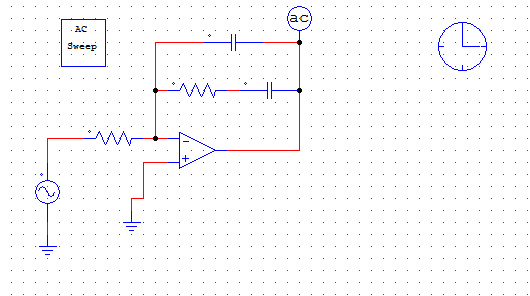


**Figure 12.** Bode plot of the system with given values.

In this bode plot, cut of frequency is almost equal to 1 and phase margin is 90 degrees. When we use this controller with a system, the system’s phase will increase around 10^4rad/s and the system’s gain will decreases gradually as frequency increase.

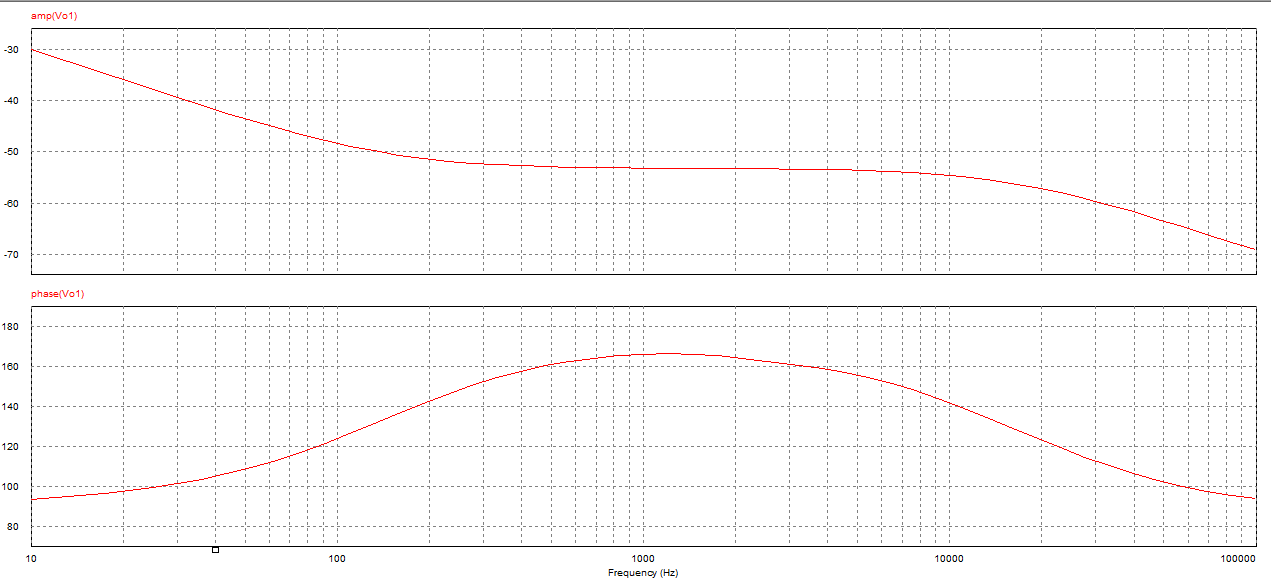
2b)

Type 2 controller circuit is designed via using PSIM and in the following figure 13.



**Figure13.** Type 2 controller

Bode plot characteristic of the controller is on figure 14.



**Figure 14**. Bode plot of the controller via using PSIM.

2-c

State equations are as follows:

On state Off state

ẋ = A1 + B1u ẋ = A2x + B2u

y= C1x y= C2x

where u is input.

Averaging them:

ẋ = [A1d +A2(1-d)] x + [B1d+B2(1-d)] u

y=C1d+C2(1-d)] x

Introducing small perturbations as follows (assuming perturbations in input is equal to zero):

x=X+x y=Y+y d=D+d

in steady state ẋ=0 and neglecting products of x and d;

ẋ=AX+Bu+Ax+[ (A1 – A2 ) X+(B1 -B2 )u]d (10-50) in text book Mohan

A = A1D + A2(1-D)

B= B1D + B2(1-D)

In steady state

AX+Bu= 0

Equation 10-50 becomes

ẋ= Ax+[ (A1 – A2 ) X+(B1 -B2 )u]d and

Y+y=CX+Cx+[(C1-C2)X]d (10-58) in text book Mohan

Where

C=C1D+C2(1-D)

Y=CX

y=Cx+[(C1-C2)X]d

Y/U=-CA-1B

Taking lap lace transform of small signal eqn. (10-58)

Y(s)/d(s)=C[sI-A]-1 [(A1-A2)X + (B1-B2)U] + (C1-C2)X

Let’s apply the formula to the buck converter state variables are defined as inductor current and capacitor voltage.

A1= [ -(R\*rc + R\*rl + rc\*rl)/(L\*(R + rc)), -R/(L\*(R + rc))]

[ R/(C\*(R + rc)) , -1/(C\*(R + rc))]

A1=A2=A;

B1= [ 1/L ]

[ 0 ]

B2=0;

B=B1\*D

For the sake of simplicity assuming R is much greater than (rc+rl);

A=A1=A2= [ -(rc + rl)/L, -1/L ]

[ 1/C , -1/(C\*R)]

C=C1=C2=[rc 1];

B remains same.

A-1=1/det(A)\* [-1/(C\*R ) , 1/L ]

[ -1/C , -(rc + rl)/L]

Finally, steady state transfer function is

==D

Small signal transfer function is as follows

=

Let’s choose;

Vd=48V

Vo=23.6V

rl=0.002ohm

L=10uH

rc=0.001ohm

C=1000uF

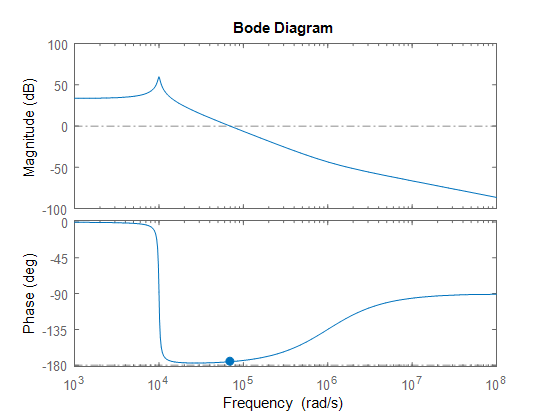
R=5ohm

Fs=150kHz

For finding gain crossover frequency: ==1;

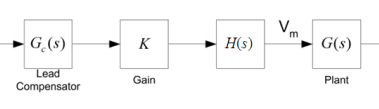
wc=7.01\*104

Bode plot characteristic of buck converter without controller can be seen on figure 15.



**Figure15**. Bode plot characteristic of open loop system without controller.

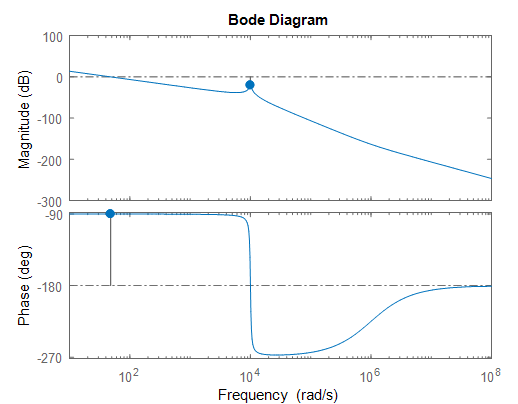
This system is stable however we have very low phase margin in this system. Lets design a lead compensator with integral term (type 2) controller for increasing the phase margin and better system characteristics. Overall open loop characteristic is as follows.



**Figure 16.** Planned open loop characteristics.

**Step1.** Satisfying the steady state error:

By choosing H(s)=1/s. This term is for eliminating the steady state error. New bode plot diagram is as follows.



**Figure17.** Bode plot with only integral term.

**Step2.** Increasing bandwidth

By adding K term to the system. Let’s say we want wc=104 rad/s.

20\*log(K\*G(s)\*H(s))=0

K=21;

**Step4.** Adjusting phase margin.

Now we have -57 degrees of phase margin which makes our system unstable. Let’s try to obtain 23 degrees of phase margin. Extra phase required to the compensate by compensator is 80 degrees. For compensator let’s choose a lead compensator which has unity DC gain. Transfer function of compensator is as follows:

Gc(s)=

where

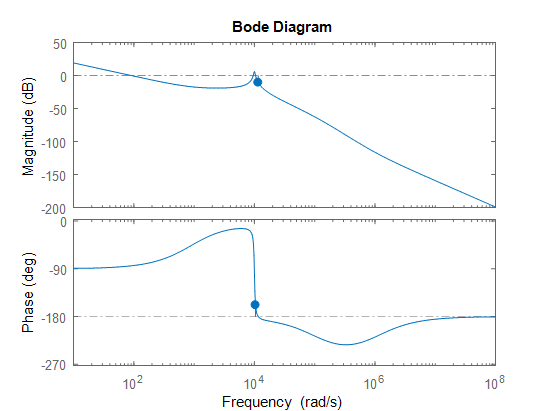
w= wc =10000

tan(a)-tan(1/a)=80

a=11

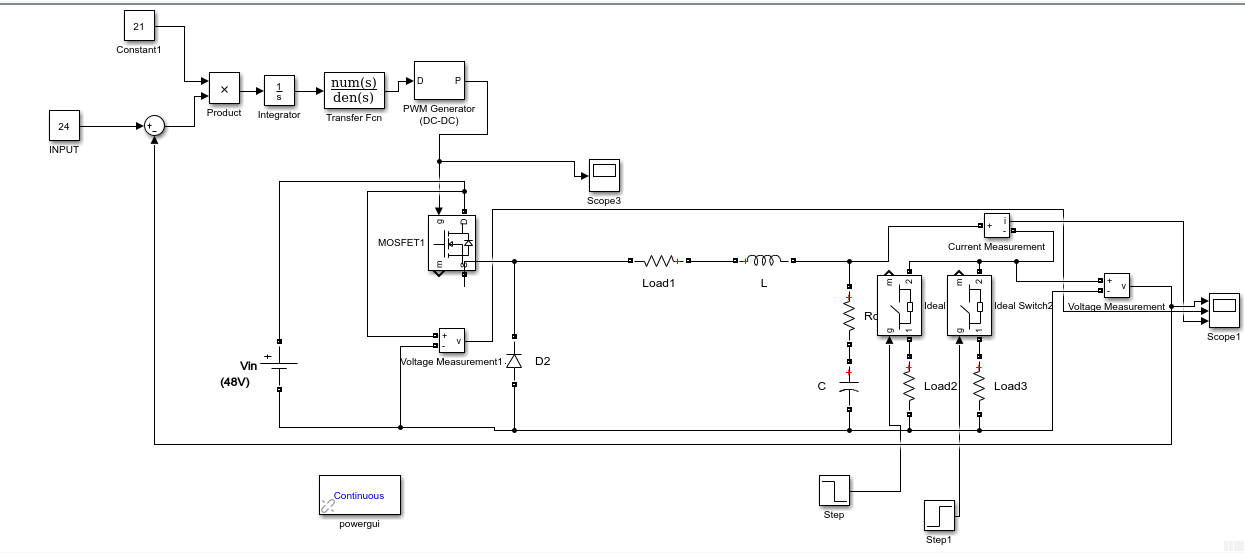
Gc(s)=

Finally, we have 21 degrees of phase margin. Final open loop bode plot characteristic is as follows:



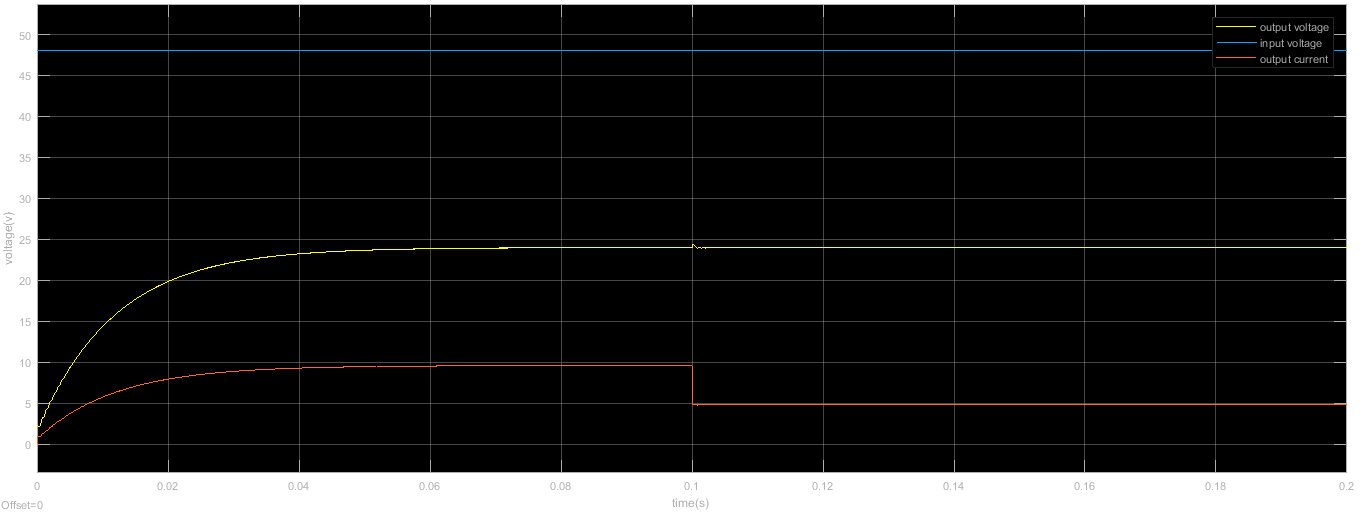
**Figure 18.** Final bode plot of the system.

d)i) case 1 load is increased, corresponding circuit is on the following figure19.



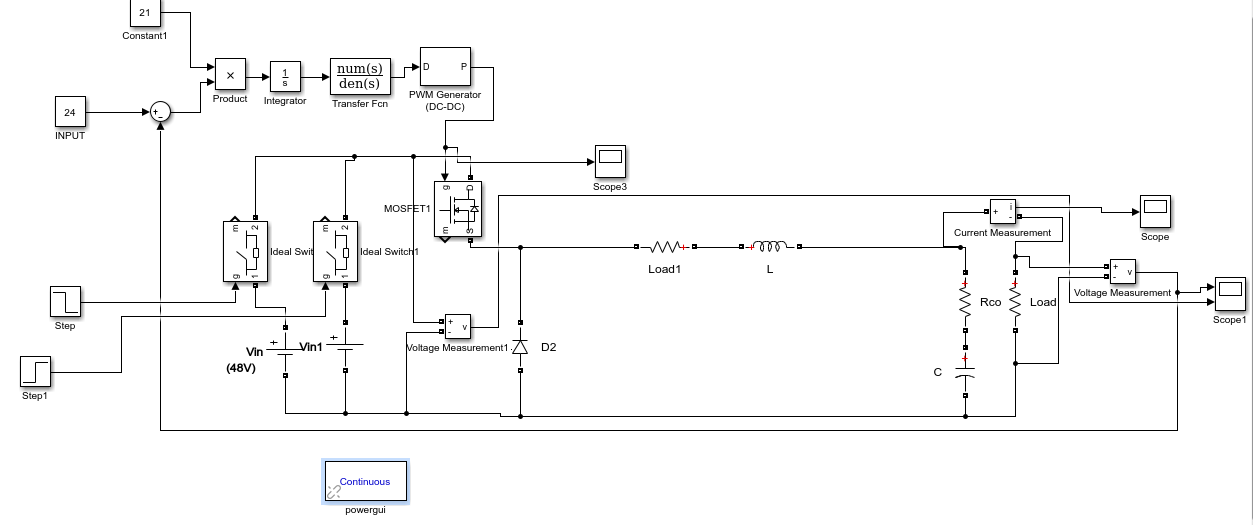
**Figure 19.** load is increased.

Simulation results are on the following figure20.



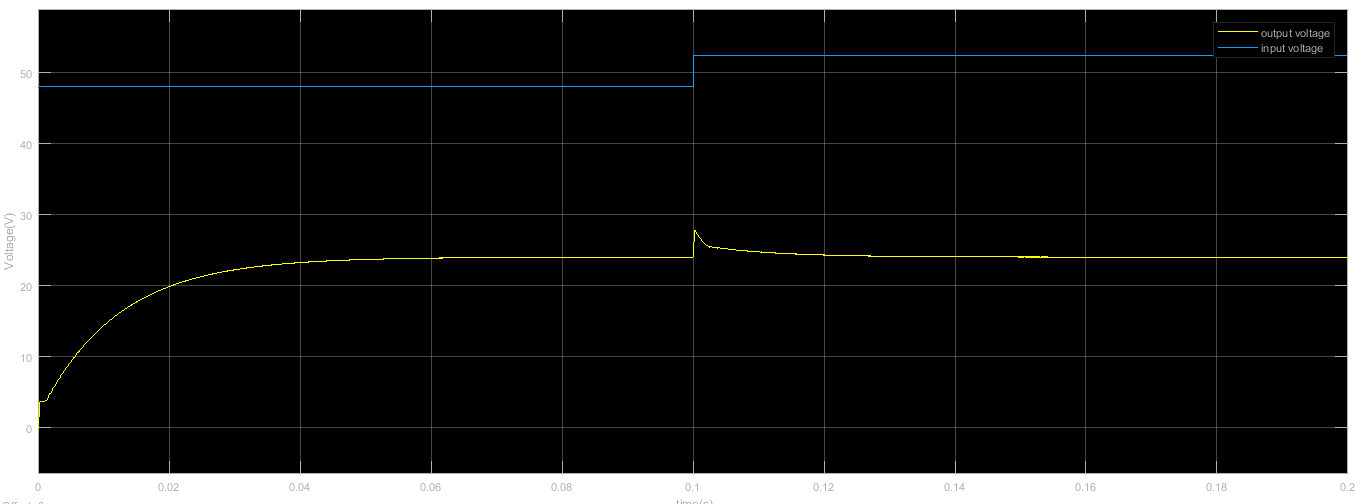
**Figure 20.** Step change from half load to full load case

d)ii) Overall circuit schematic is on the following figure 21.



**Figure21.** overall system circuit

Output voltage waveform is on the following figure22.



**Figure 22.** input voltage is increased %10 and corresponding output voltage.

e) Transient performance is good enough. However, the controller is working on close to the unstable region which causes real implements may not work.