ECE 472 – Final Project Ashtyn Moehlenhoff

Extending the Pipelined MIPS Verilog Model Torben Rasmussen

**Part I:**

Jump Instruction:

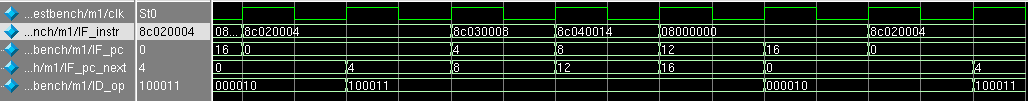
Test code:

5'd0 : data\_out = { 6'd35, 5'd0, 5'd2, 16'd4 }; // lw $2, 4($0) r2=1

5'd1 : data\_out = { 6'd35, 5'd0, 5'd3, 16'd8 }; // lw $3, 8($0) r3=2

5'd2 : data\_out = { 6'd35, 5'd0, 5'd4, 16'd20 }; // lw $4, 20($0) r4=5

5'd3 : data\_out = { 6'd2, 26'd0 }; // j 0 restart loop



Explanation: