Adder_blk.pdf

```
always @ (posedge clk, negedge reset_n)
  if (!reset_n) acc_out <= 12'h000;
  else
    if (rd_fifo == 1'b1)
      if (first_select == 1'b1)  acc_out <= data;
      else                       acc_out <= acc_out + data;
endmodule
```