Rasool Sharifi

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Overview

My research interests lie broadly in Computer Architecture, Compilers, and Computer Security. My research explores novel hardware and software techniques to design secure machines while maintaining performance, energy efficiency, and high programmability. I'm also interested in applying novel machine learning techniques to detect and mitigate security threats. I have extensive experience in designing high performance, energy efficient FPGA and embedded systems for core consumer products. Recent research highlights include:

•**Hardware Security:** High performance and transparent capability based protection mechanism to secure unmodified source and object code against temporal and spatial memory safety exploits

•**Processing in Memory:** DRAM-based in-situ k-mer matching accelerator design for simultaneous comparisons of millions of DNA base pairs

•**Side-Channel Attacks :** Study existing SRAM, DRAM, and RRAM-based neural accelerators from a security perspective and evaluate the feasibility of launching model extraction attacks on such architectures

Education

University of Virginia, Charlottesville, USA — Sep. 2018 - Present
Ph.D., Computer Science

University of Tehran, Tehran, Iran — Sep. 2013 - June 2016
M.Sc., Electronics-Circuit and Systems

Isfahan University of Technology, Isfahan, Iran — Sep. 2009 - June 2013
B.Sc., Electrical Engineering

Research Experience

University of Virginia, Charlottesville, USA, — Sep. 2018 - Present
Graduate Research Assistant
Projects:
- Architecture Support for Memory Safety
- Side-Channel Attacks and Defenses
- Processing in Memory for Bioinformatics Applications

University of Tehran, Iran, USA, — Sep. 2013 - June 2016
Graduate Research Assistant
Projects:
- Cluster Specific Multi-Rate Refreshing in Modern DRAM Systems
- Design and Implementation of SMPTE 2022-6 Video Over IP Transmitter and Receiver Cores
- Design and Implementation of a Multi-touch Framework Based on ARM-M3 Micro-Controllers

Work Experience

Huawei Technology Co., Tehran, Iran, — July. 2015 - December. 2016
Wireless Engineer

Publications

- **Rasool Sharifi** and Ashish Venkat, "CHEx86: Context-Sensitive Enforcement of Memory Safety via Microcode-Enabled Capabilities," in *2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, 2020, **Acceptance Rate: 18%**
- **Rasool Sharifi** and Zain Navabi, "Online Profiling for cluster-specific variable rate refreshing in high-density DRAM systems," in *2017 22nd IEEE European Test Symposium (ETS)*, 2017
- Lingxi Wu, **Rasool Sharifi**, Marzieh Lenjani, Ashish Venkat, and Kevin Skadron, "Sieve: A Scalable In-Situ DRAM-based Accelerator for Massively Parallel K-mer Matching," In Submission

Skills

Programming Languages/APIs:
• C/C++, Python, Bash, Assembly Programming (x86), VHDL, Verilog, SystemC

Simulators and Analyzers:
• Gem5 Architectural Simulator, McPAT, MARSSx86, Sniper Multi-Core Simulator, DRAMSim2, Ramulator, CACTI

Benchmarking and Performance Analysis:
• SPEC Benchmarks, SimPoints, Pin

Industry Software Skills:
• HSpice , Matlab , Modelsim ,Vivado, Quartus, Xilinx ISE, Xilinx EDK,Matlab System Generator

Practical Skills:
• SOC Design on FPGA, Embedded Linux on FPGA

Notable Projects

Architecture Support for Memory Safety, *ISCA 2020*
Language: *C++, Python*, **Framework:** *GEM5*

Processing in Memory for Bioinformatics Applications, *Submitted to HPCA 2021*
• This work proposes and evaluates three DRAM-based in-situ k-mer matching accelerator designs (one optimized for area,one optimized for throughput, and one that strikes a balance between hardware cost and performance),
• A novel data mapping scheme to allow for simultaneous comparisons of millions of DNA base pairs, lightweight matching circuitry for fast pattern matching
• Evaluation of Sieve using state-of-the-art workloads with real-world datasets shows that the most aggressive design provides an average of 326x/32x speedup and 74X/48x energy savings over multi-core-CPU/GPU baselines for k-mer matching.
Language: *C++, Python*, **Framework:** *DRAMSim2*

Cluster Specific Multi-Rate Refreshing in Modern DRAM Systems, *ETS 2017*
• We propose a method based on classification concept in machine learning for prediction of suitable refresh rate of the DRAM modules.
• A classification model is trained at different temperature and temperature variation rates.The trained model as a high level module proactively sets refresh rate of the DRAM module based on the temperature.
• For a realistic evaluation of our work, we use an Altera Stratix IV FPGA based on Terasic DE4 platform for implementation of our proposed method.
Language: *Verilog, VHDL, C*, **Platform:** *Terasic DE4*

Design and Implementation of SMPTE 2022-6 Video Over IP Transmitter and Receiver Cores
Language: *VHDL, Verilog*, **Platform:** *Xilinx Virtex 7*

Design and Implementation of a Multi-touch Framework Based on ARM-M3 Micro-Controllers
Language: *C, C++, Assembly*

Teaching Experience

Teaching Assistant, CS3330: Undergraduate Computer Architecture , Spring 2020
University of Virginia

Teaching Assistant, CS6354: Graduate Computer Architecture, Fall 2020
University of Virginia

Teaching Assistant, Digital Logic Design Laboratory, September 2012 – June 2015
University of Tehran