DESIGN 1 (Register Bank):

قطعات و تراشه های استفاده شده:

```
------------------------------
# BELS                   : 4217
#      INV                : 1
#      LUT2               : 1
#      LUT3               : 80
#      LUT5               : 2299
#      LUT6               : 1835
#      MUXF7              : 1
# FlipFlops/Latches       : 2176
#      FDR                : 128
#      FDRE               : 2048
# Clock Buffers           : 1
#      BUFGP              : 1
# IO Buffers              : 78
#      IBUF               : 45
#      OBUFT              : 33
```

بررسی میزان بهره برداری:

```
Slice Logic Utilization:
 Number of Slice Registers:         2176  out of  18224    11%
 Number of Slice LUTs:              4216  out of   9112    46%
   Number used as Logic:            4216  out of   9112    46%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   4216
   Number with an unused Flip Flop:    2040  out of   4216    48%
   Number with an unused LUT:             0  out of   4216     0%
   Number of fully used LUT-FF pairs:  2176  out of   4216    51%
   Number of unique control sets:       128
```

گزارش تایمینگ:

Speed Grade: -3

Minimum period: 1.507ns (Maximum Frequency: 663.460MHz)
Minimum input arrival time before clock: 9.790ns
Maximum output required time after clock: 7.813ns
Maximum combinational path delay: 13.285ns

حداکثر فرکانس کلاک: 663.460MHz

DESIGN 2 (m_counter):

قطعات و تراشه های استفاده شده:

```
------------------------------
# BELS                 : 140
#      GND             : 1
#      INV             : 4
#      LUT2            : 13
#      LUT3            : 15
#      LUT4            : 28
#      LUT5            : 16
#      LUT6            : 6
#      MUXCY           : 32
#      VCC             : 1
#      XORCY           : 24
# FlipFlops/Latches    : 29
#      FDC             : 3
#      FDCE            : 26
# Clock Buffers        : 1
#      BUFGP           : 1
# IO Buffers           : 48
#      IBUF            : 23
#      OBUF            : 25
# DSPs                 : 2
#      DSP48A1         : 2
```

بررسی میزان بهره برداری:

```
Slice Logic Utilization:
 Number of Slice Registers:          29  out of  18224    0%
 Number of Slice LUTs:               82  out of   9112    0%
   Number used as Logic:             82  out of   9112    0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    84
   Number with an unused Flip Flop:     55  out of    84   65%
   Number with an unused LUT:            2  out of    84    2%
   Number of fully used LUT-FF pairs:   27  out of    84   32%
   Number of unique control sets:        7
```

گزارش تایمینگ:

Speed Grade: -3

Minimum period: 2.772ns (Maximum Frequency:)
Minimum input arrival time before clock: 3.685ns
Maximum output required time after clock: 16.239ns
Maximum combinational path delay: 6.970ns

حداکثر فرکانس کلاک: 360.789MHz

DESIGN 3 (sequence detector)

قطعات و تراشه های استفاده شده:

```
------------------------------
# BELS                   : 77
#      GND               : 1
#      INV               : 3
#      LUT1              : 15
#      LUT2              : 2
#      LUT3              : 18
#      LUT4              : 2
#      LUT5              : 1
#      LUT6              : 2
#      MUXCY             : 15
#      MUXF7             : 1
#      VCC               : 1
#      XORCY             : 16
# FlipFlops/Latches      : 27
#      FD_1              : 7
#      FDRE              : 4
#      FDRE_1            : 16
# Clock Buffers          : 1
#      BUFGP             : 1
# IO Buffers             : 21
#      IBUF              : 4
#      OBUF              : 17
```

بررسی میزان بهره برداری:

```
Slice Logic Utilization:
 Number of Slice Registers:          27  out of  18224    0%
 Number of Slice LUTs:               43  out of   9112    0%
   Number used as Logic:             43  out of   9112    0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    46
   Number with an unused Flip Flop:     19  out of    46   41%
   Number with an unused LUT:            3  out of    46    6%
   Number of fully used LUT-FF pairs:   24  out of    46   52%
   Number of unique control sets:        3
```

گزارش تایمینگ:

Timing Summary:

Speed Grade: -3

Minimum period: 3.120ns (Maximum Frequency:)
Minimum input arrival time before clock: 3.886ns
Maximum output required time after clock: 3.668ns
Maximum combinational path delay: No path found

حداکثر فرکانس کلاک: 320.508MHz

DESIGN 4 (divisible by 7)

قطعات و تراشه های استفاده شده:

```
------------------------------
# BELS                  : 4
#      LUT3             : 1
#      LUT4             : 3
# FlipFlops/Latches           : 3
#      FDR              : 3
# Clock Buffers               : 1
#      BUFGP            : 1
# IO Buffers                  : 6
#      IBUF             : 2
#      OBUF             : 4
```

بررسی میزان بهره برداری:

```
Slice Logic Utilization:
 Number of Slice Registers:          3  out of  18224    0%
 Number of Slice LUTs:               4  out of   9112    0%
   Number used as Logic:             4  out of   9112    0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     7
   Number with an unused Flip Flop:      4  out of     7   57%
   Number with an unused LUT:            3  out of     7   42%
   Number of fully used LUT-FF pairs:    0  out of     7    0%
   Number of unique control sets:        1
```

گزارش تایمینگ:

```
Timing Summary:
---------------
Speed Grade: -3

  Minimum period: 1.714ns (Maximum Frequency)
  Minimum input arrival time before clock: 2.425ns
  Maximum output required time after clock: 4.745ns
  Maximum combinational path delay: No path found
```

حداکثر فرکانس کلاک: 583.431MHz