

FT61F02X

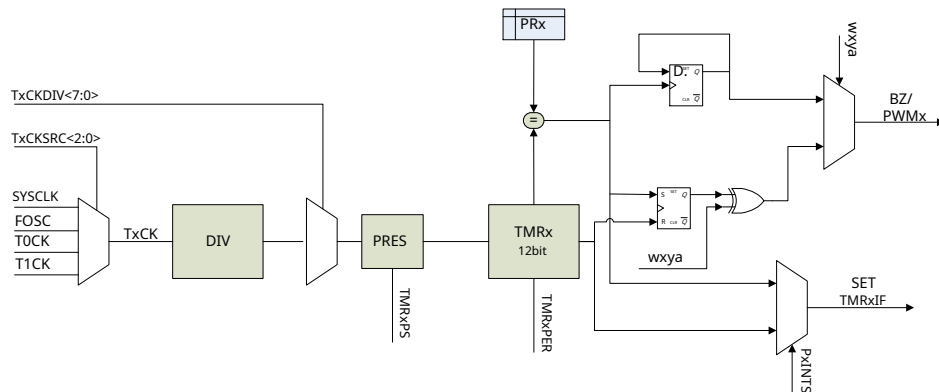
PWM345 Application note

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FT61F02x PWM3/4/5 application

1. PWMx and TIMERx



picture1-1 PWM3/4/5 Structure diagram

Apart from ECCP provided by the module 1 Road Enhanced PWM Besides, On-chip also integrates 3 Road time base and duty cycle are independent of each other 12bit PWM, They all have the following properties:

- increment counter
- BUZZER/PWM output optional BUZZER/
- PWM output polarity selectable 8 kind
- PWM resolution
- 4 Two kinds of clock sources are optional
- 1~256 frequency division optional
- 7bit prescaler
- Overflow interrupt or match interrupt
- Clock Modulation Output

TIMER3/4/5 are all 12bit-up counter that can be registered via the TMRxH:TMRxL (x can be 3/4/5). To access the count value, the software TMRxH:TMRxL write operation will directly update the count value. when PxEN (PWMxCR1.7) for 0, work in timer mode. When the internal clock is selected as the counting source, it is a timer, and when the external clock is selected as the counting source, it is a counter.

Timer3/4/5 overflow cycle

TIMERx The maximum number of digits is 12bit, by pairing PxPER[2:0]. The configuration can choose different overflow period.

- exist BUZZER mode, when the count value and PR. When the registers are equal, another count clock TIMERx will automatically clear 0;
- exist TIMERx overwrite if already enabled PxPER. The value of TMRxIF place 1, it is recommended to configure the PxPER turned on after TMRx ON.

when TIMERx count value TMRxH:TMRxL increments to the maximum count value (by PxPER specified), at this time TIMERx An overflow occurs and sets the interrupt flag (TMRxIF), and TMRxH:TMRxL register will reset on the next increment cycle to 0x00. Triggering an interrupt and/or waking up from sleep after an overflow depends on the corresponding enable/shutdown control bit (GIE, PEIE and TMRxIE). Exit on interrupt service

flagTMRxIFclear0, so as not to loop into a break.

To wake from sleep, configure to use an external clockT0CK/T1CK (PxCKSRC=010or011),otherwiseTimer1will stop

Count, maintaining the count value it had before going to sleep.

Timer3/4/5Summary of related registers

name	state		register	address	reset value
PxPER	<u>PWMxcycle selection</u>		PWMxCR0 [6:4] x = 3,4,5	0x10F/ 0x115/ 0x11B	RW-000
	000 =4bit	100 = 9bit			
	001 = 5bit	101 = 10bit			
	010 = 6bit	110 = 11bit			
	011 = 8bit	111 = 12bit			
wxya	<u>TIMERx/PWMxclock selection 1</u>		PWMxCR0 [3:1] x = 3,4,5	0x10F/ 0x115/ 0x11B	RW-000
	000 =system clock/(TxCKDIV+1)				
	001 = HIRC/(TxCKDIV +1) 010 = T0CK/(TxCKDIV +1) 011 = T1CK/ (TxCKDIV +1)				
	100 = HIRC/(TxCKDIV +1), PWM3output low level 101 = HIRC/(TxCKDIV +1), PWM3output high level 110 = HIRC/(TxCKDIV +1), PWM3According to the high pulse modulationPxCK 111 = HIRC/(TxCKDIV +1), PWM3According to low pulse modulationwxya				
wxya	<u>output selection</u>	1 = BUZZERoutput 0 = PWMoutput	PWMxCR0[0] x = 3,4,5		RW-0
wxya	<u>TIMERx/PWMxOperating mode</u>	1 = PWM/BUZZERmodel_ 0 =timer mode	PWMxCR1[7] x = 3,4,5		RW-0
wxya	<u>PWMxoutput polarity</u>	1 =active low 0 =active high	PWMxCR1[6] x = 3,4,5		RW-0
TMRxPS	<u>PWMxPrescaler2</u>		PWMxCR1 [5:3] x = 3,4,5		0x110/ 0x116/ 0x11C
	000 = 1:1	100 = 1:16			
	001 = 1:2	101 = 1:32			
	010 = 1:4	110 = 1:64			
	011 = 1:8	111 = 1:128			
TMRxON	<u>TIMERxenable bit</u>	1 =Enable 0 =closure	PWMxCR1[2] x = 3,4,5		RW-0
T3CKDIV	TMR3The clock frequency isfT3CK/ (T3CKDIV + 1)3		T3CKDIV[7:0]	0x111	RW-0000 0000
T4CKDIV	TMR4The clock frequency isfT4CK/ (T4CKDIV + 1)3		T4CKDIV[7:0]	0x117	RW-0000 0000

¹Note: Select as internalRCfast clock (HIRC)When the system clock selects slow clock, external clock or crystal clock, the internalHIRCwill be on unless in sleep mode

²Prescaler CounterTMRxPSCan not read and write directly, when theTMRxH/xLWhen the register is written, the prescaler counter is automatically cleared0.

³Note: When rightTxCKDIVWhen the register is written, the divisor divider will be automatically cleared0.

name	state	register	address	reset value
T5CKDIV	TMR5The clock frequency is $f_{T5CK} / (T5CKDIV + 1)$ ³	T5CKDIV[7:0]	0x11D	RW-0000 0000
TMR3L	TMR3Count result register low8bit	TMR3L[7:0]	0x10C	RW-xxxx xxxx
TMR3H	TMR3Count result register high4bit	TMR3H[7:4]	0x10D	RW-xxxx
PR3H	PR3Period Register High4bit	TMR3H[3:0]		RW-1111
PR3L	PR3Period Register Low8bit	PR3L[7:0]	0x10E	RW-1111 1111
TMR4L	TMR4Count result register low8bit	TMR4L[7:0]	0x112	RW-xxxx xxxx
TMR4H	TMR4Count result register high4bit	TMR4H[7:4]	0x113	RW-xxxx
PR4H	PR4Period Register High4bit	TMR4H[3:0]		RW-1111
PR4L	PR4Period Register Low8bit	PR4L[7:0]	0x114	RW-1111 1111
TMR5L	TMR5Count result register low8bit	TMR5L[7:0]	0x118	RW-xxxx xxxx
TMR5H	TMR5Count result register high4bit	TMR5H[7:4]	0x119	RW-xxxx
PR5H	PR5Period Register High4bit	TMR5H[3:0]		RW-1111
PR5L	PR5Period Register Low8bit	PR5L[7:0]	0x11A	RW-1111 1111

surface1-1 Timer3/4/5Related User Control Registers

name	state	register	address	reset value
GIE	<u>global interrupt</u> 1 =Enable (PEIE, TMR2IEBe applicable) 0 = <u>global shutdown</u> (wake up is not affected)	INTCON[7]	0x0B 0x8B 0x10B	RW-0
PEIE	Total Peripheral Interrupt 1 =Enable (TMR2IEBe applicable) 0 = <u>=closure</u> (no wakeup)	INTCON[6]		RW-0
P3INTS	Timer3interrupt select bit 1 = TMR3andPR3match break 0 = TMR3overflow interrupt	PWM3CR0[7]	0x10F	RW-0
TMR3IE	Timer3interrupt enable bit 1 =Enable 0 = <u>=closure</u> (no wakeup)	PWM3CR1[1]	0x110	RW-0
TMR3IF	Timer3interrupt flag 1 =match/overflow (latch) 0 = <u>no match/no overflow</u>	PWM3CR1[0]		RW-0
P4INTS	Timer4interrupt select bit 1 = TMR4andPR4match break 0 = TMR4overflow interrupt	PWM4CR0[7]	0x115	RW-0
TMR4IE	Timer4interrupt enable bit 1 =Enable 0 = <u>=closure</u> (no wakeup)	PWM4CR1[1]	0x116	RW-0
TMR4IF	Timer4interrupt flag 1 =match/overflow (latch) 0 = <u>no match/no overflow</u>	PWM4CR1[0]		RW-0
P5INTS	Timer5interrupt select bit 1 = TMR5andPR5match break 0 = TMR5overflow interrupt	PWM5CR0[7]	0x11B	RW-0
TMR5IE	Timer5interrupt enable bit 1 =Enable 0 = <u>=closure</u> (no wakeup)	PWM5CR1[1]	0x11C	RW-0
TMR5IF	Timer5interrupt flag 1 =match/overflow (latch) 0 = <u>no match/no overflow</u>	PWM5CR1[0]		RW-0

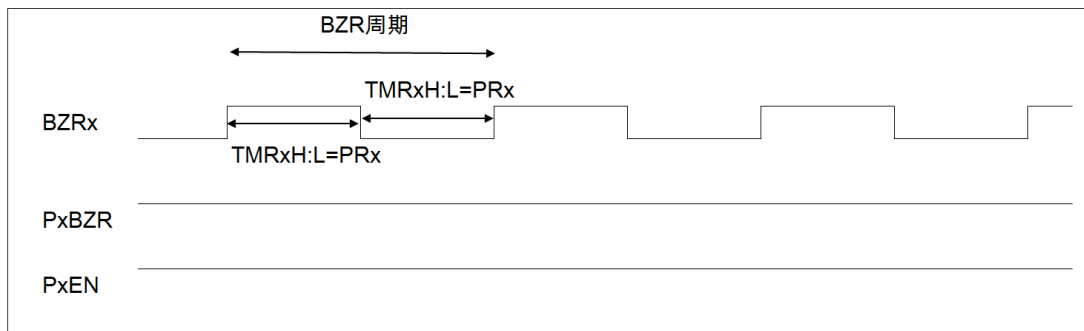
surface1-2 Timer3/4/5Interrupt Enable and Status Bits

1.1. TMRxH/Lreading and writing

TIMERx is an asynchronous clock, which is read by software in the running state. The count value may be read when the low 8 bits after the overflow occurs and the count value is reset. At this time, if it is read high again, then 0.

For write operations, it is recommended to first stop TIMERx (TMRxON=0), and then write the target value into TMRxH/TMRxL.

1.2. BUZZER Operating mode



picture1-2 50% duty cycle BUZZER square wave

BUZZER cycle

formula 1.1
$$T_{BUZ} = 2 * 2^{TMRxPS} * PRx * T_{wxya}$$

Notice:

1. work at BUZZER mode, TIMERx automatically work on 12-bit mode, with PxBZPERThe value of

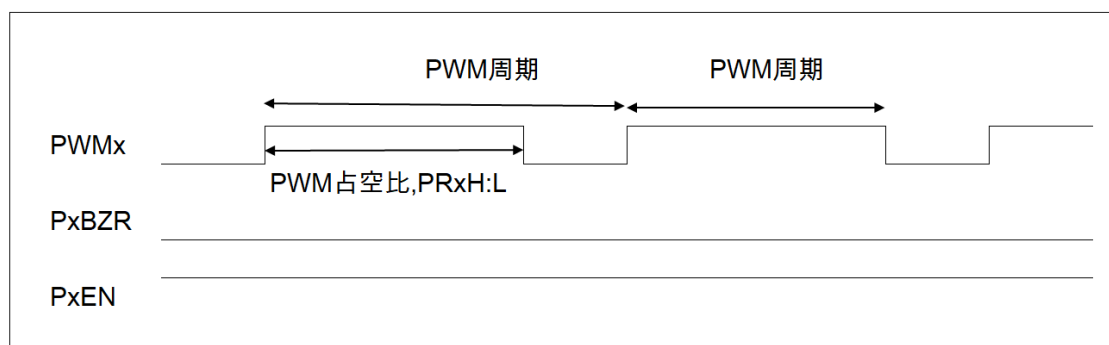
2. when TMRxH:L equal PRx, TMRxH:L will automatically clear 0

3. BUZZER mode:

- if PRx=0x000, but wxya in fixed output 0 12-bit of
- TIMERx when overflow TMRxIF will be set 1

4. same TIMER The same mode, through the configuration (wxya, wxya, TMRxON, TMRxIE, PEIE) and "PxCKSRC = 010 or 011", BUZZER can work in sleep mode

1.3. PWM Operating mode



picture1-3 PWMx Working mode (forward output)

Notice:

If you want to use both ECCP of PWM (P1A pin output PWM modulation) and PWM3/4/5, the register CCP1CON of P1M<1:0> to be configured as 00 (Single output mode = P1A modulation, P1B/P1C/P1D for the port). which is, ECCP priority ratio PWM3/PWM4/PWM5 high.

PWMx cycle

PWMx cycle by TIMERx The prescaler setting register of the TMRxPS and PxPER decided together.

$$\text{formula 1.2} \quad \text{PWM period} = 2^{\text{TMRxPS}} * 2^{\text{Nbit}} * T_{\text{wxya}}$$

- Nbit for PxPER The number of timer digits set.

PWMx duty cycle

PWM The duty cycle is set by the register PRxH:LD. PRxH:LT total 12 bit, the software needs to be written twice separately. software writing PRxH:LT the value of will take effect immediately and will directly affect the current PWMx duty cycle is recommended at start-up TIMERx Before writing the target value into PRx.

$$\text{formula 1.3} \quad T_{\text{pwm}} = 2^{\text{TMRxPS}} * (\text{PRx}) * T_{\text{wxya}}$$

PWMx configuration

1. will be related TRIS Location 1, prohibit PWMx pin output driver

2. Write PWMxCR0 register value, set PWMx Period, interrupt generation method and selection of clock source

3. Write PWMxCR1 Register value, configured as PWM mode, and the prescaler

4. load PRx register, set PWM duty cycle

5. configure and start TIMERx:

- Will PWMxCR1 register TMRXIF interrupt flag bit cleared
- Will PWMxCR1 register TMRxON Location 1 start up TIMERx

6. start over PWM cycle after enabling PWM output:

- wait TIMERx overflow (PWMxCR1 register TMRxIF Location 1)
- will be related TRIS bit clear enable PWMx pin output driver

7. same TIMER The same mode, through the configuration (wxya, wxya, TMRxON, TMRxIE, PEIE) and "PxCKSRC = 010 or 011", PWM can work in sleep mode

Note: if PWM The clock is set to the system clock (PxCKSRC=000), then any change in the system clock frequency will result in PWM frequency changes.

2.Application example

```

/*file name:TEST_61F02x_PWM345.C
* Features:    FT61F02x-EnhancedPWMDemo
*IC:          FT61F023 SOP16
* Crystal:    16M/2T
* illustrate:  This program is used to demonstratePWM345Features
*
*              In the demo program inPWM345output2kHz, 1kHz, 500Hz The
*              duty cycle is50%signal of
*
*              FT61F023 SOP16
*
*              -----
* VDD-----| 1(VDD) (VSS)16|-----GND
* NC-----| 2(PA7)   (PA0)15|-----NC
* NC-----| 3(PA6)   (PA1)14|-----NC
* NC-----| 4(PA5)   (PA2)13|-----NC
* PWM4-----| 5(PC3)   (PA3)12|-----NC
* PWM5-----| 6(PC2)   (PC0)11|-----NC
* NC-----| 7(PA4)   (PC1)10|-----NC
* NC-----| 8(PC5)   (PC4)09|----PWM3
*
*              -----
*/

# include "SYSCFG.h"

//*****Macro definition *****
//PWMPin input and output control
#define  PWM3Dir    TRISC4
#define  PWM4Dir    TRISC3
#define  PWM5Dir    TRISC2

/*-----
* Function name:interrupt
* Features:    interrupt handling
* enter:    none
* output:    none
*
*-----
---- * / void interrupt ISR(void)
{
    NOP();
}
/*-----
* Function name:POWER_INITIAL
* Features:    Power-on system initialization
* enter:    none
* output:    none
*
*-----
----- */ void POWER_INITIAL (void)

```



```

{
    OSCCON = 0B01110001;           //IRCF=111=16MHz/2=8MHz,0.125µs//Temporarily
    INTCON = 0;                     disable all interrupts
    PORTA = 0B00000000;
    TRISA = 0B00000000;           //PAinput Output1-enter0-output
    PORTC = 0B00000000;
    TRISC = 0B00000000;           //PCinput Output1-enter0-output

    WPUA = 0B00000000;           //ban allAPull up
    WPUC = 0B00000000;           //ban allPCpull up
    OPTION = 0B00001000;         //Bit3=1, WDT MODE, PS=000=WDT RATE 1:1
    MSCKCON = 0B00000000;
    //Bit6->0,prohibitPA4,PC5Regulated output
    //Bit5->0,TIMER2the clock isFosc //Bit4->0,
    prohibitLVR

    CMCON0 = 0B00000111;         //turn off the comparator,Cxfor numbersIOmouth
}

/*-----
* Function name:PWM_INITIAL
* Features:PWM3,4,5initialization
* set upPWM3period =2 TMRXPS*2 PXPEN*[(T3CKDIV+1)/PWMclock source]
*           =2 0*2 8*[(30+1)/16000000]=496µs
*   PWM4period =2 TMRXPS*2 PXPEN*[(T4CKDIV+1)/PWMclock source]
*           =2 0*2 8*[(62+1)/16000000]=1.008ms
*   PWM5period =2 TMRXPS*2 PXPEN*[(T5CKDIV+1)/PWMclock source]
*           =2 0*2 8*[(124+1)/16000000]=2ms
*
*-----
---- */ void PWM_INITIAL (void)
{
    PWM3Dir = 1;                  //PWM3outputPINTemporarily in input mode //
    PWM4Dir = 1;                  PWM4outputPINTemporarily in input mode //
    PWM5Dir = 1;                  PWM5outputPINTemporarily in input mode
    //-----PWM3-----
    PWM3CR0 = 0B00110010;
    //Bit7:      disable interrupt
    //Bit[6:4]:Period bit selection011-8bit
    //Bit[3:1]:clock selection001-internalRCfast clock/(
    T3CKDIV+1) //Bit0: PWMoutput

    PWM3CR1 = 0B10000000;
    //Bit7:      1-TMR3forPWM/BUZZERmodel
    //Bit6:      0-PWM3active high
    //Bit[5:3]:  000-PWM3The prescaler is set to1:1

```

```
//Bit2:      0-temporarily closedTMR3
//Bit1:      0-prohibitTMR3to interrupt
//Bit0:      0-TMR3Interrupt flag bit read only
```

```
TMR3H=0;
T3CKDIV = 30;          //assignmentT3CKDIV
PR3L = 128;
//-----PWM4-----
PWM4CR0 = 0B00110010;
//Bit7:      disable interrupt
//Bit[6:4]:  Period bit selection011-8bit
//Bit[3:1]:  clock selection001-internalRCfast clock/(T4CKDIV+1)
//Bit0:      PWMOutput
```

```
PWM4CR1 = 0B10000000;
//Bit7:      1-TMR4forPWM/BUZZERmodel
//Bit6:      0-PWM4active high
//Bit[5:3]:  000-PWM4The prescaler is set to1:1
//Bit2:      0-temporarily closedTMR4
//Bit1:      0-prohibitTMR4to interrupt
//Bit0:      0-TMR4Interrupt flag bit read only
```

```
TMR4H=0;
T4CKDIV = 62;          //assignmentT4CKDIV
PR4L = 128;
//-----PWM5-----
PWM5CR0 = 0B00110010;
//Bit7:      disable interrupt
//Bit[6:4]:Period bit selection011-8bit
//Bit[3:1]:clock selection001-internalRCfast clock/(
T5CKDIV+1) //Bit0: PWMOutput
```

```
PWM5CR1 = 0B10000000;
//Bit7:      1-TMR5forPWM/BUZZERmodel
//Bit6:      0-PWM5active high
//Bit[5:3]:  000-PWM5The prescaler is set to1:1
//Bit2:      0-temporarily closedTMR5
//Bit1:      0-prohibitTMR5to interrupt
//Bit0:      0-TMR5Interrupt flag bit read only
```

```
TMR5H=0;
T5CKDIV = 124;         //assignmentT5CKDIV
PR5L = 128;
```

```
}
```

```

/*-----
* Function name:main
* Features:    main function
* enter:    none
* output:    none
-----
---- */ void main(void)
{
    POWER_INITIAL();
    PWM_INITIAL();

    TMR3ON=1;
    TMR4ON=1;
    TMR5ON=1;
    PWM3Dir = 0;           //PWM3 PINSet to output mode to allowPWMoutput //
    PWM4Dir = 0;           PWM4 PINSet to output mode to allowPWMoutput //
    PWM5Dir = 0;           PWM5 PINSet to output mode to allowPWMoutput
    while(1)
    {
        NOP();
    }
}

```

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