



Fremont Micro Devices

FT61F02 Data Sheet

Main features

8-bit EEPROM-based RISC MCU

Program: 2k x 14; RAM: 128 x 8; Data: 256 x 8 6 / 8 / 10 / 14 / 16
pins

ADC: True 10-bit precision 7 timers,

4 independent PWMs + 1 enhanced capture/compare/PWM (with dead-time control)

2 analog comparators, 2 voltage regulator outputs

Low Standby, WDT and Operating Current

DUST, LVR, LVD

High ESD, High EFT

Low VDD operating voltage

Rev2.01

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**8bit CPU (EEPROM)**

- 37 RISC instructions:
- 16 MHz / 2T • Up to 16 pins
- 2T or 4T
- (VDD \geq 2.7)

- PWM (3 channels)

• Support SLEEP operation

Independent: period, duty cycle, polarity

Buzzer mode

Memory

- PROGRAM: 2k x 14 bit (read/write protection)
- DATA: 256 x 8 bit
- RAM: 128 x 8 bit • 8-layer hardware stack

Timers

- WDT (16-bit): 7-bit postscaler
- Timer0 (8-bit): 8-bit prescaler
- Timer1 (16-bit): 3-bit prescaler with gate
- Timer2 (8 bit): 4-bit prescaler and postscaler
- Timer3/4/5(12-bit): 7-bit prescaler and 8-bit postscaler

Operating Conditions (5V, 25°C)

- | | |
|---|---|
| • VDD (VPOR \geq 2.0V) | VPOR \geq 5.5 V |
| (auto-adjusted by POR, \geq 1.7V above 0°C) | • Operating temperature class 1 |
| temperature class 3 • Low Standby | $\geq -40 \text{ }^{\circ}\text{C} \text{ to } +125 \text{ }^{\circ}\text{C}$ |
| | $\geq 40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C}$ |
| | $\geq 40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}$ |
| | 0.7 μA |
| • WDT | 3.2 μA |
| • Normal mode (16 MHz) high | 207 $\mu\text{A}/\text{mips}$ |

Frequency division • Supports

operation in SLEEP • 1 or 2x {instruction clock, HIRC}, LP, T0CK,T1CK

I/O PORTS (Multiple 14 I/O)

- Pull-Up/Down Resistor
- All I/O Source Current: 30mA (5V, 25°C)
- All I/O Drain Current: 23mA (5V, 25°C)
- 8 I/Os: Interrupt/Wakeup

reliability

- 1 million erase cycles • > 20 years / 85°C storage • ESD > 4 kV, EFT > 5.5 kV
- (typical)
- (typical)

power management

- SLEEP
- LVR: 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1 • LVD: 2.0, 2.4, 2.8, 3.0, 3.6, 4.0
- (IN)
- (IN)

ADC (10bit) •

- True 10bit accuracy (\geq 1 MHz ADC clock) • 7 + 1 channel
- VADC \geq REF \geq Internal: 2.0, 3.0, VDD \geq External: VREF pin
- Special event trigger and interrupt

System Clock (SysClk) •

HIRC High Speed Internal Oscillator

\geq 16MHz $\leq \pm 1.5\%$ typical (2.5 \pm 5.5V, 25°C) \geq 1, 2, 4, 8, 16, 32, 64 divided • LIRC Low Power Low Speed Internal oscillator \geq 32 kHz or 256 kHz • EC external clock (I/O input) • LP / XT crystal input \geq Two-speed clock start (HIRC or LIRC) \geq Fail-safe clock monitor

Comparator (2 channels)

- 16-level programmable reference voltage

Regulator output (2 channels)

- It can output 32 voltages

PWM (Total 5)

- Enhanced Capture/Compare/PWM
 - \geq PWM Mode: Single PWM, Half-Bridge, Full-Bridge \geq 3
 - Pairs of PWM (6 I/Os): Complementary Output + Dead Time \geq Single Pulse Mode \geq Same Period, Duty Cycle \geq Polar Sex is optional

Integrated Development

- Environment (**IDE**) • On-Chip Debug (OCD), ISP • 3 Hardware Breakpoints
- Soft Reset, Halt, Single Step, Run, etc.

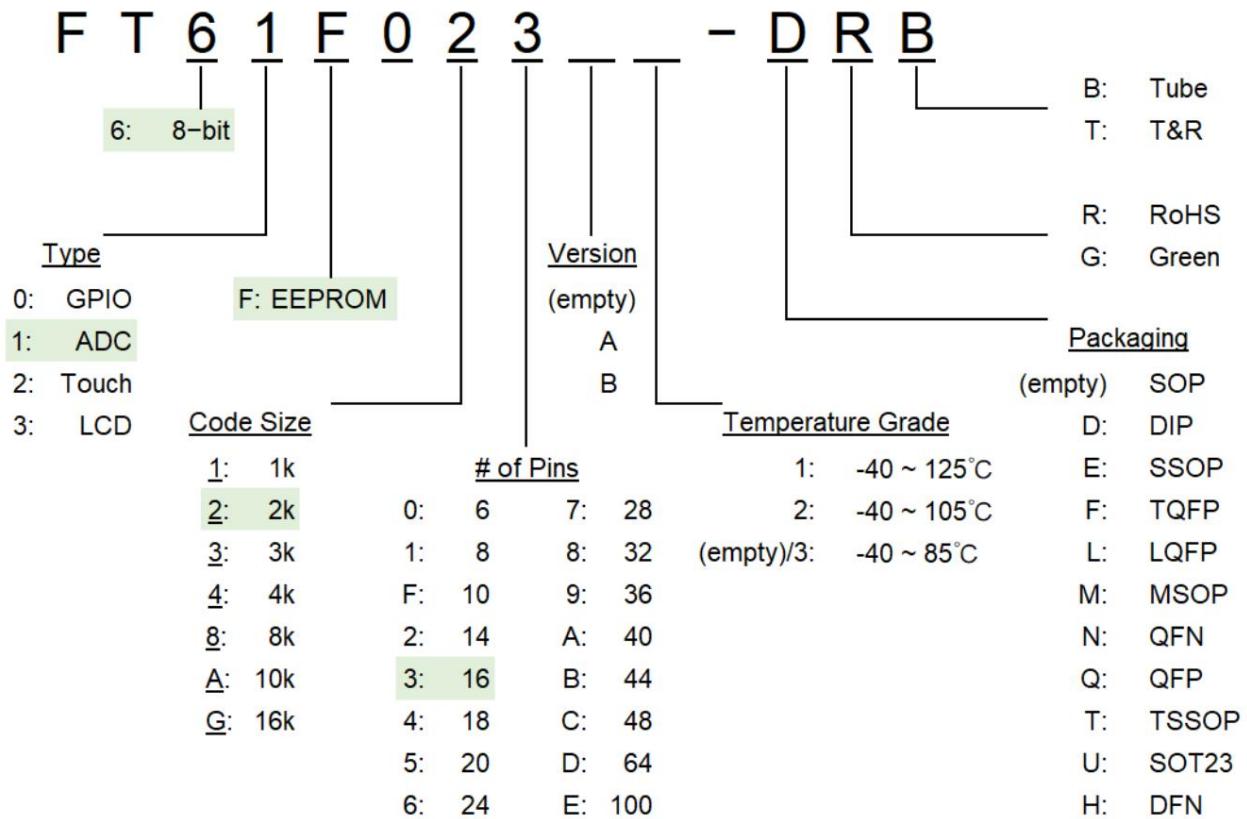
package

- SOT23-6 SOP8 DIP8 MSOP10
- SOP14 DIP14 SOP16 DIP16

Product Information and Selection Charts

| model | Number of I/Os | package |
|-------------------------------|----------------|---------|
| FT61F020 \bar{y} Uab _____ | 4 | SOT23-6 |
| FT61F021A-ab _____ | 6 | SOP8 |
| FT61F021A \bar{y} Dab _____ | | DIP8 |
| FT61F021B \bar{y} ab _____ | | SOP8 |
| FT61F021B \bar{y} Dab _____ | | DIP8 |
| FT61F02F \bar{y} Mab _____ | | MSOP-10 |
| FT61F02FA \bar{y} Mab _____ | | |
| FT61F022A \bar{y} ab _____ | 12 | SOP14 |
| FT61F022A \bar{y} Dab _____ | | DIP14 |
| FT61F022B \bar{y} ab _____ | | SOP14 |
| FT61F023 \bar{y} ab _____ | 14 | SOP16 |
| FT61F023 \bar{y} Dab _____ | | DIP16 |

Here a = R; RoHS b = B; Tube
= G; Green = T; T&R



MCU Product Ordering Information



Document modification history

| date | Version | describe |
|------------|---------|---|
| 2016-05-25 | 1.00 | First edition |
| 2021-11-26 | 2.00 | Fully optimized version (please ignore the first version) |
| 2022-06-10 | 2.01 | Updated Electrical Characteristics section |



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1. Block diagram and pins

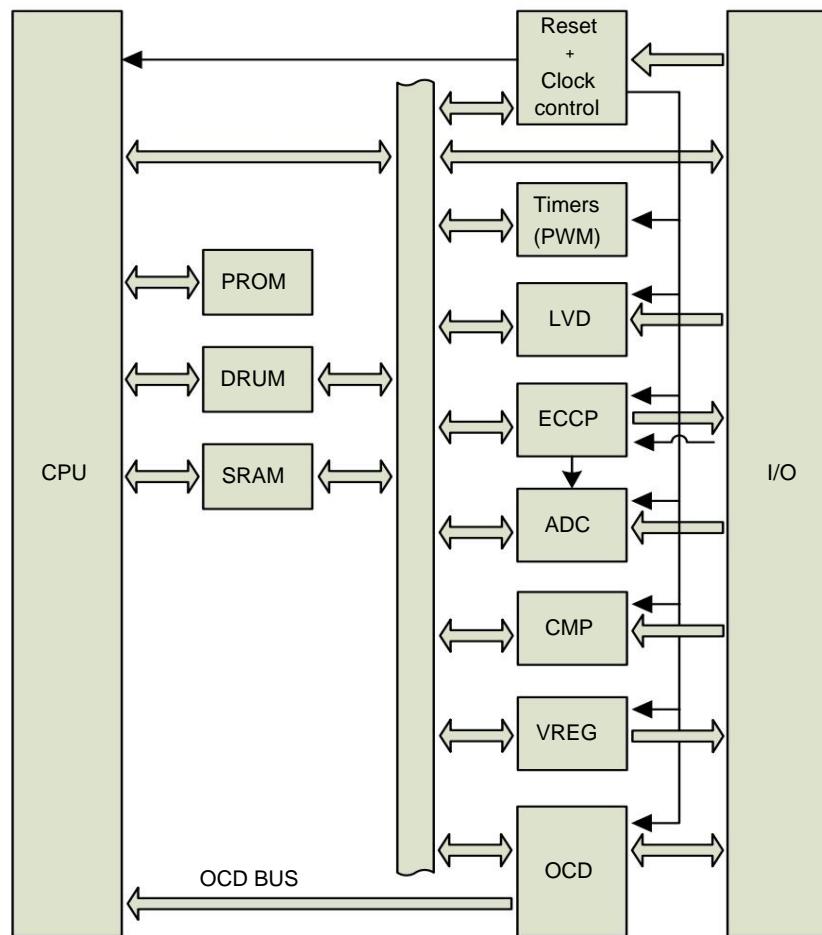


Figure 1-1 System structure block diagram

The list of standard abbreviations is as follows:

| abbreviation | describe |
|--------------|---|
| CPU | Central Processing Unit |
| SFR | Special Function Registers |
| SRAM | Static Random Access Memory |
| DRUM | Data EEPROM |
| PROM | Program EEPROM |
| Timers | WDT, Timer0, Timer1, Timer2, Timer3, Timer4, Timer5 |
| PWM | Pulse Width Modulator |
| ECCP | Enhanced Capture Compare and PWM |
| ADC | Analog to Digital Converter |
| CMP | Comparator |
| VREG | Voltage Regulator |
| LVD | Low Voltage Detect |
| OCD | On Chip Debug |
| I/O | Input / Output |

1.1 Pin Diagram



Figure 1-2 SOT23-6

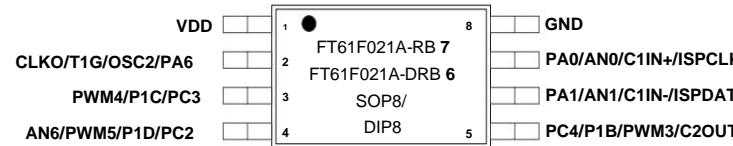


Figure 1-3 SOP8 / DIP8 (A)



Figure 1-4 SOP8 / DIP8 (B)

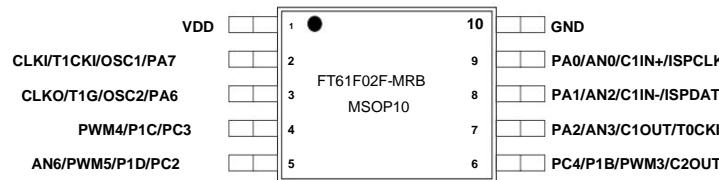


Figure 1-5 MSOP10 (A)

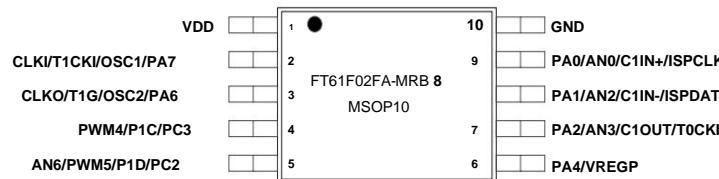


Figure 1-6 MSOP10 (B)

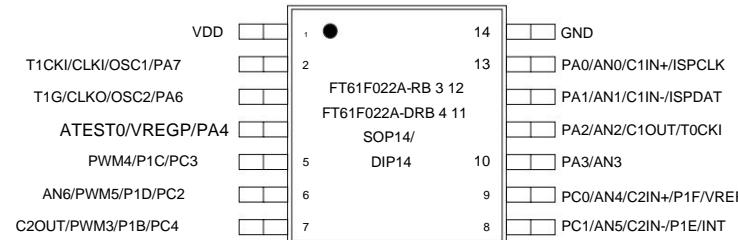


Figure 1-7 SOP14 / DIP14 (A)

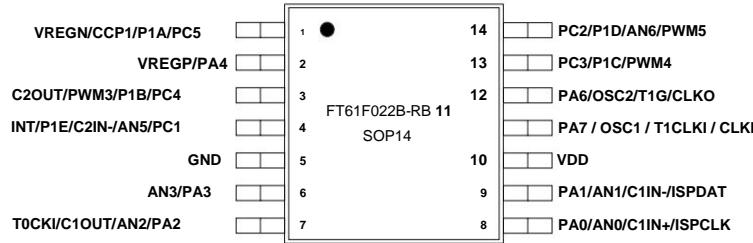


Figure 1-8 SOP14 (B)

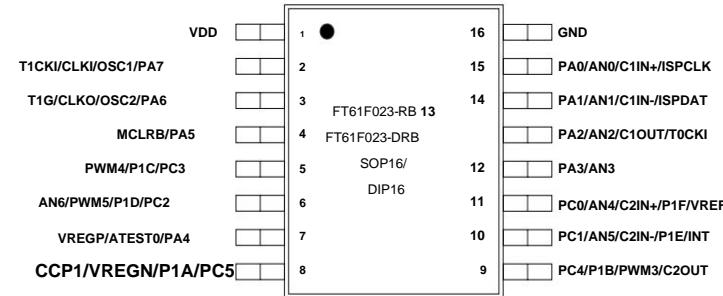


Figure 1-9 SOP16 / DIP16

1.2 Pin description---Classified by function

| Function | Description pin name | correspond GPIO | 6 pins | 8(A) pins | 8(B) pins | 10(A) pins | 10(B) pins | 14(A) pins | 14(B) pins | 16 pins |
|--------------------------------------|--|-----------------|--------|-----------|-----------|------------|------------|------------|------------|---------|
| power supply | VDD | | 5 | 1 | 1 | 1 | 1 | 1 | 10 | 1 |
| | GND | | 2 | 8 | 8 | 10 | 10 | 14 | 5 | 16 |
| GPIO | pull-up/pull-down, digital input, digital output | PC5 | | | | | | | 1 | 8 |
| | | PC4 | | 5 | | 6 | | 7 | 3 | 9 |
| | | PC3 | | 3 | 3 | 4 | 4 | 5 | 13 | 5 |
| | | PC2 | | 4 | 4 | 5 | 5 | 6 | 14 | 6 |
| | | PC1 | 3 | | 5 | | | 8 | 4 | 10 |
| | | PC0 | | | | | | 9 | | 11 |
| | | PA7 | | | | 2 | 2 | 2 | 11 | 2 |
| | | PA6 | 4 | 2 | 2 | 3 | 3 | 3 | 12 | 3 |
| | | PA5 | | | | | | | | 4 |
| | | PA4 | | | | | 6 | 4 | 2 | 7 |
| | | PA3 | | | | | | 10 | 6 | 12 |
| | | PA2 | | | | 7 | 7 | 11 | 7 | 13 |
| | | PA1 | 1 | 6 | 6 | 8 | 8 | 12 | 9 | 14 |
| | | PA0 | | 6 | 7 | 9 | 9 | 13 | 8 | 15 |
| clock | output | CLKO | PA6 | 4 | 2 | 2 | 3 | 3 | 12 | 3 |
| | Timer0 clock T0CKI | | PA2 | | | | 7 | 7 | 11 | 7 |
| | Timer1 clock T1CKI | | PA7 | | | | 2 | 2 | 2 | 11 |
| | OSC + | OSC1 | PA7 | | | | 2 | 2 | 2 | 11 |
| | OSC - | OSC2 | PA6 | 4 | 2 | 2 | 3 | 3 | 12 | 3 |
| Timer1 gate input | | T1G | PA6 | 4 | 2 | 2 | 3 | 3 | 12 | 3 |
| ISP debugging | ISP-Data | ISPDAT PA1 | | 1 | 6 | 6 | 8 | 8 | 12 | 9 |
| | ISP-CLK | ISPCLK PA0 | | 6 | 7 | 7 | 9 | 9 | 13 | 8 |
| External reset pull-up | | /MCLR PA5 | | | | | | | | 4 |
| PC1 edge interrupt | | INT | PC1 | 3 | | 5 | | | 8 | 4 |
| BRINGS port is changing broken | enter | PA7 | | | | | 2 | 2 | 2 | 11 |
| | | PA6 | | 4 | 2 | 2 | 3 | 3 | 3 | 12 |
| | | PA5 | | | | | | | | 4 |
| | | PA4 | | | | | | 6 | 4 | 2 |
| | | PA3 | | | | | | | 10 | 6 |
| | | PA2 | | | | | 7 | 7 | 11 | 7 |
| | | PA1 | 1 | 6 | 6 | 8 | 8 | 12 | 9 | 14 |
| | | PA0 | | | 7 | 7 | 9 | 9 | 13 | 8 |

| Function | Description pin name | | correspond GPIO | 6 pins | 8(A) pins | 8(B) pins | 10(A) pins | 10(B) pins | 14(A) pins | 14(B) pins | 16 pins |
|--|-------------------------------|----------------------|--------------------|-----------|--------------|--------------|---------------|---------------|---------------|---------------|------------|
| Stabilizer | High voltage output VREGP Low | | PA4 | | | | | 6 | 4 | 2 | 7 |
| | voltage output VREGN | | PC5 | | | | | | | 1 | 8 |
| ADC | enter | AN6 | PC2 | | 4 | 4 | 5 | 5 | 6 | 14 | 6 |
| | | AN5 | PC1 | 3 | | 5 | | | 8 | 4 | 10 |
| | | AN4 | PC0 | | | | | | 9 | | 11 |
| | | AN3 | PA3 | | | | | | 10 | 6 | 12 |
| | | AN2 | PA2 | | | | 7 | 7 | 11 | 7 | 13 |
| | | AN1 | PA1 | 1 | 6 | 6 | 8 | 8 | 12 | 9 | 14 |
| | | AN0 | PA0 | 6 | 7 | 7 | 9 | 9 | 13 | 8 | 15 |
| | VREF+ | VREF | PC0 | | | | | | 9 | | 11 |
| Comparators | enter | C1IN+ | PA0 | 6 | 7 | 7 | 9 | 9 | 13 | 8 | 15 |
| | | C1IN- | PA1 | 1 | 6 | 6 | 8 | 8 | 12 | 9 | 14 |
| | | C2IN+ | PC0 | | | | | | 9 | | 11 |
| | | C2IN- | PC1 | 3 | | 5 | | | 8 | 4 | 10 |
| | output | C1OUT PA2 | | | | | 7 | 7 | 11 | 7 | 13 |
| | | C2OUT PC4 | | | 5 | | 6 | | 7 | 3 | 9 |
| Enhanced capture/compare / PWM (ECCP) | PWM | Capture/Compare CCP1 | PC5 | | | | | | | 1 | 8 |
| | | P1A | PC5 | | | | | | | 1 | 8 |
| | | P1B | PC4 | | 5 | | 6 | | 7 | 3 | 9 |
| | | P1C | PC3 | | 3 | 3 | 4 | 4 | 5 | 13 | 5 |
| | | P1D | PC2 | | 4 | 4 | 5 | 5 | 6 | 14 | 6 |
| | | P1E | PC1 | 3 | | 5 | | | 8 | 4 | 10 |
| | | P1F | PC0 | | | | | | 9 | | 11 |
| PWM3 | | PWM3 PC4 | | | 5 | | 6 | | 7 | 3 | 9 |
| PWM4 | | PWM4 PC3 | | | 3 | 3 | 4 | 4 | 5 | 13 | 5 |
| PWM5 | | PWM5 PC2 | | | 4 | 4 | 5 | 5 | 6 | 14 | 6 |

Table 1-1 Pin descriptions by function

2. I/O terminal

According to different package types, FT61F02x series chips have up to 14 I/O pins, which are divided into 2 groups: PORTA (8) and PORTC (6). Table 2-1 lists the functions of all I/O pins.

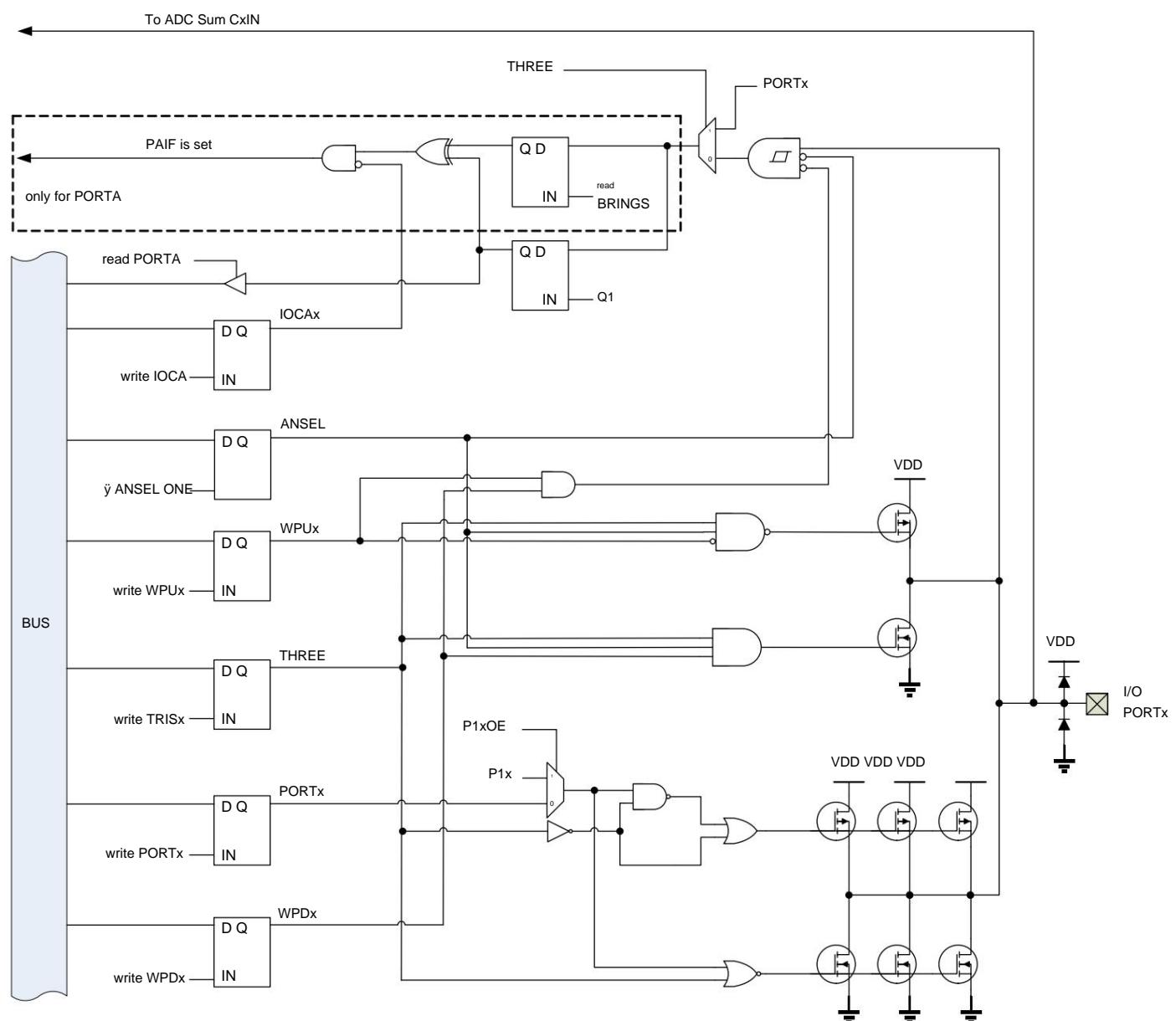


Figure 2-1 PORT port structure block diagram

The I/O pins all have the following functions (Table 2-3, Table 2-4):

- Digital output
- Weak pull-up
- Digital input
- Weak pull-down (PA4, PC1, PC2, PC3)



In addition, some I/Os have the following special functions:

a. Burn the debug pins (ISP-Data, ISP-CLK), which are connected inside the hardware and do not need to be set.

b. Functions selected through the IDE interface and loaded when the chip is initialized and configured ([Table 2-2](#)):

- External clock/crystal input (OSC1, OSC2)
- Internal clock output
- System external reset (/MCLRB)

c. Other functions of configuring corresponding I/O pins through instructions can be divided into 3 categories:

a. Digital output

- PWM3/4/5
- Enhanced PWM
- ECCP compare output

b. Digital input

- Timer0 clock input
- Timer1 clock input
- Timer1 gate input
- ECCP capture input
- External edge interrupt (INT)
- GPIO port change interrupt

c. Analog input

- LVD / BOR
- ADC
- VREF
- Comparator

d. Analog output

- Regulator VREG output

| pin name | ISP debugging | Clock | ADC | Regulator | Comparator | Interrupt | ECCP / PWM | Pull Up/Down | Numeric I/O | source current (mA) | sink current (mA) |
|----------|------------------|-----------------|----------|-----------|------------|---------------|---------------|--------------|-------------|------------------------|----------------------|
| PA0 | CLK | | AN0 | | C1IN+ | ÿ | | | ÿ / -- | 30 | 23 |
| PA1 DATA | A | | AN1 | | C1IN- | ÿ | | | ÿ / -- | 30 | 23 |
| PA2 | | T0CKI | AN2 | | C1OUT | ÿ | | | ÿ / -- | 30 | 23 |
| PA3 | | | AN3 | | | ÿ | | | ÿ / -- | 30 | 23 |
| PA4 | | | | VREGP | | ÿ | | | ÿ / ÿ | 30 | 23 |
| PA5 | | | | | | ÿ + /MCLRB | | | ÿ / -- | 30 | 23 |
| PA6 | | output /OSCÿ | | | | ÿ | | | ÿ / -- | 30 | 23 |
| PA7 | | T1CKI /OSC+ | | | | ÿ | | | ÿ / -- | 30 | 23 |
| PC0 | | | AN4 | | C2IN+ | | P1F | | ÿ / -- | 30 | 23 |
| PC1 | | | AN5 | | C2IN- | INT | P1E | | ÿ / ÿ | 30 | 23 |
| PC2 | | | AN6 | | | | PWM5 / P1D | ÿ / ÿ | | 30 | 23 |
| PC3 | | | | | | | PWM4 / P1C | ÿ / ÿ | | 30 | 23 |
| PC4 | | | | | C2OUT | | PWM3 / P1B | ÿ / -- | | 30 | 23 |
| PC5 | | | | WRECK | | | CCP1 / P1A | ÿ / -- | | 30 | 23 |
| Note | | T1G=PA6 | VREF=PC0 | | | | | | | VDD=5, VDS=0.5 | |

Table 2-1 I/O port functions

2.1 I/O port related register summary

| name | | default |
|--------------------|---|--------------|
| RDCTRL | Function When TRISx = 0, read the return value of the PORTx register • Input Latches • Output Latch | output latch |
| MCLRE External I/O | reset • LP: PA7 (+) | closure |
| DARK | and PA6 (ÿ) are connected to external low-speed crystal oscillator • XT: PA7 (+) and PA6 (ÿ) are connected to external high-speed crystal oscillator • EC: PA7 (+) is connected to external clock input, PA6 is I/O • INTOSC: PA6 outputs "instruction clock", PA7 is I/O • INTOSClO: PA7 and PA6 for I/O | INTOSClO |

Table 2-2 I/O related initialization configuration registers

| name | address | bit 7 | | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset value |
|--------|---------|-------------------------------------|--|----------|-------|-----------------------------|-------------------------|-------|-------|-------|-------------|
| ANSEL | 0x91 | ANSEL [7:0] | | | | | | | | | 1111 1111 |
| TRISA | 0x85 | TRISA[7:0], PORTA direction control | | | | | | | | | 1111 1111 |
| TRISC | 0x87 | | | | | | PORTC direction control | | | | ÿÿ11 1111 |
| PORTA | 0x05 | PORTA output register | | | | | | | | | xxxx xxxx |
| PORTC | 0x07 | | | | | PORTC output register | | | | | ÿÿxx xxxx |
| WPUA | 0x95 | PORTA weak pull-up | | | | | | | | | 1111 1111 |
| WPUC | 0x88 | | | | | PORTC weak pull-up | | | | | ÿÿ00 0000 |
| WPD | 0x89 | | | | | ÿ WPDA4 WPDC1 WPDC2 WPDC3 ÿ | | | | | ÿÿ00 000ÿ |
| JOKE | | 0x96 | IOCA[7:0]: PORTA port change interrupt setting | | | | | | | | 0000 0000 |
| OPTION | 0x81 | /PAPU | INTEDG T0CS | T0SE PSA | | | | PS2 | PS1 | PS0 | 1111 |

Table 2-3 Addresses and reset values of I/O-related user registers

| name | state | | Register address | reset value |
|-------------|---|-------------|------------------|-------------|
| TRISA PORTA | PORT port digital output (direction control) 1 = off 0 = enabled (pull-up/pull-down off) | TRISA[7:0] | 0x85 RW | 1111 1111 |
| TRISC PORTC | | | | |
| ANSEL | 1 = turn off pull-up/pull-down, and digital input (only for 8 ADC channels) 0 = (no action) | ANSEL[7:0] | 0x91 RW | 1111 1111 |
| /PAPU | 1 = Disable all PORTA pull-ups 0 = Pull-up is controlled by WPUA | OPTION[7] | 0x81 RW | 1 |
| WPUA PORTA | weak pull-up 1 = enabled (PORTA default) 0 = off (PORTC default) | WPUA[7:0] | 0x95 RW | 1111 1111 |
| WPUC PORTC | | WPUC[5:0] | 0x88 RW | 00 0000 |
| WPDA4 PORTA | weak pull-down 1 = enabled 0 = disabled | WPD[4] | 0x89 | RWÿ0 |
| WPDC PORTC | | WPD[3:1] | | RWÿ000 |
| DOOR DOOR | | PORT [7: 0] | 0x05 RW | xxxx xxxx |
| PORTC PORTC | data output register | PORTC[5:0] | 0x07 RW | xx xxxx |

Table 2-4 I/O related user registers

2.2 I/O configuration

For each PORT port, the following 4 modules need to be configured according to their corresponding functions (Table 2-5):

- Weak pull-up
- Weak pull-down (PA4, PC1, PC2, PC3)
- Digital input
- Digital output

| Function | Digital input pull-up/pull-down digital output | | set up |
|--------------------------------------|--|------------|---|
| ISP-DATA | On | Off | On (hardware built-in, ignore commands) |
| ISP-CLK | On | Off | Off (hardware built-in, ignore commands) |
| /MCLRB | On | pull up | Off (initialize configuration, ignore commands) |
| clock output | (ignore) | Off | On (initialize configuration, ignore commands) |
| OSC+ (EC) | On | (optional) | Off (initialize configuration, ignore commands) |
| OSC+ / OSC ⁻ (LP, XT) | Off | Off | Off (initialize configuration, ignore commands) |
| ADC | Off | Off | TRISx = 1; ANSELx = 1 |
| VREF | Off | Off | TRISx = 1; ANSELx = 1 |
| Comparator Input | Off | Off | TRISx = 1; ANSELx = 1 |
| Comparator Output | On | Off | THREEx = 0 |
| Timer0 clock | On | (optional) | THREEx = 1 |
| Timer1 clock | On | (optional) | THREEx = 1 |
| Timer1 gate | On | (optional) | THREEx = 1 |
| Timer3/4/5 Clock Port | On | (optional) | THREEx = 1 |
| Change Interrupt | On | (optional) | THREEx = 1 |
| PC1 ⁻ INT | On | (optional) | THREEx = 1 |
| digital input | On | (optional) | THREEx = 1 |
| PWM | On | Off | THREEx = 0 |
| ECCP capture | On | (optional) | THREEx = 1 |
| ECCP Compare/PWM Output On Regulator | | Off | THREEx = 0 |
| (Ignore) Digital Output | | Off | Off VREG_OE = 1 |
| | On | Off | THREEx = 0 |

Table 2-5 I/O Configuration Flags and User Registers

Note:

1. TRISx = 0: "Digital output" is enabled, "Pull-up/Pull-down" is automatically disabled (ignore WPD, WPUx), the TRIS bit has a higher priority than ANSELx⁻
2. TRISx = 1: "Digital Output" is off.
3. ANSELx = 1: "Pull-up", "Interrupt-on-Change", "Digital Input" auto-off (ignore WPD, WPUx).
4. The only instruction that can turn off the Digital Input is "ANSELx = 1".
5. "/PAPU = 1" disables "weak pull-ups" for all PAx ports. PCx has no such control bits.
6. /MCLR enable: the weak pull-up function of PA5 is automatically enabled (ignore WPUA[5]); read PORTA[5] as "0".
7. Write to the PORTx data output register, the I/O port will output the corresponding logic level. Data for up to 8 I/Os per group
 The registers share the same address, and the write operation actually performs the process of 'read-modify-write', that is, read the group of PORTx port latches first value (output or input), then modified, and then written back to the PORTx data register.
8. Digital output and digital input functions can coexist, and some applications need to enable digital output and digital input at the same time.
9. When TRISx = 0, the value of the PORTx output or input latch can be optionally read through the IDE interface.
10. On a full reset or system reset, the PORTx registers will not be reset, but TRISx will be reset to '1', turning off the output.
11. When the IO turns on the weak pull-up and weak pull-down at the same time, the weak pull-down will be disabled and the weak pull-up will work.

For PC1-INT and PORTA port change interrupt settings, see [Section 9 "Interrupts"](#).

3. Power-on reset (POR)

The power-up process, that is, the process in which VDD rises from below the Power-On-Reset voltage (VPOR) to above VPOR. When the CPU is powered back on, VDD may not have fully powered down to 0V.

1. When VDD is below VPOR, the CPU is in full reset state.

a. All calibration configuration registers are not reset. Except TMR0, PORTx, Z, HC, C, FSR, INDF, ADRESL,

The Special Function Registers (SFRs) other than ADRESH, TMRxL, TMRxH, CCPR1L, CCPR1H and SRAM (see [Section 17 "Special Function Registers"](#)) are all in reset. The registers that are not reset, such as SRAM, will keep their data until VDD drops to 0.6V (typ.), and when VDD is lower than 0.6V, its value is indeterminate.

b. Program Counter PC = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (top of stack).

2. When VDD rises above VPOR, the chip starts the initial configuration (BOOT) process.

3. After the initial configuration is complete, the instruction will execute from the PC = 0x00 address.

Typical VPOR is ~1.6V at room temperature (25°C), rising to ~1.9V at low temperature (-40°C). When VDD > VPOR, the CPU can work normally at a lower speed of 8 MHz / 2T, so the operating range of VDD is automatically adjusted with temperature. This feature is important for battery-powered systems, where in a typical battery operating environment, the CPU can still operate when the battery voltage is as low as 1.5V, thereby increasing battery life.

Note:

1. VPOR is not configurable.
2. The hardware circuit of POR is turned on by default. When the VDD voltage is lower than VPOR, the chip power reset is performed, not only when the power is turned on.
when executed.

3.1 Initialization Configuration Timing

| name | Function | default |
|---------|---|---------|
| PWRTEB | Power-on delay timer, additional delay ~64ms after initial configuration is completed | closure |
| CSUMENB | program space checksum verification function | closure |

Table 3-1 Initial configuration

The above two initialization configurations are set by the IDE interface and cannot be modified by commands. Initial configuration process:

1. CPU idle wait ~4ms;
2. Load the initialization configuration register value from non-volatile memory, the process ~24us. These register values are preset by the IDE, not affected by the order;
3. If the Power-On-Timer (PWRT) is enabled, the CPU will idle for an additional ~64ms;
4. If the checksum (Checksum, CSUM) is enabled, this function will accumulate and check the entire program space.
 - a. If the verification fails, the CPU will restart the initialization configuration process from idle waiting for ~4ms;
 - b. If the verification is successful and there are no other reset conditions, the CPU starts to execute the instruction;

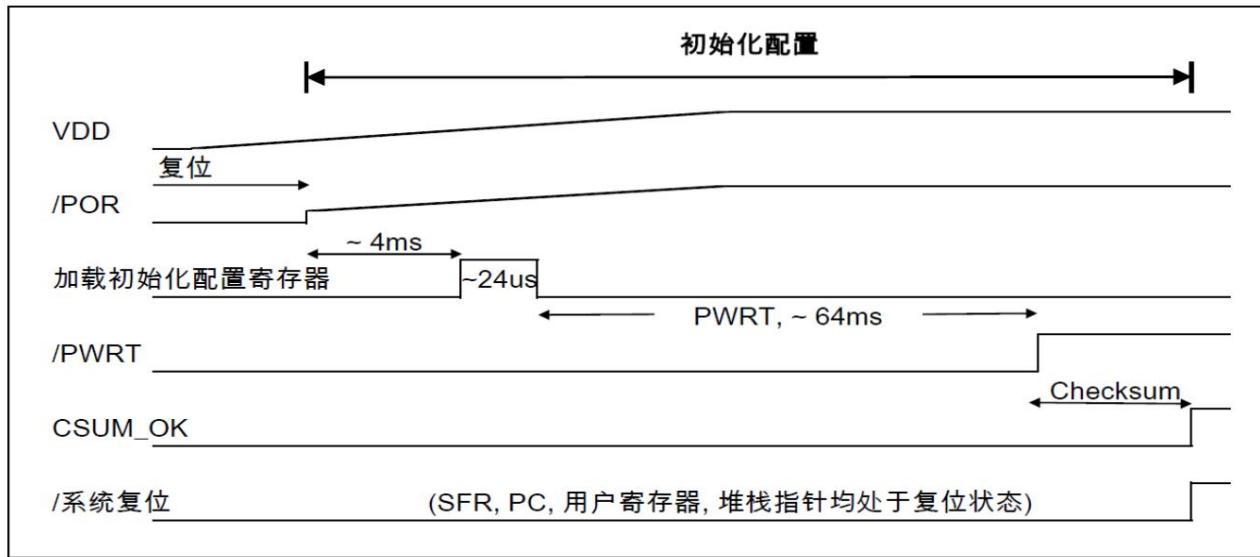


Figure 3-1 Power-on sequence (PWRT and Checksum enabled)

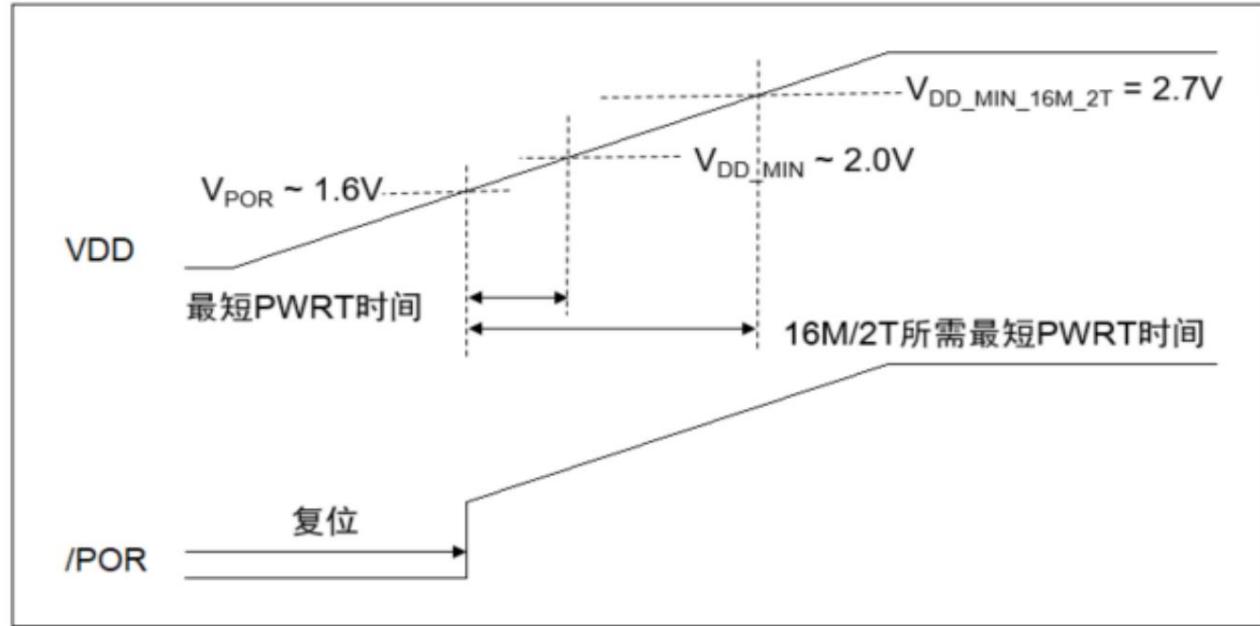


Figure 3-2 Minimum PWRT time required for power-on process

If the CPU needs to run at 16MHz / 2T, then VDD must be higher than 2.5V at the end of the initial configuration (BOOT). By enabling PWRT, the initial configuration time can be increased from ~4ms to ~68ms, thereby improving the settling time of the power system.

When running at 16MHz / 2T, the LVR should be enabled and VBOR ≥ 2.5V. In addition, the frequency of LVR enable can be controlled by command to monitor VDD from time to time instead of always enabling (refer to "LVREN", "SLVREN") to reduce power consumption.

Note:

1. The VDD power-on process should not be too slow, and it is not recommended that the VDD capacitor CVDD < 22 μF;
2. The VDD capacitor value is preferably 1 to 10μF. CVDD < 1μF may be too small for EFT performance ;
3. If the startup delay is acceptable, it is recommended to enable PWRT and CSUM to improve the stability of the CPU;

4. System reset

Unlike POR, a system reset is not a complete reset. Whether the CPU starts the initialization configuration process when the system is reset

It depends on the reset trigger type and settings. If the initialization configuration is started, wait for ~4ms idle, then reload the initialization configuration register

If the PWRT is enabled, an additional delay of ~64ms will occur, and then the system will start normally. During system reset:

- In addition to initializing the configuration registers, the registers that are reset during the POR process will also be reset when the system is reset;
- Program Counter PC = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (top of stack);

In addition to the OCD (On-Chip Debugger) module for simulation debugging, the four events that can trigger system reset are as follows:

1. Brown-out Reset (LVR / BOR) – always starts initial configuration;
2. Illegal instruction reset;
3. Watchdog Timer (WDT) – starts initial configuration if CPU is not in SLEEP state;
4. External I/O reset (/MCLRB);

Note: If a longer system restart time is acceptable, it is recommended to enable the initial configuration process (BOOT) to improve system stability.

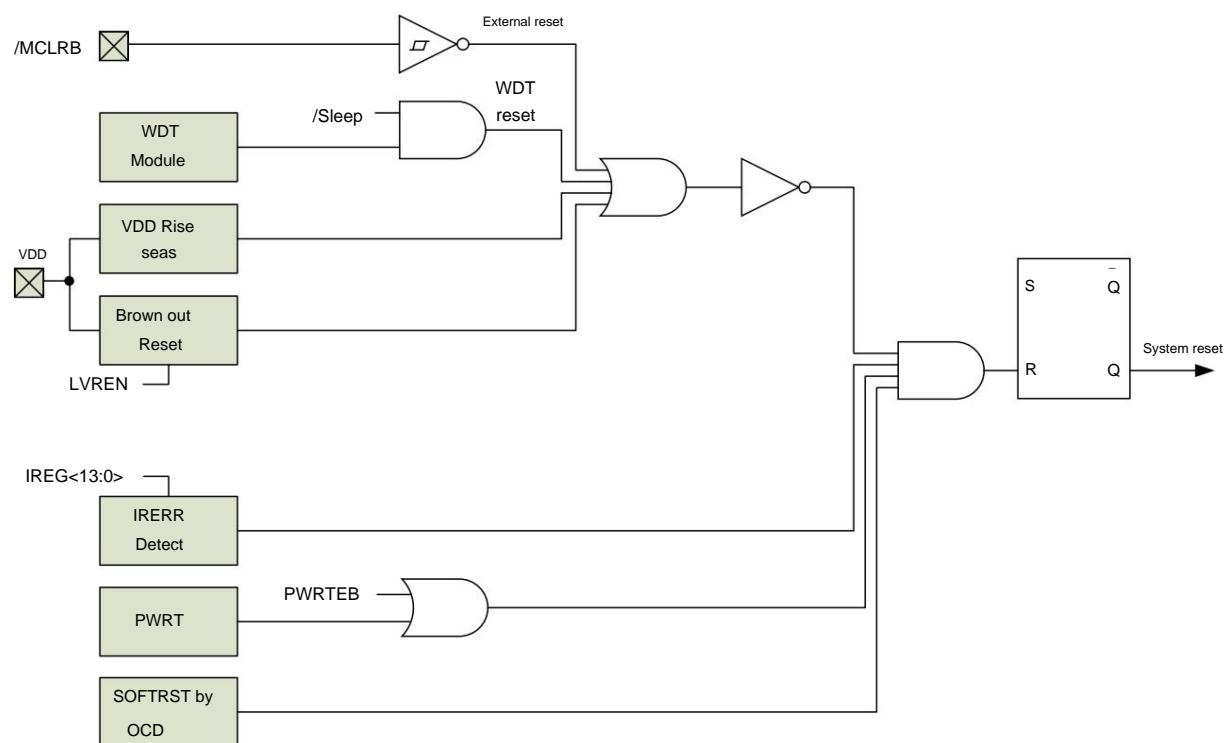


Figure 4-1 Block diagram of reset circuit structure

4.1 Summary of system reset related registers

Most of the system reset settings are configured from the IDE interface and cannot be modified by commands.

| name | Function | default |
|--------------------------|---|-------------------|
| LVRS | 7- level VBOR voltage (V): 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1 | 2.0 |
| LVREN | LVR •Enable •Disable •Enable in non- SLEEP mode •Control by instruction (SLVREN) | closure |
| WDTE | WDT •Enable (command cannot be disabled) •Controlled by command (SWDTEN) | SWDTEN control |
| MCLRE External I/O reset | | closure |

Table 4-1 Reset related initialization configuration registers

4.2 Brown-Out Reset (LVR / BOR)

A brown-out condition occurs when the VDD value decreases and falls below the preset brown-out value (VBOR) for more than the TBOR time. TBOR is approximately 3 to 4 LIRC clock cycles (~94 – 125µs, LIRC will automatically turn on if not pre-started). When $VDD < VBOR$, the CPU remains in system reset state until $VDD > VBOR$ when the CPU starts the initial configuration process (BOOT).

The VPOR value is not configurable, while the VBOR value can be set to 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1V (see "LVRS", Table 4-1).

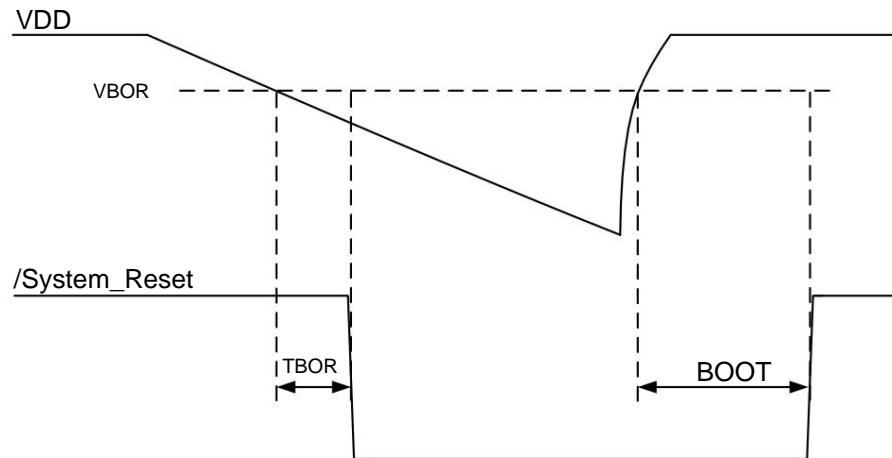


Figure 4-2 LVR initialization configuration sequence diagram

The LVR can be configured for 4 different functions (see "LVREN", Table 4-1).

1. LVR enable;

2. LVR is closed;
3. LVR is enabled in non-SLEEP mode;
4. Enable or disable LVR by command control (SLVREN, [Table 4-2](#)).

Note: In SLEEP mode, the LVR can be turned off by command to reduce power consumption. But if the system VDD is unstable, the CPU should wake up regularly and enable LVR to monitor VDD.

| name | Status | Register address | reset value | |
|--------|---|------------------|-------------|------|
| SLVREN | <u>only applies to LVREN Configured to control LVR by instruction SLVREN</u> 1 = LVR is enabled 0 = LVR is disabled _____ | MSCKCON[4] | 0x1B | RW-0 |

Table 4-2 LVR User Register

Note: This bit can be cleared by any other reset except BOR reset

4.3 Illegal Instruction Reset

There are many reasons for CPU fetching instruction error, the most common ones are interference and unstable VDD. A system reset will be generated when an illegal command occurs.

Although there is no dedicated reset instruction, any intentionally illegal instruction is equivalent to a reset instruction.

4.4 Watch Dog Timer (WDT) Reset

In SLEEP mode, WDT overflow will cause wake-up.

In normal mode (non-SLEEP mode), a WDT overflow will trigger a system reset and then initiate initial configuration. A WDT reset can be used to reset a hung CPU. The WDT should be cleared from time to time in the program to avoid false resets.

For details on WDT operation and settings, please refer to [Section 7.1 Watch Dog Timer \(WDT\)](#).

4.5 External I/O System Reset /MCLRB

The CPU can be reset by applying a low voltage on the /MCLRB (PA5) pin if the initialization configuration registers have been set accordingly.

WDT reset does not pull the /MCLRB pin low. The /MCLRB pin is usually weakly pulled up to VDD through a resistor, rather than directly connected to VDD, as shown in [Figure 4-3](#). It is recommended to use an external RC circuit to provide fault filtering and overcurrent protection.

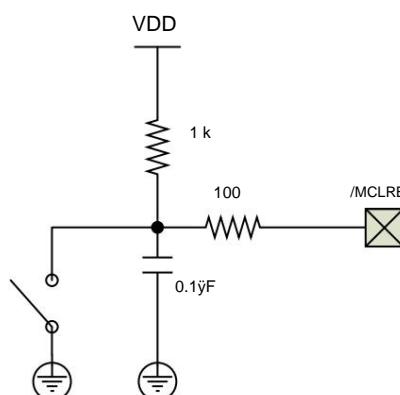


Figure 4-3 /MCLRB reset circuit

4.6 Detection of last reset type

Through different combinations of 4 status flag bits /POR, /BOR, Time Out (/TF), Power Down (/PF), the last system can be traced back.

type of system reset, except "/MCLR system reset in normal mode" and "Illegal instruction reset". These status flag bits are required by the pointer

Set to 1. After reset, the corresponding flag bit will be locked to "0".

| reset source | /BY | /THERE IS | /TF | /PF |
|--|---------|-----------|-------------------|-----------|
| | PCON[1] | PCON[0] | STATUS[4] | STATUS[3] |
| | 0x8E | | 0x03, 0x83, 0x103 | |
| BY | 0 | (unknown) | 1 | 1 |
| LVR | - | 0 | 1 | 1 |
| In normal mode (non-SLEEP) WDT overflow (reset) | - | - | 0 | - |
| WDT overflow (wake-up) in SLEEP mode | - | - | 0 | 0 |
| In SLEEP mode/MCLR reset In normal mode | - | - | 1 | 0 |
| (non-SLEEP)/MCLR reset Illegal instruction reset On-chip | y | - | - | - |
| debug (OCD) | - | - | - | - |
| | - | - | - | - |

Table 4-3 Reset related status flag bits ("y" no change)

5. Low Voltage Detection (LVD)

LVDs work similarly to LVRs, with the following exceptions:

- All control bits and parameter selection bits are set by user instructions, not when initializing configuration;
- LVD events will set LVDW instead of /BOR;
- The LVD input is VDD, which is compared with one of the 6-level LVDL voltage values (VLVD-REF) ;
- Debounce time (TLVD) is about 3 to 4 LIRC clock cycles (~94 - 125µs, LIRC will automatically turn on if not pre-started start);

5.1 Summary of LVD related registers

| name | state | Register address | reset value | |
|-------|---|------------------|-------------|--------|
| LVDEN | <u>LVD</u> 1 = enabled 0 = off 000 | PCON[3] | | RWÿ0 |
| LVDL | <u>VLVDÿREF</u> = reserved 001 = reserved 010 = 2.0 011 = 2.4 100 = 2.8 101 = 3.0 110 = 3.6 111 = 4.0 | PCON[6:4] | 0x8E | RWÿ000 |
| LVDW | <u>LVD trigger?</u> 1 = Yes (not latched) 0 = No | PCON[2] | | ROÿx |

Table 5-1 LVD User Settings and Flags Register

6. Oscillator and System Clock

System clock (SysClk) can be selected as internal high-speed oscillator HIRC, internal low-speed oscillator LIRC, or external oscillator by command (EC, LP, XT, see "SCS", Table 6-2). If an external oscillator is selected, then the initialization configuration register "FOSC" (Table 6-1) selects one of 3 external oscillators. The system clock can be further selected as a division of the internal oscillator by instructions (see IRCF, Table 6-2). The system clock is used to generate the instruction clock (Instruction Clock):

$$\text{Instruction Clock} = \text{SysClk} / N; N = 2 \text{ for } 2T, 4 \text{ for } 4T.$$

The external clock input and internal instruction clock output pins are set by the initialization configuration register (see FOSC).

The Timers and ADC modules have independent oscillators, so multiple oscillators can run simultaneously.

When Timers are enabled, their chosen oscillator is automatically turned on and remains active as long as the Timers are running. When the corresponding oscillator The ADC, Timers and PWM functions also work in SLEEP while keeping running in SLEEP mode.

In SLEEP mode, the instruction stops running, and the instruction clock will also stop, so the peripheral module that selects the instruction clock as the clock source will also Stop working in SLEEP mode.

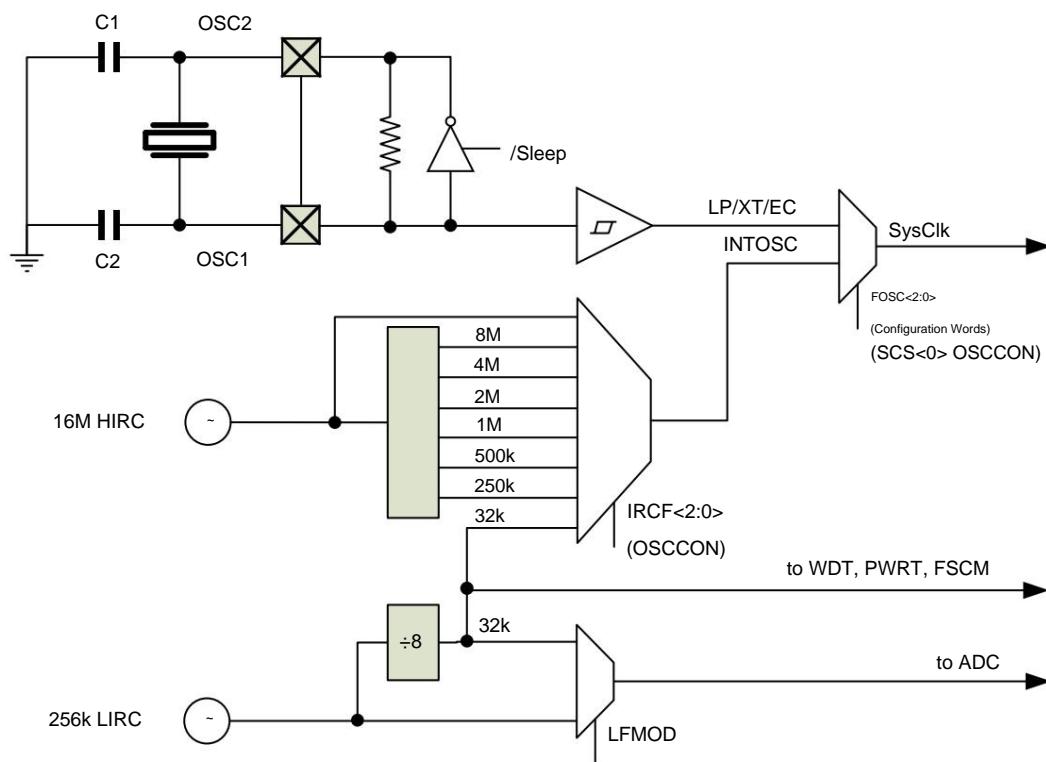


Figure 6-1 Clock source block diagram of system clock SysClk

6.1 Summary of Oscillator Module Related Registers

| name | Function | default |
|-------|---|----------|
| DARK | LP: PA7 (+) and PA6 (y) are connected to external low-speed crystal oscillator • XT: PA7 (+) and PA6 (y) are connected to external high-speed crystal oscillator • EC: PA7 (+) is connected to external clock input, PA6 is I/O • INTOSC: PA6 outputs "instruction clock", PA7 is I/O • INTOSCIO: PA7 and PA6 for I/O | INTOSCIO |
| IESO | XT/LP two-speed clock start • Enable • Closed | Enable |
| FCMEN | Fail-Safe Clock Monitor • Enable • Closed | Enable |
| TSEL | Correspondence between instruction clock and system clock (2T or 4T) • 2 (Instruction Clock = SysClk/2) • 4 (Instruction Clock = SysClk/4) | 2 |

Table 6-1 FOSC and Two-Speed Boot Initialization Configuration Registers

| SysClk system clock source | | configure | | | |
|----------------------------|-------|-----------|-------------|-----------|---------------|
| | | SCS | IRCF | LFMOD | OST |
| | | OSCCON[0] | OSCCON[3:4] | OSCCON[7] | (Fixed value) |
| | | 0x8F | | | |
| external | EC | RW-0 | RW-101 | RW-0 | 1,024 |
| | XT | 0 | - | - | |
| | LP | 0 | - | - | |
| internal | THERE | 16 MHz | 1 | 111 | - |
| | | 8 MHz | 1 | 110 | - |
| | | 4 MHz | 1 | 101 | - |
| | | 2 MHz | 1 | 100 | - |
| | | 1 MHz | 1 | 011 | - |
| | | 500 kHz | 1 | 010 | - |
| | | 250 kHz | 1 | 001 | - |
| | LIRC | 256 kHz 1 | 1 | 000 | 1 |
| | | 32 kHz 2 | 1 | 000 | 0 |

Table 6-2 SysClk system clock source setting related user registers

1 256 kHz LIRC for ADC use only (see ADCS and LFMOD, Table 12-2).

2 The system clock source (IRCF=000), PWRT, FSCM and WDT (WCKSRC=00) uniformly use LIRC divided by 8, that is, 32 kHz, regardless of the What is the value of LFMOD.

| name | Status | register | address | reset value |
|---------------|--|--------------|-------------------|-------------|
| OSTS | Oscillator Start Timeout Status Bit (Latched) | OSCCON[3] | 0x8F | ROÿx |
| | 1 = Running from external oscillator (startup successful) | | | |
| | 0 = Running from internal oscillator | | | |
| HTS | HIRC ready (latched) | OSCCON[2] | 0x8F | ROÿ0 |
| | 1 = Yes 0 = No | | | |
| LTS | LIRC ready (latched) | OSCCON[1] | 0x1B | ROÿ0 |
| | 1 = Yes 0 = No | | | |
| CKMAVG | 4 average measurement mode for LIRC and HIRC cross-calibration | MSCKCON[2] | 0x1B | RWÿ0 |
| | 1 = enable 0 = off | | | |
| CKCNTI | Enable cross-calibration of LIRC and HIRC | MSCKCON [1] | 0x1B | RWÿ0 |
| | 1 = start 0 = done (auto-cleared) | | | |
| SOSCPR Number | Number of HIRC cycles required to calibrate LIRC cycles | SOSCPR[11:0] | 0x1D[3:0] 0x1C | RWÿFFF |

Table 6-3 Oscillator Control/Status Bits

| name | State | | Register address | reset value |
|---------|--|--|------------------|-----------------------|
| GIE | global interrupt | 1 = Enable (PEIE, CKMEAIE, OSFIE applicable) | INTCON[7] | 0x0B 0x8B 0x10B |
| | | 0 = global shutdown (wake up is not affected) | | |
| | | | | |
| PEIE | general interrupt | 1 = Enabled (CKMEAIE, OSFIE applicable) 0 = off (no wakeup) | INTCON[6] | RWÿ0 |
| CKMEAIE | LIRC and HIRC cross calibration complete interrupt | 1 = enable 0 = off (no wakeup) | PIE1 [6] | |
| OSFIE | External oscillator failure broken | 1 = enable 0 = off (no wakeup) | PIE1 [2] | RWÿ0 |
| CKMEAIF | LIRC and HIRC cross calibration complete flag | 1 = Yes (latched) 0 = No | PIR1[6] | RWÿ0 |
| OSFIF | External oscillator failure indicator Shii | 1 = Yes (latched) 0 = No | PIR1[2] | |

Table 6-4 Oscillator Interrupt Enable/Status Bits

6.2 Internal Clock Modes (**HIRC** and **LIRC**)

The Internal high frequency clock (**HIRC**) is factory calibrated to 16 MHz @ 2.5V/25°C. of the chip

Frequency variation between typ. < ±2.0% @2.5 V/25°C and temperature variation typ. ±4.0% @40 °C/2.5V.

HIRC accuracy is calibrated during wafer test. The packaging process may cause HIRC frequency drift. The burner software can choose to HIRC to recalibrate.

The Internal low frequency clock (**LIRC**) is shipped uncalibrated and operates at 32 kHz. between chips

The frequency change is typically < ±10.5% @2.5 V/25°C, and the temperature change is typically < ±2.0% @40 °C/2.5V.

LIRC and **HIRC** can be cross-calibrated with each other – in one LIRC cycle, use Timer2 to measure the number of instruction clocks (SysClk select 16MHz HIRC), this is a built-in hardware function. Due to the low temperature coefficient of LIRC, when the temperature is unstable, it can be to calibrate the HIRC function to achieve the same ±2% temperature coefficient.

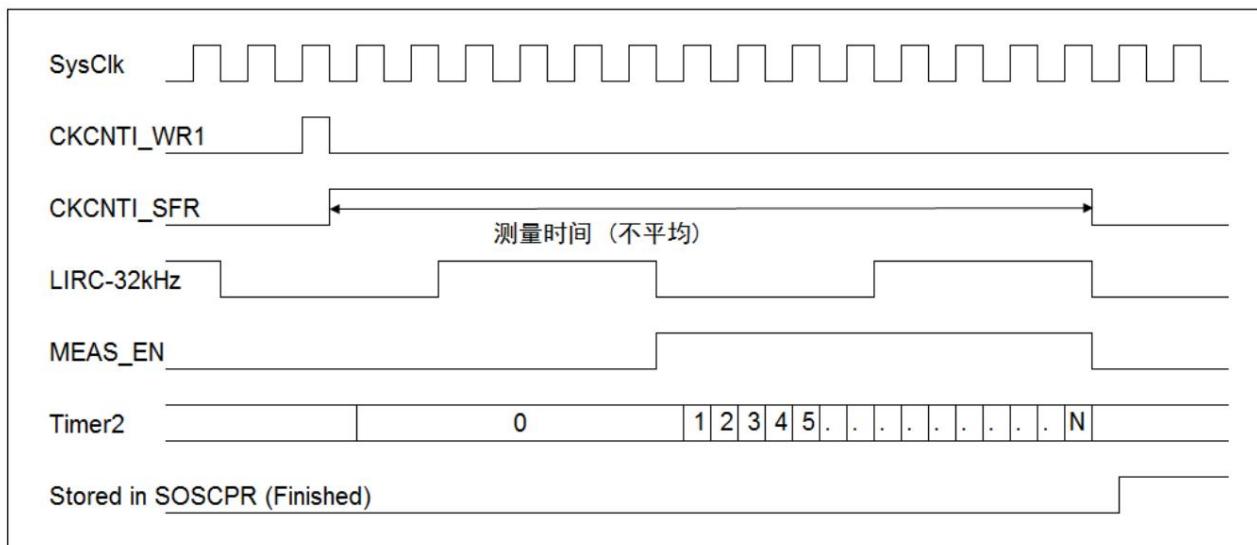


Figure 6-2 Timing diagram of single measurement

LIRC and HIRC cross-calibration steps:

1. Set IRCF = 111, SCS = 1 ; SysClk select 16MHz HIRC (other frequency settings will be less accurate)
2. Set CKMAVG = 1 ; Average of 4 measurements, choose 0 to mean no averaging
3. Set TMR2ON = 1 ; enable Timer2
4. Set CKCNTI = 1 ; Start calibration, default Timer2 prescaler = 1, postscaler = 1, T2CKSRC = SysClk for 2T; SysClk/2 for 4T
5. When calibration is completed, CKCNTI is automatically cleared ("CKCNTI =0"), and CKMEAIF is automatically set ("CKMEAIF = 1").
6. The measured value is stored in the SOSCPR register.
7. LIRC is 32kHz, if the CPU is running at 16MHz/2T, the ideal match value is 500.

Note:

- Do not write the SOSCPRH/L register when LIRC and HIRC are cross-calibrated;
- When LIRC and HIRC are cross-calibrated, Timer2 cannot be used by other peripherals;
- LIRC and HIRC cross-calibration functions are not compatible with the IDE's single-step debug mode;



6.3 External Clock Mode (EC/LP/XT)

6.3.1 EC Mode

An external digital signal is connected to the OSC1 pin as a clock source (OSC2 is used as I/O). When SysClk selects EC mode, EC mode requires no setup or transition time delay when POR resets or wakes up from sleep.

6.3.2 LP and XT modes

In LP or XT mode, a quartz crystal resonator or ceramic resonator is connected to the OSC1 and OSC2 pins as a clock source.

The **LP** oscillator mode has the lowest gain setting and current consumption among the 3 modes (EC, LP, XT). This mode is only used to drive a 32.768 kHz tuning fork crystal (clock crystal).

The **XT** oscillator mode selects the highest gain setting for the internal inverting amplifier.

If the clock source is selected in XT or LP mode, when the initial configuration is completed or wake-up from sleep, the CPU will suspend program execution while the Oscillator Start-up Timer (OST) is counting, which is beneficial to the stabilization of the XT or LP clock. For XT and LP modes, the OST counts 1,024 and 32,768 OSC1s (crystal input +ve terminal), respectively. For 32.768 kHz tuning fork crystals, OST timing requires at least 1 second.

Note:

- WDT will remain cleared until OST finishes counting; • Do not write to WDTCON or OPTION registers during OST counting, otherwise unpredictable behavior will occur;

Two-speed clock start (see "IESO", [Table 6-1](#)) allows the CPU to select the internal oscillator INTOSC mode as the SysClk then executes the instruction. In the case of frequent entering and exiting sleep mode, the dual-speed clock start-up function enables the chip to execute instructions immediately after waking up, thereby eliminating the start-up time required by the external oscillator to reduce the power consumption of the whole machine. That is, the CPU wakes up from sleep, executes a few instructions with INTOSC as SysClk, and then returns to sleep without waiting for the stabilization of the external oscillator.

Note: Two-speed start-up is disabled in EC mode as the oscillator does not require settling time.

Two-speed startup sequence:

1. The initial configuration is over or wake up from sleep;
2. Select INTOSC as the SysClk execution command until the OST times out;
3. SysClk remains low from the falling edge of INTOSC until the falling edge of the new clock (LP or XT mode);
4. SysClk switches to external clock source;

The Oscillator Start-up Timeout Status bit (OSTS) is used to indicate that SysClk is running from an external clock source or an internal clock source. When the two-speed clock start-up function is enabled, OSTS can indirectly query whether the oscillator start-up timer (OST) in LP or XT mode has timed out.

Executing a SLEEP instruction will abort the OST timing and OSTS will remain at '0'.

The Fail-Safe Clock Monitor (FSCM, enabled by "FCMEN", see [Table 6-1](#)) allows the chip to continue operating in the event of a failure of the external oscillator. The FSCM detects oscillator failure any time after the oscillator start-up timer (OST) expires.

FSCM is available in all external oscillator modes (EC, LP and XT). When an external oscillator is selected, it is recommended to enable the FSCM function.

An external oscillator is considered faulty if its oscillation frequency is ~1 kHz or less. The sampling clock is generated by dividing LIRC by 64.

There is a latch inside the fault monitor, the external clock sets the latch on each falling edge, and the sampling clock latches on each rising edge.

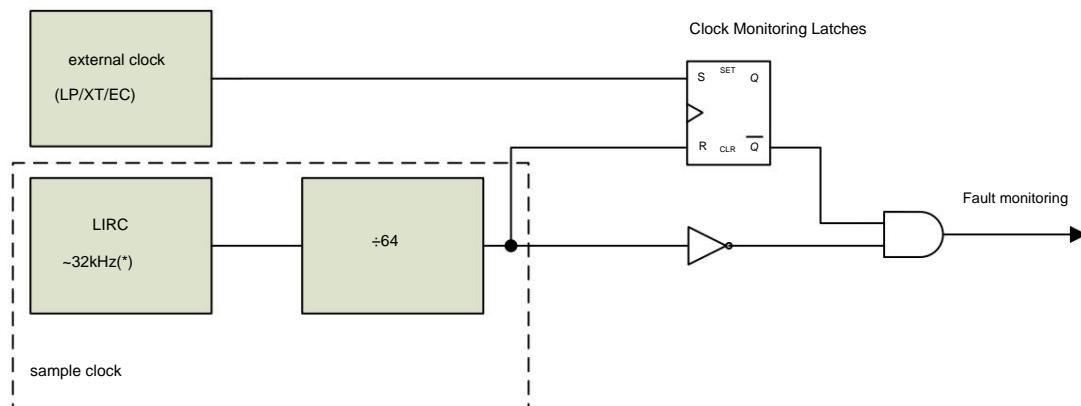
The register is cleared to 0. A fault is detected when the full half-cycle of the sample clock is complete and the master clock has not gone low.

When the external clock fails, the FSCM automatically switches SysClk to the internal clock source and sets OSFIF. If OSFIE is enabled,

Setting OSFIF to 1 will generate an interrupt. The chip firmware should then take steps to mitigate problems that may be caused by the faulty clock. SysClk will continue

It continues to run under the internal clock source until the chip firmware successfully restarts the external oscillator.

The internal clock source used by the "FSCM" is determined by "IRCF", which allows the internal oscillator to be configured before the external clock fails.



Note: LFMOD does not affect the sampling clock.

Figure 6-3 Block diagram of FSCM structure

The Fail-Safe condition will be cleared after a reset, executing a SLEEP instruction, or toggling the SCS bit. When the SCS bit is modified, the OST will reset the

Start the timer. During OST operation, the CPU selects INTOSC mode as SysClk to continue executing instructions. After the OST times out, the fail-safe

protection condition is cleared, the chip will switch back to the external clock source for operation. The fail-safe condition must be cleared before the OSFIF flag can be cleared bit.

Note: The SCS bits will not be updated by any automatic clock switching that may be initiated by the two-speed clock or by the fail-safe clock monitor.

Programs should monitor the OSTS bits to determine the current SysClk system clock source.

6.4 Internal switching of HIRC, LIRC and EC clocks

Figure 6-4 shows the timing diagram of internal clock switching. If the HIRC or LIRC is turned off before switching (to save power), there will be additional vibration

The oscillator sets the delay time, and the state of the corresponding oscillator can be queried through the HTS and LTS flag bits.

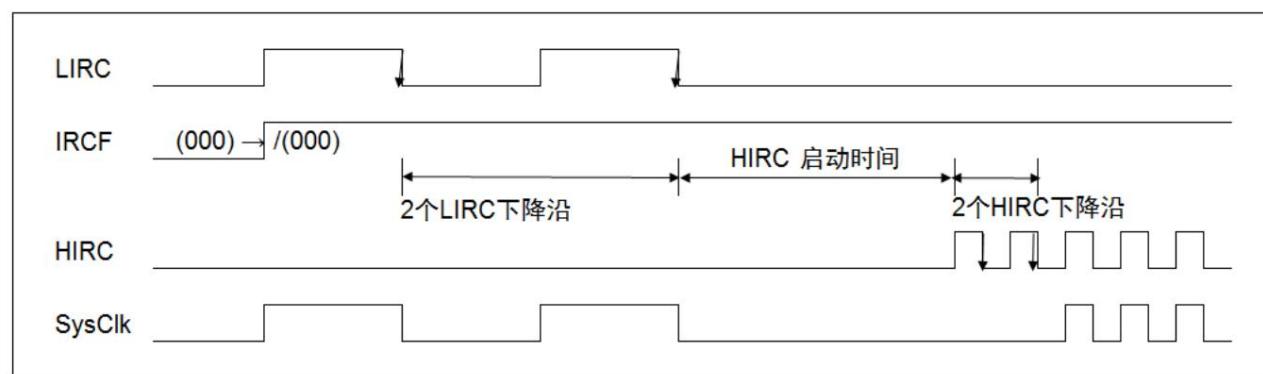


Figure 6-4 Sequence diagram of switching from LIRC to HIRC (the same principle applies to switching between EC, LIRC, HIRC)

7. Timer (TIMERS) and PWMx

There are 7 timers, including the watchdog timer (WDT).

| | WDT | Timer0 | Timer1 | Timer2 | Timer3/4/5 |
|---|--|---|---|---|---|
| Prescaler (bits) | - | 8 (together with WDT use) | 3 (1x, 2x, 4x, 8x) 4 (1x, 4x, 16x) | | 7 (1x, 2x, 4x, 8x, 16x, 32x, 64x, 128x) |
| counter (bit) | 16 | 8 | 16 | 8 | 12 |
| Postscaler (bit) 7 (shared with Timer0) | | - | - | 4 (1 ÷ 16x) | - |
| clock source | <ul style="list-style-type: none"> • LIRC | <ul style="list-style-type: none"> • Instruction clock • PA2/T0CKI (Transition edge count device) | <ul style="list-style-type: none"> • Instruction clock • LP • PA7/T1CKI (rising edge count device) | <ul style="list-style-type: none"> • 2x instruction clock • 2x HIRC | <ul style="list-style-type: none"> • THERE • 2x instruction clock • PA2/T0CKI (transition edge counter) • PA7/T1CKI (rising edge counter) |

Table 7-1 Timer resources

Note: If the clock source of the timer is not the instruction clock, set "TMRxON = 0" before changing TMRx.

When the timer is enabled, its selected clock source is automatically turned on. When the timer clock source selects the LP oscillator, the FOSC must be configured accordingly. Set to LP mode or select INTOSCIO mode, otherwise the LP oscillator will be off and no counts will be generated.

The postscaler of WDT and the prescaler of Timer0 share the same hardware frequency division circuit. The hardware circuit consists of Instruction selection is assigned to WDT or Timer0, but not both. A timer that is not assigned a divider has a divider ratio of "1" ÷

When a POR or system reset occurs, the counters, prescalers and postscalers of all timers except Timer0 will be reset.

bit. The following events will also reset the corresponding timer counters and dividers:

| | WDT | Timer0 | Timer1 | Timer2 | Timer3/4/5 |
|------------|---|---|---|---|--|
| prescaler | - | <ul style="list-style-type: none"> • Write TMR0 • PSA switch | <ul style="list-style-type: none"> • TMR1ON = 0 • Write TMR1L/H | <ul style="list-style-type: none"> • LIRC and HIRC Cross-calibration start • Write T2CON, TMR2L/H • Any reset action | <ul style="list-style-type: none"> • Write TMRxL/H |
| counter | <ul style="list-style-type: none"> • WDT, OST overflow • Enter/Exit SLEEP • CLRWDAT • Write to WDTCON | <ul style="list-style-type: none"> • Timer0 overflow • TMR1 = PR1 (match, special event trigger) • ECCP trigger feature special event | | <ul style="list-style-type: none"> • TMR2 = PR2 (match) | <ul style="list-style-type: none"> • TMRx = PRx (BUZZER mode match below) |
| postscaler | <ul style="list-style-type: none"> • Rejection WDTCON All of the above except piece • PSA switch | | | <ul style="list-style-type: none"> • Write T2CON, TMR2L/H • Any reset action | |

Table 7-2 Timer counter and divider reset events

7.1 Watch Dog Timer (WDT)

WDT is used to "wake up from SLEEP" or "generate system reset on CPU suspend". When the WDT counts to a preset number of clock cycles overflow occurs.

- In SLEEP mode, WDT overflow will trigger wake-up. The CPU will resume operation from where it was before entering SLEEP. wake up not in is not a system reset event.
- In normal mode (non-SLEEP mode), WDT overflow will trigger system reset, and then start initial configuration (refer to [Section 4 System Reset](#) bits).

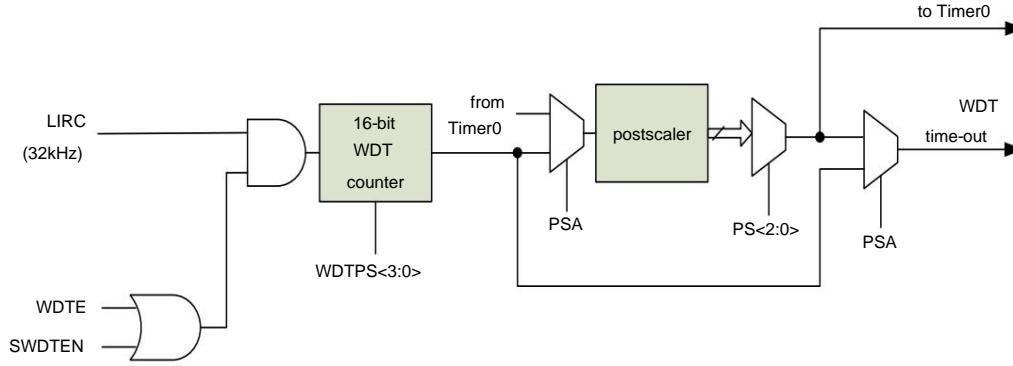


Figure 7-1 Block diagram of WDT structure

When the timer exceeds the watchdog timer time: $(\text{WDT-period} \times \text{WDT-postscaler}) / \text{WDT clock frequency}$, the WDT will overflow.

Due to the binary nature of the WDT postscaler, the watchdog timing time step is a continuous multiple. The maximum value that can be set before the WDT overflows Timing time is:

$$2^{16} \times 2^7 / 32\text{kHz} = \sim 262 \text{ seconds.}$$

7.1.1 Summary of WDT related registers

| name | state | | | | | Register address | reset value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|---|---------------------------------|---------|------------|--|------------------|-------------|---------------------------------|--|--|--|-----|--|---|--|---|--|-----|--|---|--|---|--|-----|--|---|--|---|--|-----|----------------|---|---------|----|--|-----|--|----|--|----|--|-----|--|----|--|----|--|-----|--|----|--|-----|--|-----|--|------------|--|------------|--|-----|----------|-------------------|--|---|--|-------------|------|---------------------|
| WDTPS | <u>WDT period</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0000 = 32 0001 = 64 0010 = 128 0011 = 256 0100 = 512 <u>(default)</u> 0101 = 1,024 0110 = 2,048 | | | | | WDTCON[4:1] | 0x18 | RW _y 0100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SWDTEN | 1 = WDT is enabled 0 = <u>WDT is off (when WDTE = 0)</u> | | | | | WDTCON[0] | | RW _y 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PSA | 1 = <u>The divider circuit is assigned to the WDT postscaler</u> 0 = The divider circuit is assigned to the Timer0 prescaler | | | | | OPTION[3] | | RW _y 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PS | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2"></th> <th colspan="3">WDT Postscaler Timer0 Prescaler</th> <th></th> </tr> <tr> <th>000</th> <th></th> <th>1</th> <th></th> <th>2</th> <th></th> </tr> </thead> <tbody> <tr> <td>001</td> <td></td> <td>2</td> <td></td> <td>4</td> <td></td> </tr> <tr> <td>010</td> <td></td> <td>4</td> <td></td> <td>8</td> <td></td> </tr> <tr> <td>011</td> <td><u>(PSA=1)</u></td> <td>8</td> <td>(PSA=0)</td> <td>16</td> <td></td> </tr> <tr> <td>100</td> <td></td> <td>16</td> <td></td> <td>32</td> <td></td> </tr> <tr> <td>101</td> <td></td> <td>32</td> <td></td> <td>64</td> <td></td> </tr> <tr> <td>110</td> <td></td> <td>64</td> <td></td> <td>128</td> <td></td> </tr> <tr> <td>111</td> <td></td> <td><u>128</u></td> <td></td> <td><u>256</u></td> <td></td> </tr> <tr> <td>xxx</td> <td>(PSA =0)</td> <td>1 <u>(PSA =1)</u></td> <td></td> <td>1</td> <td></td> </tr> </tbody> </table> | | | | | | | WDT Postscaler Timer0 Prescaler | | | | 000 | | 1 | | 2 | | 001 | | 2 | | 4 | | 010 | | 4 | | 8 | | 011 | <u>(PSA=1)</u> | 8 | (PSA=0) | 16 | | 100 | | 16 | | 32 | | 101 | | 32 | | 64 | | 110 | | 64 | | 128 | | 111 | | <u>128</u> | | <u>256</u> | | xxx | (PSA =0) | 1 <u>(PSA =1)</u> | | 1 | | OPTION[2:0] | 0x81 | RW _y 111 |
| | | WDT Postscaler Timer0 Prescaler | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | | 1 | | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | | 2 | | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | | 4 | | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | <u>(PSA=1)</u> | 8 | (PSA=0) | 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | | 16 | | 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | | 32 | | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 110 | | 64 | | 128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | | <u>128</u> | | <u>256</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| xxx | (PSA =0) | 1 <u>(PSA =1)</u> | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 7-3 WDT related user registers

| name | Function | default |
|------|---|----------------|
| WDTE | •Enable (command cannot be disabled) •Controlled by command (SWDTEN) | SWDTEN control |

Table 7-4 WDT option initialization configuration register

7.1.2 Setup and use of WDT

The WDT is enabled by WDTE (initialization configuration register) and SWDTEN (user register), and initialization occurs after WDT triggers a reset configuration process.

The WDT clock source is fixed at 32kHz LIRC, and the postscaler is set by WDTPS, PSA and PS together. When WDT is enabled, LIRC will automatically turn on and keep running in SLEEP mode.

To prevent the WDT from overflowing, the WDT must be cleared before the set timing. For details, please refer to the clearing of the WDT in [Table 7-2](#). pieces. Timing will restart after the WDT is cleared.

7.1.3 Switch the divider circuit between **Timer0** and **WDT**

The shared hardware divider circuit can be assigned to Timer0 or WDT, and the divider circuit may be changed when switching between Timer0 and WDT.

Cause the system to reset by mistake.

When switching the divider circuit from being assigned to Timer0 to the WDT, the following sequence of instructions must be followed:

```
BANKSEL TMR0 ; Can skip if already in TMR0 bank
CLRWDT ; Clear WDT
CLRR TMR0 ; Clear TMR0 and scaler
BANK SALE OPTION
BSR OPTION, PSA ; Select WDT
LDWI b'11111000' ; Mask scaler bits (PS2-0)
ANDWR OPTION, W
IORWI b'000000101' ; Set WDT scaler bits to 32 (or any value desired)
STR OPTION
```

When switching the divider circuit from being assigned to WDT to Timer0, the following sequence of instructions must be followed:

```
CLRWDT ; Clear WDT and scaler
BANK SALE OPTION
LDWI b'11110000' ; Mask TMR0 select and scaler bits (PSA, PS2-0)
ANDWR OPTION, W
IORWI b'00000011' ; Set Timer0 scale to 16 (or any value desired)
STR OPTION
```

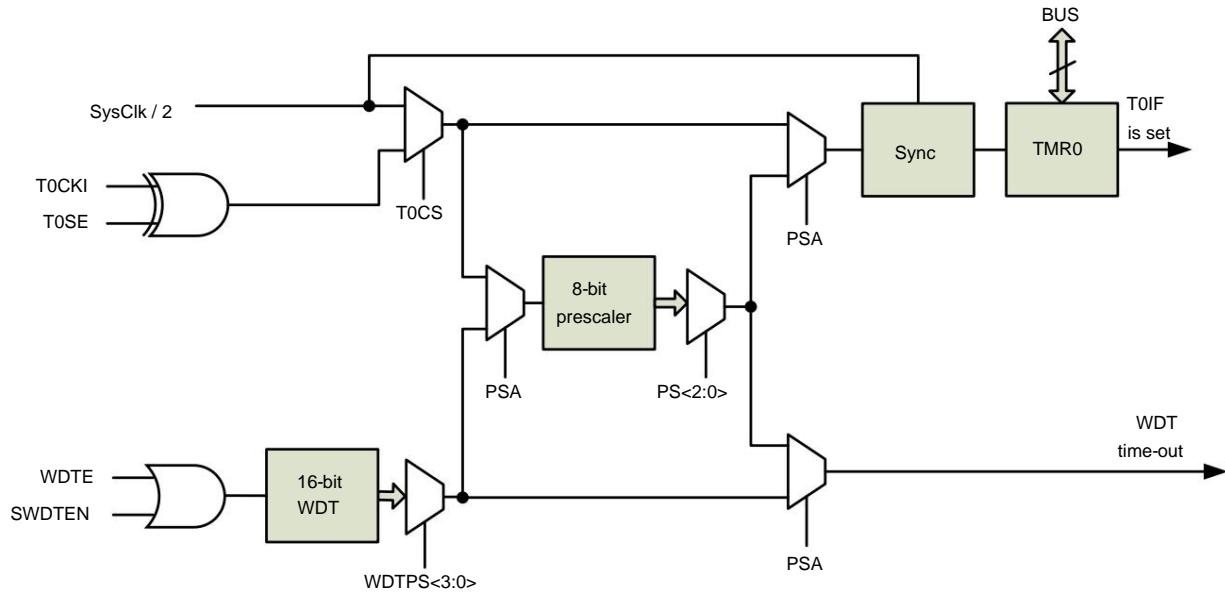
7.2 Timer 0 (TMR0)

Figure 7-2 Timer0 block diagram

Timer0 can be used as a rising/falling edge counter for I/O "PA2 \rightarrow T0CKI", or a timing timer (the clock source is the instruction clock).

$$\text{Timer0 count and time-out time} = \text{TMR0}[7:0] \times \text{Timer0_prescaler}$$

Timer0 overflow will set the interrupt flag bit (T0IF), whether the interrupt is triggered depends on the corresponding enable control bits (T0IE and GIE).

Note:

1. Within 2 instruction cycles after writing to TMR0, Timer0 stops incrementing;
2. In SLEEP mode, Timer0 will stop counting and maintain the count value before it enters sleep;
3. If Timer0 is used to count T0CKI, then T0CKI has a minimum period, high/low pulse width relative to Timer0 requirements. These constraints are usually met unless T0CKI is very fast and TT0CK is very slow;

| T0CKI | minimum | Unit | condition |
|----------------------|------------------------------------|----------------------|--|
| high/low pulse width | 0.5 * TT0CK + 20 | ns without prescaler | |
| | 10 | ns with prescaler | |
| cycle | The greater of 20 and (TT0CK+40)/N | ns | N = 1, 2, 4, ..., (no prescaler) N = 1 prescaler) |

4. For "Switching the divider circuit between Timer0 and WDT", please refer to [Section 7.1.3](#);

7.2.1 Summary of Timer0 Related Registers

| name | state | | | Register address | reset value |
|-------------|---|----------------|------------------|------------------|-------------------|
| T0CS | <u>Timer0 clock source</u> 1 = PA2/T0CKI (counter) 0 = instruction clock (timer) | | | OPTION[5] | RWý1 |
| T0SE | <u>Counter trigger edge</u> 1 = falling edge 0 = rising edge | | | OPTION[4] | |
| PSA | 1 = <u>divider circuit assigned to WDT postscaler</u> 0 = divider circuit assigned to Timer0 prescaler | | | OPTION[3] | |
| PS | | WDT postscaler | TIMERO prescaler | OPTION[2:0] | 0x81 RWý111 |
| | 000 | 1 | 2 | | |
| | 001 | 2 | 4 | | |
| | 010 | 4 | 8 | | |
| | 011 | (PSA=1) | 16 | | |
| | 100 | 16 | 32 | | |
| | 101 | 32 | 64 | | |
| | 110 | 64 | 128 | | |
| | 111 | 128 | 256 | | |
| xxx (PSA=0) | | 1 (PSA=1) | 1 | | |
| TMRO[7:0] | Timer0 count value | | | TMRO[7:0] | 0x01 RWýxxxx xxxx |

Table 7-5 Timer0 related user control registers

| name | state | | Register address | reset value |
|----------------------|--|--|------------------|-------------------------------|
| GIE global interrupt | 1 = Enabled (for TOIE) 0 = <u>global shutdown</u> (wakeup not affected) | | INTCON[7] | RWý0 0x0B 0x8B 0x10B |
| TOIE | Timer0 overflows interrupt control bit | | INTCON[5] | |
| TOIF | Timer0 overflows interrupt flag | | INTCON[2] | |

Table 7-6 Timer0 Interrupt Enable and Status Bits

7.3 Timer 1 (TIMER1)

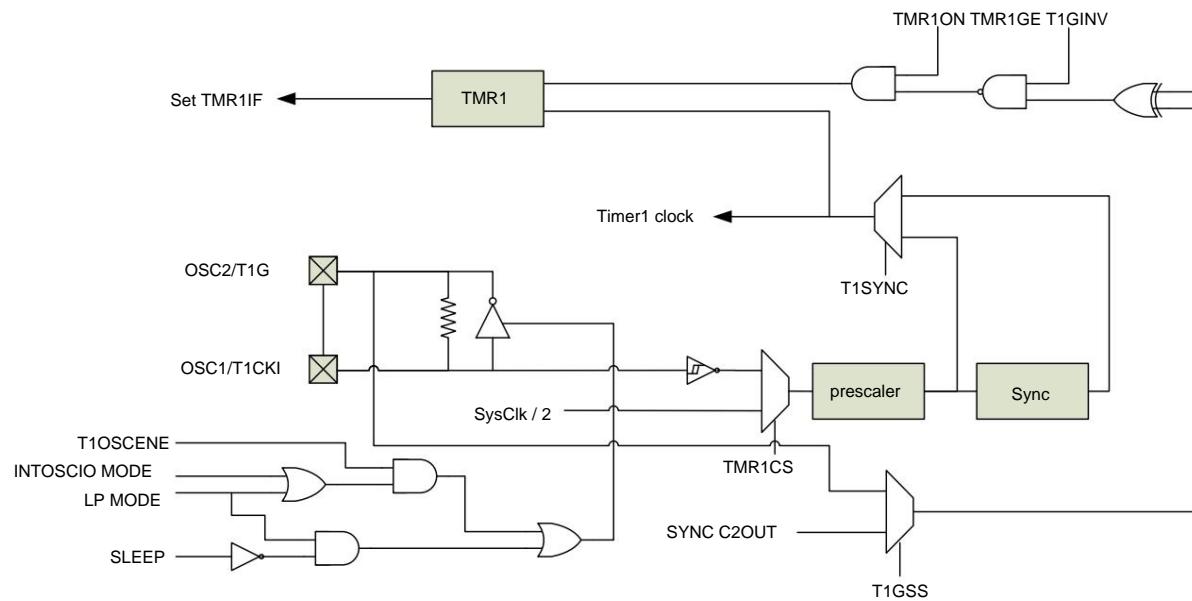


Figure 7-3 Timer1 block diagram

Timer1 can be used as a rising edge counter (synchronous or asynchronous) for I/O "PA7-T1CKI", or a timer for timing (the clock source is the instruction clock or LP oscillator), can also be used in gated mode (gate source is the T1G pin or the output of comparator C2), and as an ECCP capture/compare function enabled time base (see Section 10 Enhanced Capture/Compare/PWM).

Timer1 count and time-out time = TMR1

* Timer1_prescaler

Timer1 overflow will set the interrupt flag (TMR1IF), whether to trigger an interrupt and/or wake up from sleep depends on the corresponding enable control bit (GIE, PEIE and TMR1IE).

Note:

1. In counter mode, a falling edge must pass before the first rising edge is incremented. The applicable conditions are as follows:

- Enable Timer1 after POR reset
- Timer1 is turned off and then re-enabled
- Write TMR1H/TMR1L

2. To wake up from sleep, set "TMR1ON = 1", "T1SYNC = 1" and "TMR1CS = 1" to make Timer1 work

In asynchronous counter mode, it may be necessary to set "TMR1ON = 1", "T1SYNC = 1", "TMR1CS = 1" and "T1OSCEN = 1",

make Timer1 work in asynchronous timer mode and the clock source is LP oscillator, otherwise Timer1 will stop in SLEEP mode

Count, maintain the count value before it goes to sleep;

3. If Timer1 is used to count T1CKI, there is a minimum period, high/low pulse width for T1CKI relative to Timer1

requirements. These constraints are usually met unless T1CKI is very fast and TT1CK is very slow;

| T1CKI | Mode Min Sync | | unit | condition |
|----------------------|---------------|------------------------------------|------|---------------------------------|
| high/low pulse width | | (Tsysclk + 20) / N | ns | N = 1, 2, 4, 8 (with prescaler) |
| | asynchronous | 10 or 60 / N whichever is greater | | |
| cycle | Sync 2 | * (Tsysclk + 20) / N | ns | N = 1, 2, 4, 8 (with prescaler) |
| | asynchronous | 20 or 60 / N, whichever is greater | ns | |

7.3.1 Summary of Timer1 related registers

| name | State | | Register address | reset value |
|--------------------|---|--|------------------|----------------------------|
| T1GINV | gate toggle bit (the gate active level when Timer1 counts) 1 = high level 0 = low level | | T1CON[7] | RW yo 0 |
| TMR1GE | Gated mode (valid when TMR1ON = 1) 1 = Gating enabled (Timer1 only turns on when gate is active) 0 = gate off (Timer1 on) | | T1CON[6] | RW yo 0 |
| T1CKPS | Timer1 prescaler 00 = 1 01 = 2 10 = 4 11 = 8 | | T1CON[5:4] | RW yo 00 |
| T1OSCENE | Timer1 external clock source LP oscillator 1 = enable (*) 0 = off (*) FOSC should be configured in LP mode or INTOSCIO should be selected accordingly mode, and TMR1CS = 1, otherwise the oscillator will not run Row. | | T1CON[3] | 0x10 RW-0 |
| T1SYNC 3 | Timer1 external clock input is synchronized with the internal system clock 1 = Asynchronous 0 = Sync Note: This bit is valid when TMR1CS = 1 | | T1CON[2] | RW-0 |
| TMR1CS | Timer1 clock source 1 = External PA7/T1CKI (rising edge) or LP oscillator 0 = Internal instruction clock | | T1CON[1] | RW-0 |
| TMR1ON Timer1 | 1 = enable 0 = off | | T1CON[0] | RW-0 |
| T1GSS gated source | 1 = T1G pin (configured as digital input) 0 = output of comparator C2 | | CMCON1[1] | RW-1 |
| C2SYNC | Comparator C2 output synchronization control 1 = Output is synchronized to falling edge of Timer1 clock 0 = Asynchronous output | | CMCON1[0] | 0x1A RW yo 0 |
| TMR1L | TMR1 count result register lower 8 bits | | TMR1L[7:0] 0x0E | RW yo 0000 |
| TMR1H | TMR1 count result register upper 8 bits | | TMR1H[7:0]xF | 0000 |

Table 7-7 Timer1 related user control registers

3. One increment may be missed when switching from synchronous to asynchronous operation, and one more increment may be generated when switching from asynchronous to synchronous operation.

| name | state | Register address | reset value | |
|--|--|--|-----------------------|----------------------|
| GIE global interrupt | 1 = enabled (for PEIE, TMR1IE) 0 = <u>global shutdown</u> (wake up is not affected) | INTCON[7] | 0x0B 0x8B 0x10B | |
| PEIE peripheral general interrupt | 1 = Enabled (TMR1IE applies) 0 = off (<u>no wakeup</u>) | INTCON[6] | RW ₀ | |
| TMR1IE Timer1 and PR1 overflow interrupt | 1 = enable 0 = off (<u>no wakeup</u>) | PIE1 [0] | 0x8C RW ₀ | |
| TMR1IF | Timer1 and PR1 overflow interrupt flag bit | 1 = overflow (latch) 0 = <u>no overflow</u> | PIR1[0] | 0x0C RW ₀ |

Table 7-8 Timer1 Interrupt Enable and Status Bits

7.3.2 Read/Write Operation of Timer1 Register

TMR1H and TMR1L cannot be read or written at the same time and must follow the following read and write order:

- When reading TMR1, in order to avoid possible overflow between two read operations, set "TMR1ON = 0" to stop counting, then Read TMR1L and TMR1H.
- When writing to TMR1, in order to avoid the competition between the write operation and the count, set "TMR1ON = 0" to stop the count before the write operation. number, then write to TMR1L and TMR1H.

In addition, when Timer1 works in asynchronous mode, the read operation of TMR1H or TMR1L will be guaranteed to be valid (implemented by hardware).

7.3.3 Timer1 Gate Mode

The Timer1 gate function can time external events directly through the T1G pin, or analog events through the output of comparator C2 (see

See "T1GSS", Table 7-7), the gate can be configured to be active high or low (see "T1GINV", Table 7-7). This feature simplifies

Programs for delta-sigma A/D converters and many other applications.

Note:

1. When Timer1 clock source selects external LP oscillator, gate control source select T1G pin is invalid;
2. When the Timer1 gate source is selected as the output of Comparator C2 (T1GSS = 0), it is recommended to configure the output of Comparator C2 to Timer1 synchronization (C2SYNC = 1) to ensure that Timer1 does not miss an increment when the comparator output changes;

7.4 Timer 2 (TIMER2)

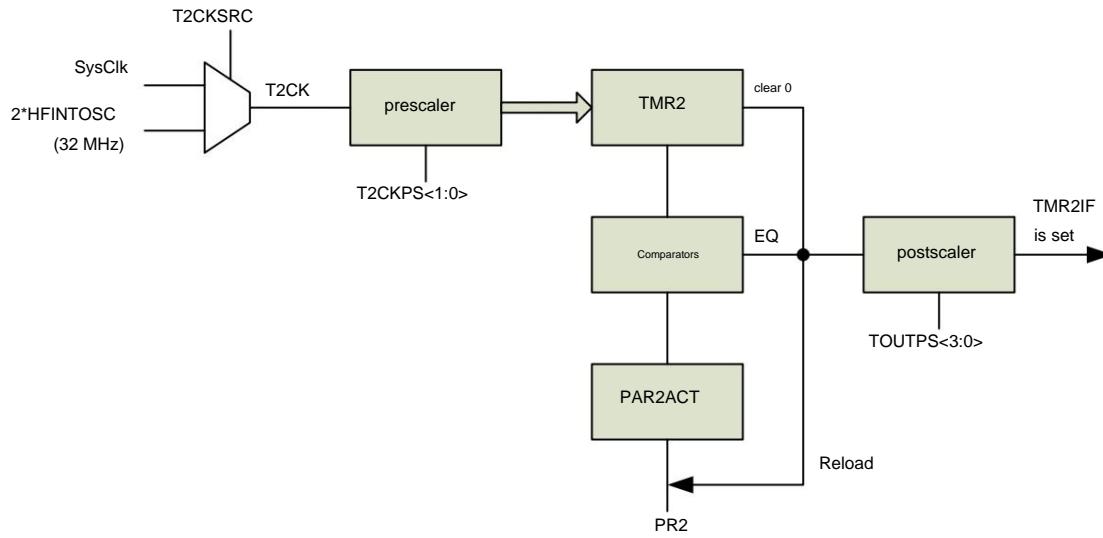


Figure 7-4 Timer2 block diagram

Timer2 is a timer that can also be used to generate enhanced PWM (no postscaler, see Section 10 Enhanced Capture/Compare/PWM), or use Cross-calibrate counts between LIRC and HIRC (CKCNTI=1). The count match and postscaler overflow functions can be used simultaneously.

The Timer2 clock is fed into the Timer2 prescaler (1, 4 or 16) and the output of the prescaler is used to increment the TMR2 register device, TMR2 is incremented from 0x00 until it matches PR2. When matching:

1. TMR2 is reset to 0x00 on the next increment cycle;
2. The Timer2 postscaler increments;
3. Timer2 overflows when the incremented output value of the Timer2 postscaler is equal to the postscaler setting value (1, 2 15 or 16);
4. The interrupt flag bit TMR2IF is set to 1, and whether the interrupt is triggered depends on the corresponding enable control bits (GIE, PEIE and TMR2IE);

Note:

1. Writing to T2CON does not clear the TMR2 register.
2. Both TMR2 and PR2 are read/write registers. On reset, their values are 0x0000 and 0xFFFF, respectively.
3. In SLEEP mode, Timer2 will stop counting and maintain the count value before it goes to sleep.

7.4.1 Summary of Timer2 related registers

| name | state | | | | Register address | reset value |
|----------------------------|--|-----------------------------|-----------|------------|------------------|---------------------------|
| TOUTPS | <u>Timer2 postscaler</u> | | | | T2CON[6:3] | RW _Y 0000 |
| | 0000 = 1 | 0100 = 5 | 1000 = 9 | 1100 = 13 | | |
| | 0001 = 2 | 0101 = 6 | 1001 = 10 | 1101 = 14 | | |
| | 0010 = 3 | 0110 = 7 | 1010 = 11 | 1110 = 15 | | |
| TMR2ON Timer2 | | 1 = enable 0 = off | | T2CON[2] | 0x12 | RW _Y 0 |
| | | 00 = 1 01 = 4 1x = 16 | | T2CON[1:0] | | RW _Y 00 |
| <u>Timer2 clock source</u> | | | | | | |
| T2CKSRC | 1 = 2 x HIRC (ie 32MHz, ECCP mode only) 0 = 2 x instruction clock | | | | MSCKCON[5] 0x1B | RW _Y 0 |
| TMR2 | TMR2 count result register | | | TMR2[7:0] | 0x11 | RW _Y 0000 0000 |
| PR2 | PR2 Period Register | | | PR2[7:0] | 0x92 | RW _Y 1111 1111 |

Table 7-9 Timer2 related user control registers

| name | state | | Register address | reset value |
|-----------------|---|---|------------------|-------------------|
| GIE | global interrupt | 1 = enable (for PEIE, TMR2IE) 0 = <u>global shutdown</u> (wake up is not affected) | INTCON[7] | RW _Y 0 |
| PEIE peripheral | general interrupt | 1 = Enabled (TMR2IE applies) 0 = off (<u>no wakeup</u>) | | |
| TMR2IE | Timer2 matches PR2 <small>broken</small> | 1 = enable 0 = off (<u>no wakeup</u>) | PIE1 [1] | 0x8C |
| TMR2IF | Timer2 matches PR2 break flag | 1 = match (latch) 0 = no match | PIR1[1] | 0x0C |

Table 7-10 Timer2 Interrupt Enable and Status Bits

7.5 Timer 3/4/5 (TIMER3/4/5) and PWM3/4/5

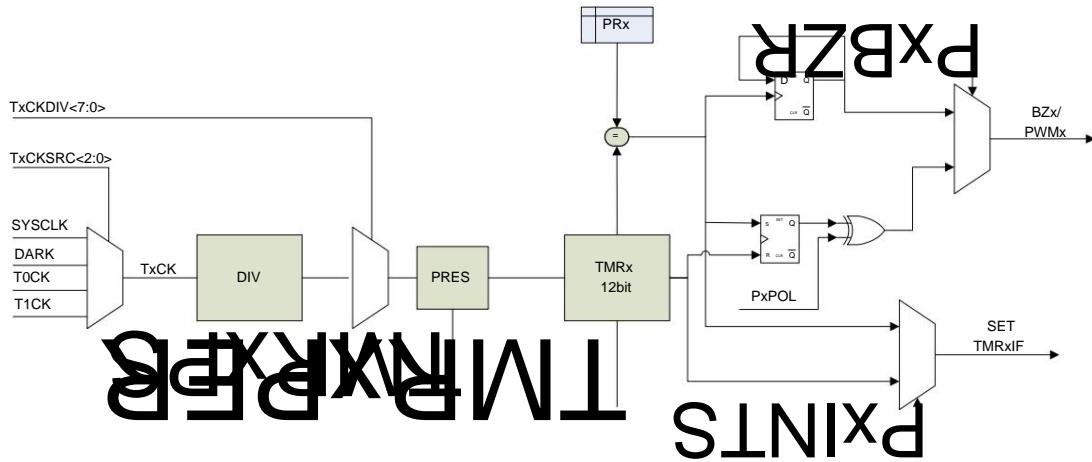


Figure 7-5 Timerx/PWMx (x = 3, 4, 5) block diagram

Timer3/4/5 can be used as I/O "PA2-T0CKI" or "PA7-T1CKI" counter, or timing timer, and can also be used to generate 3-way PWMx with independent duty ratios and selectable output polarity.

The Timerx/PWMx clock source is selected by PxCKSRC, and the clock source can be divided by 1~256 (refer to "TxCKDIV").

The Timerx clock is fed into a 7-bit prescaler (prescaler is 1~128), and the output of the prescaler is used to increment the TMRx register.

The Timerx module can be configured as an interrupt on overflow or a match (see "PxINTS").

Overflow Mode: Count and Timeout Time = $TMRx[11:0]$ prescaler , the valid bit of TMRx is determined by PxPER;
match mode: $TMRx$ increments to set time = PRx match; $TMRx$ prescaler / (Do not fear clock divider), $TMRx$ matches PRx

When Timerx overflows or TMRx matches PRx, the interrupt flag bit (TMRxF) is set, and TMRx resets on the next increment cycle.

Bit is 0x000. Whether an overflow or match event triggers an interrupt and/or wake-up from sleep depends on the corresponding enable control bits (TMRxE, PEIE and GIE).

Note:

1. When the Timerx/PWMx clock source selects HIRC, the internal HIRC will be turned on automatically unless it enters sleep mode;
2. Both TMRx and PRx are read/write registers. When reset, the value of PRx is 0xFFFF, but the value of TMRx is indeterminate and needs to be cleared by software first
Or write other initial values.
3. To wake up from sleep, set "PxCKSRC = 010 / 011", select Timerx clock source as I/O "PA2-T0CKI" or "PA7-T1CKI" to keep Timerx/PWMx/BUZZERx running in SLEEP mode, otherwise Timerx will stop counting
count, maintain the count value before it goes to sleep.
4. If Timerx is used to count T0CKI or T1CKI, please refer to Section 7.2 and Section 7.2 for requirements of T0CKI/T1CKI

7.3

7.5.1 Summary of Timer3/4/5 Related Registers

| name | state | Register address | reset value |
|---------|---|---|---------------------|
| P3PER | <u>TMRx valid bit (valid when PxINTS = 0)</u> ⁴ | PWM3CR0[6:4] 0x10F | RW ^W 000 |
| P4PER | 000 = 4 digits 001 = 5 digits 010 = 6 bits 011 = 8 bits | 100 = 9 bits 101 = 10 bits 110 = 11 bits 111 = 12 bits | |
| P5PER | | PWM5CR0[6:4] 0x11B | |
| P3CKSRC | <u>TIMERx / PWMx clock source</u> 000 = 2x instruction clock / (TxCKDIV + 1) 001 = HIRC / (TxCKDIV + 1) 010 = T0CKI / (TxCKDIV + 1) 011 = T1CKI / (TxCKDIV + 1) | PWM3CR0[3:1] 0x10F | RW ^W 000 |
| P4CKSRC | 100 = HIRC / (TxCKDIV + 1), while PWMx output is low 101 = HIRC / (TxCKDIV + 1), while PWMx output is high | PWM4CR0[3:1] 0x115 | |
| P5CKSRC | 110 = HIRC / (TxCKDIV + 1), while PWMx is modulated according to the high pulse PxCK (see Table 7-13) 111 = HIRC / (TxCKDIV + 1), while PWMx is modulated according to the low pulse PxCK (see Table 7-13) | PWM5CR0[3:1] 0x11B | |
| P3BZR | <u>PWM / BUZZER mode selection</u> | PWM3CR0[0] 0x10F | RW ^W 0 |
| P4BZR | 1 = BUZZER output | PWM4CR0[0] 0x115 | |
| P5BZR | 0 = <u>PWM output</u> | PWM5CR0[0] 0x11B | |
| P3EN | <u>TIMERx / PWMx operating mode</u> | PWM3CR1 [7] 0x110 | |
| P4EN | 1 = PWM / BUZZER mode | PWM4CR1 [7] 0x116 | |
| P5EN | 0 = <u>Timer/Counter mode</u> | PWM5CR1 [7] 0x11C | |
| P3POL | <u>PWMx output polarity</u> | PWM3CR1[6] 0x110 | |
| P4POL | 1 = Active low | PWM4CR1[6] 0x116 | |
| P5POL | 0 = <u>active high</u> | PWM5CR1[6] 0x11C | |
| TMR3PS | <u>PWMx Prescaler</u> | PWM3CR1[5:3] 0x110 | RW ^W 000 |
| TMR4PS | 000 = 1 001 = 2 010 = 4 011 = 8 | 100 = 16 101 = 32 110 = 64 111 = 128 | |
| TMR5PS | | PWM5CR1[5:3] 0x11C | |
| TMR3ON | <u>TIMERx</u> | PWM3CR1[2] 0x110 | |
| TMR4ON | 1 = enable | PWM4CR1[2] 0x116 | RW ^W 0 |
| TMR5ON | 0 = <u>off</u> | PWM5CR1[2] 0x11C | |

4 When changing the value of PxPER, first set TMRxON = 0;

| name | state | Register address | reset value |
|----------------|---|--------------------|--------------------|
| T3CKDIV 5 TMR3 | clock divider bit (refer to "P3CKSRC") | T3CKDIV[7:0] 0x111 | RWÿ0000 0000 |
| T4CKDIV 5 TMR4 | clock divider bits (refer to "P4CKSRC") | T4CKDIV[7:0] 0x117 | RWÿ0000 0000 |
| T5CKDIV 5 TMR5 | clock divider bits (refer to "P5CKSRC") | T5CKDIV[7:0] 0x11D | RWÿ0000 0000 |
| TMR3L | TMR3 count result register lower 8 bits | TMR3L[7:0] | 0x10C RWÿxxxx xxxx |
| TMR3H | TMR3 count result register high 4 bits | TMR3H[7:4] | 0x10D RWÿxxxx |
| PR3L | PR3 period register lower 8 bits | PR3L[7:0] | 0x10E RWÿ1111 1111 |
| PR3H | PR3 period register upper 4 bits | TMR3H[3:0] | 0x10D RWÿ1111 |
| TMR4L | TMR4 count result register lower 8 bits | TMR4L[7:0] | 0x112 RWÿxxxx xxxx |
| TMR4H | TMR4 count result register upper 4 bits | TMR4H[7:4] | 0x113 RWÿxxxx |
| PR4L | PR4 period register lower 8 bits | PR4L[7:0] | 0x114 RWÿ1111 1111 |
| PR4H | PR4 period register upper 4 bits | TMR4H[3:0] | 0x113 RWÿ1111 |
| TMR5L | TMR5 count result register lower 8 bits | TMR5L[7:0] | 0x118 RWÿxxxx xxxx |
| TMR5H | TMR5 count result register upper 4 bits | TMR5H[7:4] | 0x119 RWÿxxxx |
| PR5L | PR5 period register lower 8 bits | PR5L[7:0] | 0x11A RWÿ1111 1111 |
| PR5H | PR5 period register upper 4 bits | TMR5H[3:0] | 0x119 RWÿ1111 |

Table 7-11 Timer3/4/5 related user control registers

5 When writing to TxCKDIV, the divided output of the clock source will be updated immediately;

| name | state | register | address | reset value |
|---------------|--|-----------------------------------|-----------------------|------------------|
| GIE | <u>global interrupt</u> 1 = Enabled (PEIE, TMRxE applies) 0 = <u>Globally disabled (wakeup not affected)</u> | INTCON[7] | 0x0B 0x8B 0x10B | RW _{yo} |
| LIKE THIS | <u>Peripheral total interrupt</u> 1 = Enabled (TMRxE applies) 0 = off (no wakeup) | INTCON[6] | | RW _{yo} |
| P3INTS | <u>Timerx Interrupt Select Bits</u> | PWM3CR0[7] 0x10F RW _{yo} | | |
| P4INTS | 1 = TMRx and PRx match interrupt | PWM4CR0[7] 0x115 RW _{yo} | | |
| P5INTS | 0 = TMRx overflow interrupt | PWM5CR0[7] 0x11B RW _{yo} | | |
| TMR3IE Timerx | <u>interrupt</u> 1 = enable 0 = off (no wakeup) | PWM3CR1[1] 0x110 RW _{yo} | | |
| TMR4IE | | PWM4CR1[1] 0x116 RW _{yo} | | |
| TMR5IE | | PWM5CR1[1] 0x11C RW _{yo} | | |
| TMR3IF | <u>Timerx interrupt flag bit</u> | PWM3CR1[0] 0x110 RW _{yo} | | |
| TMR4IF | 1 = match/overflow (latched) | PWM4CR1[0] 0x116 RW _{yo} | | |
| TMR5IF | 0 = no match/no overflow | PWM5CR1[0] 0x11C RW _{yo} | | |

Table 7-12 Timerx (x = 3, 4, 5) Interrupt Enable and Status Bits

7.5.2 Timer3/4/5 Register Read/Write Operation

TMRxH and TMRxL cannot be read or written at the same time, should set “TMRxON = 0” to stop counting, and then read/write TMRxH/TMRxL write operation.

7.5.3 PWMx Mode

PWMx mode - 3 PWM3/4/5 duty cycles are independent of each other.

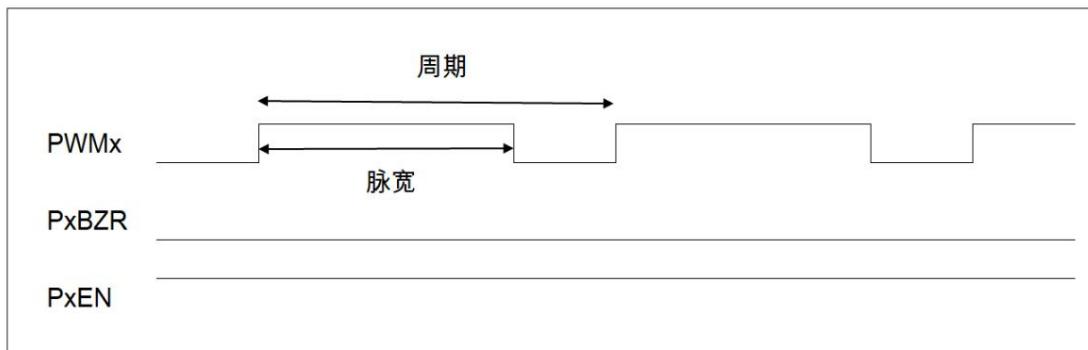


Figure 7-6 PWMx mode (forward output)

The PWMx period is determined by the PxPER register, as shown in Equation 7-1. The pulse width and duty cycle are determined by PRxH:L as shown in Equation 7-2 and Equation 7-3_{yo}

$$\text{Equation 7-1 } \text{PWMx cycle} = 2^{N^*} \cdot TPxCK \cdot (TMRx \text{ prescale value}) \quad \text{for } PxPER \text{ valid bits set}$$

$$\text{Equation 7-2 } \text{PWMx pulse width} = (PRx) * TPxCK \cdot (TMRx \text{ prescale value})$$

$$\text{Equation 7-3 } \text{PWMx duty cycle} = (PRx) / 2^N \quad \text{for } PxPER \text{ valid bits set}$$

In addition, PWMx can output different modulation waveforms with clock frequency division. The 8 clock sources and PWM outputs of Timerx/PWMx are as follows:

| PxCKSRC | Clock source and frequency division | PWMx / BUZZERx outputs |
|---------|--------------------------------------|---|
| 000 | 2x Instruction Clock / (TxCKDIV + 1) | normal |
| 001 | HIRC / (TxCKDIV + 1) | normal |
| 010 | T0CKI / (TxCKDIV + 1) | normal |
| 011 | T1CKI / (TxCKDIV + 1) | normal |
| 100 | HIRC / (TxCKDIV + 1) | low level |
| 101 | HIRC / (TxCKDIV + 1) | high level |
| 110 | HIRC / (TxCKDIV + 1) | PWMx modulates PxCK according to high pulse (that is, when the TIMERx frequency division is output during the original high pulse of PWMx clock, the original low pulse keeps the output low) |
| 111 | HIRC / (TxCKDIV + 1) | PWMx modulates PxCK according to low pulse (that is, when the TIMERx frequency division is output during the original low pulse of PWMx clock, the original high pulse becomes the output low) |

Table 7-13 PWM output mode

Note:

1. In PWMx mode, when TMRxH:L = 2 N (N is the valid bit set by PxPER), TMRxH:L will be automatically cleared to 0;

2. PRxH and PRxL cannot be written at the same time. Writing to PRx will immediately update the current duty cycle.

The scalar value is written to PRx;

3. The priority of ECCP is higher than that of PWM3/4/5. If you use ECCP's PWM and PWM3/4/5 at the same time, you need to set ECCP to single output mode (P1M=00, see [chapter 10](#) ECCP module);

Buzzer (**BUZZERx**) Mode—PWMx outputs a 50% duty cycle square wave with a period determined by PRxH:L, as shown in Equation [7-4](#).

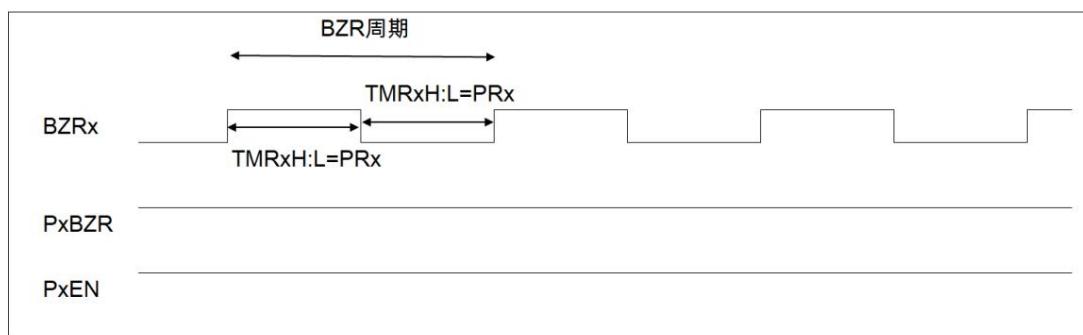


Figure 7-7 BUZZER square wave with 50% duty cycle

$$\text{Official 7-4 BUZZERx cycle} = 2 \cdot PRx \cdot TPxCK \cdot (TMRx \text{ prescale value})$$

Note:

1. In BUZZER mode, the valid bit of TMRx is 12 bits, which has nothing to do with PxPER. When TMRxH:L = PRxH:L, TMRxH:L will be automatically cleared to 0;

2. In BUZZER mode, when PRx = 0x000, PWMx outputs 0, and TMRxF will be set to 1 only when TMRx overflows;

8. SLEEP sleep mode (POWER-DOWN)

In sleep mode, the instruction clock is turned off, instruction execution is stopped, and most modules are powered down to reduce power consumption. As shown in Table 8-1 , FT61F02x

Each module can be selectively turned on during sleep according to actual needs, without the need for instruction intervention, so that its corresponding functions such as LVR, LVD,

WDT, Timers, Comparator, PWM and ADC can keep running in SLEEP mode. Some modules can also be configured to enter

Automatically shuts down after SLEEP without being commanded to shut down.

| module | Configuration conditions of each module in SLEEP mode | |
|----------------------------|---|--------------------------|
| | Run | Auto close? |
| instruction clock | (always off) | Yes |
| LVR (config LVREN) | Enabled or controlled by command (SLVREN = 1) | Enable in non-SLEEP mode |
| LVD | LVDEN = 1 | No |
| WDT | WDTE or SWDTEN | No |
| TIMER0 | (always off) | Yes |
| HOUR1 | TMR1ON = 1 & T1SYNC = 1 & TMR1CS = 1 & T1OSCEN = 1 | TMR1ON = 0 |
| TIMER2 | (always off) | Yes |
| PWM3/4/5 | PxCKSRC = 010 / 011 & TMRxON = 1 | No |
| Enhanced ECCP | (follow TIMER2) | |
| HIRC / LIRC / EC / LP / XT | (follows the state of the peripherals that use them) | |
| ADC | (ADC is operational when ADON = 1 and ADCS = x11) | |
| Comparator | (Comparator keeps running when CM ѕ 000 or 111) | |
| Regulator | (Regulator keeps running when VREG_OE = 1) | |
| I/O | (Unless the PWM is enabled while SLEEP, the I/O will remain in the state it was in before going into SLEEP state) | |

Table 8-1 Except for the instruction clock, other modules can keep running in SLEEP mode as required

8.1 Enter SLEEP

The CPU enters sleep mode by executing the SLEEP instruction. When going to sleep:

1. If the WDT is enabled, the WDT postscaler (if assigned to the WDT) and the timer will be cleared and restarted.

2. Timeout flag (/TF) = 1.

3. Power-down flag (/PF) = 0.

4. Clock Source

• The instruction clock is automatically turned off;

• If Timer keeps running under SLEEP, its selected clock source is HIRC, LIRC or external oscillator (EC, LP, XT)

will also keep running. If a Timer is automatically shut down during sleep, its clock source will also be shut down automatically, unless this clock source

Also used by another Timer that keeps running.

• The instruction clock is automatically stopped, so even if the output internal instruction clock is configured, its output will stop after going to sleep.

5. I/O end

- If Timer3/4/5 keep running in SLEEP, the PWM output will also keep running. If Timer3/4/5 is automatically turned off, Then the output of the PWM will keep the state it was in before going into SLEEP.
- Other digital output ports will maintain their state (high-impedance, low or high) before entering SLEEP. • When "ADON = 1" and ADC selected clock source keeps running, ADC can run. If its clock source is automatically turned off, the ADC will also be turned off automatically.

For details on how each peripheral works in the SLEEP state, please consult the appropriate chapters.

8.2 Wake up from **SLEEP**

There are 2 basic principles for waking from sleep:

- Time based, i.e. the CPU wakes up after a certain amount of time. It is recommended to choose LIRC as the clock source for timing, because LIRC is faster than HIRC lower power consumption.
- Event based, i.e. trigger POR, system reset, wake up only without generating interrupt, and events that generate interrupt, such as ADC, port Change interrupt, PC1 edge interrupt.

1. If enabled, the watchdog timer can trigger wake-up (see [Section 7.1 Watchdog Timer](#)).

2. Full reset and system reset:

- POR full reset (cannot be shut down) •

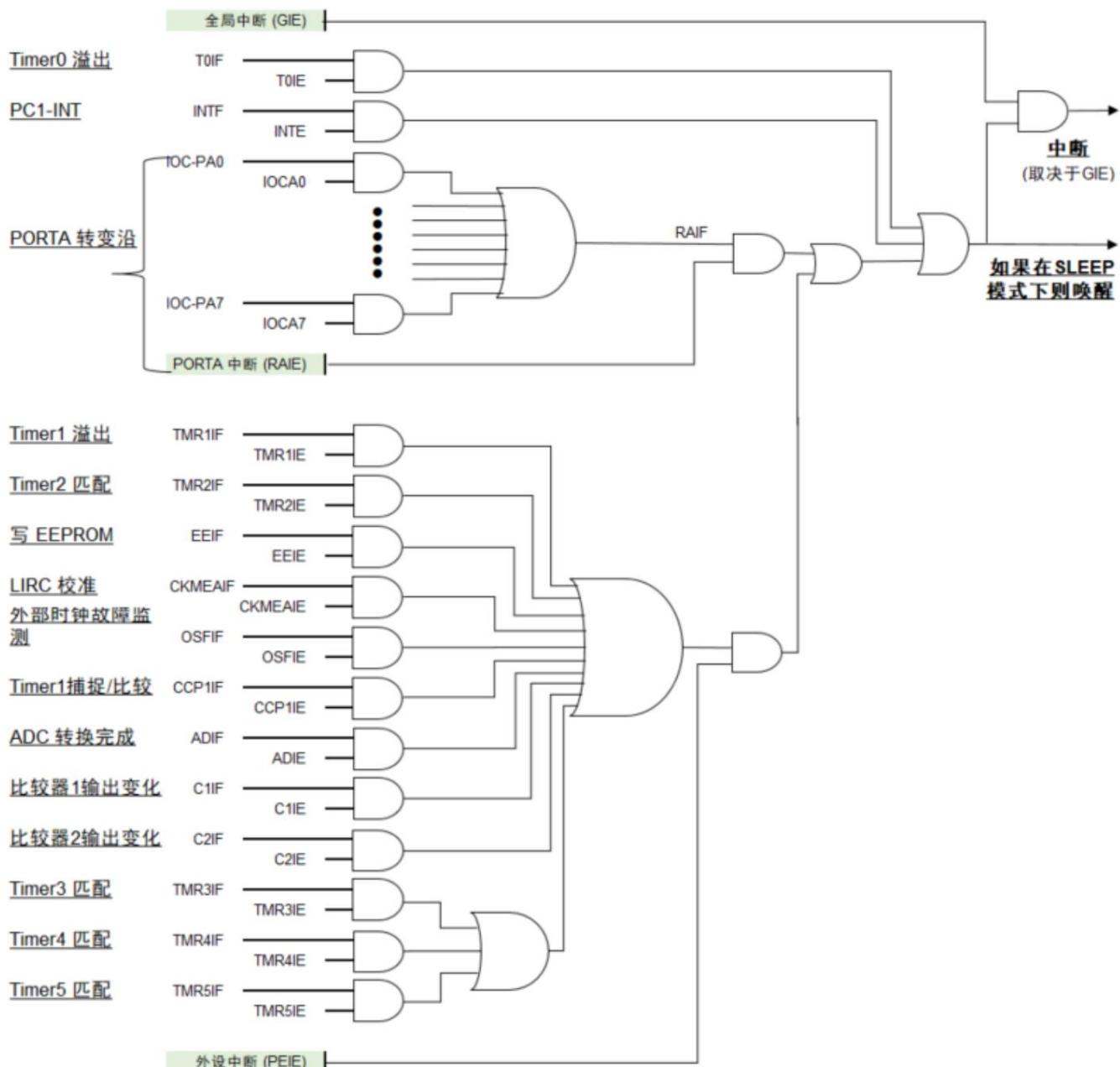
External system reset via /MCLR (if enabled) • LVR reset (if enabled)

3. Enable interrupt (disabling "global interrupt enable" does not affect the wake-up function). See [Section 9 Interrupts](#).

Note:

1. Waking up from sleep will clear the WDT.

9. Interrupt (INTERRUPTS)



注：由于指令时钟在睡眠期间停止，只有不选择指令时钟作为时钟源的外设能将器件从睡眠中唤醒；

Figure 9-1 Block Diagram of Interrupt Structure

The CPU supports 15 interrupt sources, divided into 2 groups:

1) Non-peripheral interrupts (Timer0 and I/O)

- Timer0 overflow
- PC1-INT (automatic rising or falling edge interrupt)
- PORTA port change interrupt (software control)

2) Peripheral interrupt



- Timer1 overflow
- Timer2 matches PR2
- DATA EEPROM write complete
- LIRC and HIRC cross calibration complete
- Fail-safe clock monitor
- Timer1 capture/compare
- ADC conversion complete
- Comparator 1 / Comparator 2 output changes
- Timer3 / Timer4 / Timer5 match

Unlike other Timers, WDT overflows do not generate interrupts. Except for external I/O interrupts, please refer to the corresponding chapters for other interrupts.

When an interrupt occurs, the PC jumps and executes the "Interrupt Service Routine (ISR)". There are multiple layers of control for the disable/enable of interrupts:

- Each interrupt source has its own independent interrupt enable bit: T0IE, INTE, IOCAx, TMRxIE(x=1,2,3,4,5), EEIE, CKMEAIE, CxIE(x=1,2), OSFIE, ADIE, CCP1IE
- Eight PAx interrupt inputs share one port interrupt enable bit: PAIE (PORTA Interrupt Enable).
- Peripheral interrupts have a total interrupt enable bit: PEIE (PEripheral Interrupt Enable).
- If all of the above control bits are turned off, wake-up from sleep will not be performed.
- All interrupts are controlled by the global interrupt enable bit: GIE (Global Interrupt Enable). Unlike other enable bits, wake-up from sleep is still allowed when the global interrupt enable bit is turned off.
- Turning off the interrupt enable bit does not affect the setting of the interrupt flag bit.
- Timer0 and Timer2 interrupts cannot wake the CPU from sleep.

The interrupt processing sequence is as follows:

- Automatically set "GIE = 0", thus turning off interrupts.
- The return address is pushed onto the stack and the program pointer PC is loaded with address 0x0004.
- 1 – 2 instruction cycles after the interrupt occurs, jump to the "Interrupt Service Routine (ISR)" to start processing the interrupt.
- Execute the "Return from Interrupt (RETI)" instruction to exit the ISR. The currently serviced interrupt flag must be cleared before RETI.
- When the ISR completes, the PC returns to the address before the interrupt, or to the address immediately following the SLEEP instruction if in SLEEP mode address.
- Automatically set "GIE = 1" when RETI is executed, thereby enabling interrupts.

Note: During an interrupt, only the return PC address is automatically saved on the stack. If the user needs to save other important register values

(such as W, STATUS registers, etc.), these values must be correctly written into the temporary registers through instructions. It is recommended to use the last 16 bytes of SRAM as temporary registers, because all banks share these 16 bytes, and there is no need to switch banks to Save code.

9.1 Summary of interrupt related registers

| name | address bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset value (RW) | |
|---------------|--|-------|-----------|-------------|-------|---------------|--------|-----------|------------------|-----------|
| INTCON 0x0B | | GIE | LIKE THIS | TOIE | NOT | PAY | TOIF | INTF | PAIF | 0000 0000 |
| PIE1 | 0x8C EEEE | | CKMEAIE | ÿ | | C2IE | C1IE | OSFIE | TMR2IE TMR1IE | 0000 0000 |
| PIR1 | 0x0C EEIF | | CKMEAIF | ÿ | | C2IF | C1IF | OSFIF | TMR2IF TMR1IF | 0000 0000 |
| PIE2 | 0x8D | | | | | | | CHICKEN | CCP1IE | ----00 |
| PIR2 | 0x0D | | | | | | | ADIF | CCP1IF | ----00 |
| PWM3CR0 0x10F | P3INTS P3PER[2:0] | | | | | P3CKSRC[2:0] | | | P3BZR | 0000 0000 |
| PWM3CR1 0x10 | P3EN | P3POL | | TMR3PS[2:0] | | TMR3ON TMR3IE | TMR3IF | 0000 0000 | | |
| PWM4CR0 0x15 | P4INTS P4PER[2:0] | | | | | P4CKSRC[2:0] | | | P4BZR | 0000 0000 |
| PWM4CR1 0x16 | P4EN | P4POL | | TMR4PS[2:0] | | TMR4ON TMR4IE | TMR4IF | 0000 0000 | | |
| PWM5CR0 0x1B | P5INTS P5PER[2:0] | | | | | P5CKSRC[2:0] | | | P5BZR | 0000 0000 |
| PWM5CR1 0x1C | P5EN | P5POL | | TMR5PS[2:0] | | TMR5ON TMR5IE | TMR5IF | 0000 0000 | | |
| OPTION 0x81 | /PAPU INTEDG T0CS T0SE | | | | PSA | PS2 | PS1 | PS0 | | 1111 1111 |
| TRISA | 0x85 PORTA direction control | | | | | | | | | 1111 1111 |
| JOKE | 0x96 PORTA port change interrupt setting | | | | | | | | | 0000 0000 |

Table 9-1 Interrupt related register addresses and default values

| name | state | | Register address | reset value |
|----------------------|---|--|------------------|-------------|
| GIE global interrupt | 1 = Enable (PEIE, independent enable bits for each interrupt apply) 0 = <u>global shutdown</u> (wakeup not affected) | | INTCON[7] | RWÿ0 |
| LIKE THIS | Peripheral center broken 1 = Enable (independent enable bits for each interrupt apply) 0 = off (no wakeup) | | INTCON[6] | RWÿ0 |
| TOIE | Timer0 overflow interrupt | | INTCON[5] | 0x0B |
| NOT | PC1ÿINT External interrupt | | INTCON[4] | 0x8B |
| PAY | PORTA port change total interrupt | | INTCON[3] | 0x10B |
| TOIF | Timer0 overflow interrupt flag | | INTCON[2] | RWÿ0 |
| INTF | PC1ÿINT External interrupt flag bit | | INTCON[1] | RWÿ0 |
| PAIF | PORTA port change total interrupt flag | | INTCON[0] | RWÿ0 |

Table 9-2 INTCON register

| name | state | | Register address | reset value |
|-----------------------------|---|--|------------------|-------------|
| THIS | EE write complete interrupt | | PIE1 [7] | RWÿ0 |
| CKMEAIE LIRC | and HIRC cross calibration complete interrupt | | PIE1 [6] | RWÿ0 |
| C2IE Comparator 2 Interrupt | | | PIE1 [4] | RWÿ0 |
| C1IE Comparator 1 Interrupt | | | PIE1 [3] | 0x8C |
| OSFIE External | Oscillator Fail Interrupt | | PIE1 [2] | RWÿ0 |
| TMR2IE Timer2 | and PR2 match interrupt | | PIE1 [1] | RWÿ0 |
| TMR1IE Timer1 | overflow interrupt | | PIE1 [0] | RWÿ0 |
| CHICKEN | ADC conversion complete interrupt | | PIE2[1] | 0x8D |
| CCP1IE CCP1 | Capture/Match Interrupt | | PIE2[0] | RWÿ0 |

Table 9-3 PIE register

| name | state | Register address | reset value |
|---------|---|-----------------------------|-------------------|
| EEIF | EEPROM write complete flag | 1 = Yes (latched) 0 = No | RW _y 0 |
| CKMEAIF | LIRC and HIRC cross calibration complete flag | | RW _y 0 |
| C2IF | Comparator 2 Interrupt Flag | | RW _y 0 |
| C1IF | Comparator 1 Interrupt Flag | | RW _y 0 |
| OSFIF | External Oscillator Failure Flag | | RW _y 0 |
| TMR2IF | Timer2 and PR2 match flag | | RW _y 0 |
| TMR1IF | Timer1 overflow flag | | RW _y 0 |
| ADIF | ADC conversion complete flag | | RW _y 0 |
| CCP1IF | CCP1 capture/match flag occurred | | RW _y 0 |
| PIR1[7] | 0x0C | 0x0D | RW _y 0 |
| PIR1[6] | | | RW _y 0 |
| PIR1[4] | | | RW _y 0 |
| PIR1[3] | | | RW _y 0 |
| PIR1[2] | | | RW _y 0 |
| PIR1[1] | | | RW _y 0 |
| PIR1[0] | | | RW _y 0 |
| PIR2[1] | | | RW _y 0 |
| PIR2[0] | | | RW _y 0 |

Table 9-4 PIRx Registers

| name | state | register | address | reset value |
|---------------|----------------------|--|------------------|-------------------|
| P3INTS Timer3 | Interrupt Select Bit | 1 = TMRx and PRx match interrupt 0 = TMRx overflow interrupt Note: x=3, 4, 5 | PWM3CR0[7] 0x10F | RW _y 0 |
| P4INTS Timer4 | Interrupt Select Bit | | PWM4CR0[7] 0x115 | RW _y 0 |
| P5INTS Timer5 | Interrupt Select Bit | | PWM5CR0[7] 0x11B | RW _y 0 |
| TMR3IE Timer3 | Interrupt Enable Bit | 1 = enable 0 = off (no wakeup) | PWM3CR1[1] 0x110 | RW _y 0 |
| TMR4IE Timer4 | Interrupt Enable Bit | | PWM4CR1[1] 0x116 | RW _y 0 |
| TMR5IE Timer5 | Interrupt Enable Bit | | PWM5CR1[1] 0x11C | RW _y 0 |
| TMR3IF Timer3 | interrupt flag bit | 1 = match/overflow (latched) 0 = no match/no overflow | PWM3CR1[0] 0x110 | RW _y 0 |
| TMR4IF Timer4 | interrupt flag bit | | PWM4CR1[0] 0x116 | RW _y 0 |
| TMR5IF Timer5 | interrupt flag bit | | PWM5CR1[0] 0x11C | RW _y 0 |

Table 9-5 Timer3/4/5 Interrupt Register

| name | state | register address | reset value |
|--------|---|----------------------------|--|
| /PAPU | <u>PORTA pull-up</u> 1 = global shutdown 0 = Controlled by WPUA | OPTION[7] OPTION[6] | RW _y 1 RW _y 1 |
| INTEDG | <u>PC1 interrupt edge</u> 1 = rising edge 0 = falling edge | | |
| TRISA | <u>PORTA I/O digital output (direction control)</u> 1 = <u>input</u> (turns off digital output) 0 = pull-up/pull-down off | TRISA[7:0] 0x85 | RW _y 11111111 |
| JOKE | <u>PORTA port change interrupt</u> 1 = enabled 0 = disabled | | |

Table 9-6 OPTION, TRISA and IOCA registers

9.2 PC1-INT and PORTA port change interrupt

| name | PC1-INT | PORTA port change interrupt |
|---------------------------|--|--|
| number of channels | PC1 only | PA0 – PA7 (up to 8 channels) |
| I/O settings | TRISC[1] = 1; ANSEL[4] = 0; CMCON0[2:0] = 111 | TRISA[x] = 1; ANSEL[x] = 0; CMCON0[2:0] = 111 |
| Triggered by other | INTEDG, INTE, GIE, INTF Rising edge | YOCA, STRAW, GIE, PAIF |
| settings | or falling edge (choose one of two) | 0 $\ddot{\vee}$ 1 or 1 $\ddot{\vee}$ 0 |
| Need software monitoring? | No | need |

Table 9-7 Differences between PC1-INT and PORTA port change interrupts

The PC1-INT and PORTA port change interrupts are external I/O interrupts. If set correctly, PC1-INT will run in the background without monitoring

Governor. PORTA port change interrupts require continuous software monitoring. For PORTA port change interrupt:

1. Latch the input register value into the port change interrupt latch (by reading PORTA).
2. When the input changes, the difference between the input register value and the latch value sets PAIF.
3. The latching process of the input register (ie, the process of reading PORTA) will update the reference level for comparison, if immediately after PAIF is set

Reading PORTA clears the triggering condition of the port change interrupt. When the port mismatch event no longer exists, the PAIF can be cleared by the command
remove.

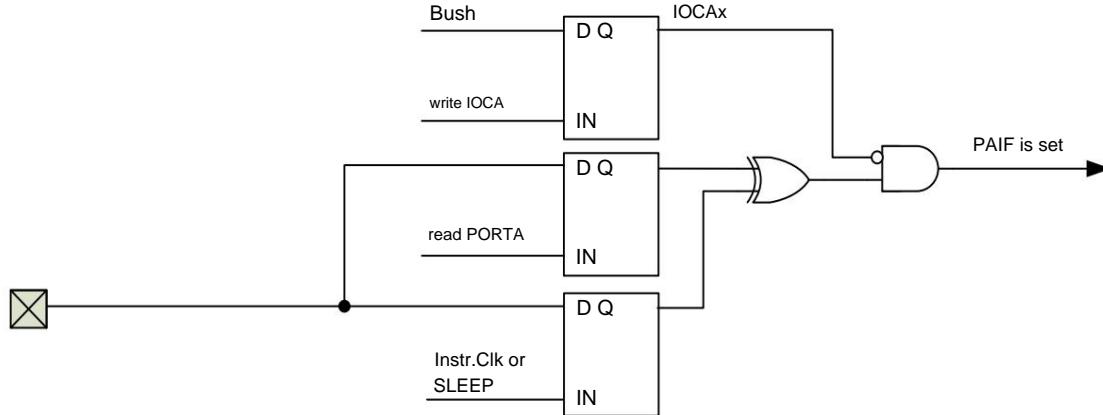


Figure 9-2 PORTA transition edge interrupt

10. Enhanced Capture/Compare/PWM Module (ECCP)

The Enhanced Capture/Compare/PWM module (ECCP) can be used to time and control various events.

- Capture Mode: Time the duration of the event.
- Compare Mode: Trigger an external event after a preset duration.
- PWM Enhanced Mode: Single Output, Half-Bridge Mode, Full-Bridge Mode (forward or reverse).

| ECCP | timer |
|-----------------------|---|
| catch | Timer1 (must run in timer mode or synchronous counter mode) |
| Compare | Timer1 (must run in timer mode or synchronous counter mode) |
| PWM (Enhanced) Timer2 | |

Table 10-1 Timer resources required by ECCP modes

10.1 Summary of ECCP related registers

| name | address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | reset value |
|--------------|---------|------------|------------------------|--------------|----------------|-------------------|---|------------|-----------|-------------|
| T1CON | 0x10 | T1GINV TMR | GE | T1CKPS[1:0] | T1OSCEN T1SYNC | TMR1CS | TMR1ON 0000 0000 | | | |
| T2CON | 0x12 | | | TOUTPS[3:0] | | TMR2ON | T2CKPS[1:0] | | -000 0000 | |
| TMR1L | 0x0E | | | | | | TMR1 count result register lower 8 bits | | | xxxx xxxx |
| TMR1H | 0x0F | | | | | | TMR1 count result register upper 8 bits | | | xxxx xxxx |
| TMR2 | 0x11 | | | | | | TMR2 count result register | | | xxxx xxxx |
| PR2 | 0x92 | | | | | | PR2 Period Register | | | 1111 1111 |
| CCPR1L | 0x13 | | | | | | Capture/Compare/PWM Register Lower 8 Bits | | | xxxx xxxx |
| CCPR1H | 0x14 | | | | | | Capture/compare/PWM register upper 8 bits | | | xxxx xxxx |
| CCP1CON 0x15 | | | P1M[1:0] | DC1B[1:0] | | | CCP1M[3:0] | | | 0000 0000 |
| PWM1CON 0x16 | | PRSEN | | | | | PDC[6:0] | | | 0000 0000 |
| ECCPAS | 0x17 | ECCPASE | | ECCPAS [2:0] | | PSSAC[1:0] | | PSSBD[1:0] | | 0000 0000 |
| PWM1AUX 0x90 | | AUX1EN | P1OS P1FOE P1EOE P1DOE | | | P1COE P1BOE P1AOE | 0000 0000 | | | |

Table 10-2 ECCP related user register addresses

| name | state | | | Register address | reset value | |
|---|---------------------|--------------------------------------|---|------------------|-------------|-------------|
| TMR1L TMR1 count result register lower 8 bits | | | | TMR1L[7:0] | 0x0E RW | Wÿ0000 0000 |
| TMR1H TMR1 count result register upper 8 bits | | | | TMR1H[7:0] | 0x0F RW | Wÿ0000 0000 |
| CCPR1L Capture Compare Register Lower 8 Bits | | | | CCPR1L[7:0] | 0x13 RW | Wÿxxxx xxxx |
| CCPR1H capture compare register upper 8 bits | | | | CCPR1H[7:0] | 0x14 RW | Wÿxxxx xxxx |
| CCP1M | ECCP mode selection | | | CCP1CON[3:0] | RWÿ0000 | |
| | value | Mode | describe | | | |
| | 0000 | off | Reset the ECCP module | | | |
| | 0001/0011 | Not used (none) | | | | |
| | 0100 | capture mode (catch feet CCP1) | Every 1 falling edge | | | |
| | 0101 | | Every 1 rising edge | | | |
| | 0110 | | Every 4th rising edge | | | |
| | 0111 | | Every 16 rising edges | | | |
| | 0010 | Compare mode (when matching) | CCP1 toggle output | | | |
| | 1000 | | CCP1 output high | | | |
| | 1001 | | CCP1 output low | | | |
| | 1010 | | CCP1 pin is not affected | | | |
| | 1011 | | Trigger on a special event (CCP1 pin not affected) | | | |
| | 1100 | PWM mode | P1A and P1C are active high; P1B and P1D are active high | | | |
| | 1101 | | P1A and P1C are active high; P1B and P1D are active low | | | |
| | 1110 | | P1A and P1C are active low; P1B and P1D are active high | | | |
| | 1111 | | P1A and P1C are active low; P1B and P1D are active low | | | |

Table 10-3 ECCP Capture/Compare/PWM Mode Registers

| name | state | | | Register address | reset value |
|---|--|---|--|-------------------------|--------------------|
| TMR2 | TMR2 count result register | | | TMR2[7:0] | 0x11 RW\0000 0000 |
| PR2 | PR2 Period Register | | | PR2[7:0] | 0x92 RW\1111 1111 |
| DC1B | PWM duty cycle lower 2 bits (only valid when CCP1M = 11xx) | | | CCP1CON[5:4] 0x15 RW\00 | |
| CCPR1L PWM duty cycle high 8 bits | | | | CCPR1L[7:0] | 0x13 RW\0xxxx xxxx |
| CCPR1H PWM duty cycle high 8-bit latch | | | | CCPR1H[7:0] | 0x14 RC\0xxxx xxxx |
| P1M | <u>PWM output configuration (only valid when CCP1M = 11xx) error! Not found</u> <small>Cite the source.</small> | | | CCP1CON[7:6] 0x15 RW\00 | |
| | 00 single output | P1A modulation, P1B, P1C and P1D are GPIO | | | |
| | 01 Full-bridge forward output | P1D modulation, P1A valid, P1B and P1C are invalid | | | |
| | 10 Half-bridge output | P1A and P1B modulation (with deadband control), P1C and P1D are GPIO | | | |
| | 11 Full-bridge reverse output | P1B modulation, P1C valid, P1A and P1D are invalid | | | |
| Note: When CCP1M = 11xx, P1A is capture input/compare output CCP1, P1B/P1C/P1D are GPIO; | | | | | |
| PRSEN | <u>After PWM auto-shutdown, auto-restart control</u> 1 = Enabled (ECCPASE is automatically cleared on exit shutdown event) 0 = <u>shutdown</u> (ECCPASE must be cleared by software when exiting shutdown event) | | | PWM1CON[7] | RW\0 |
| PDC | <u>PWM dead-time delay (valid in half-bridge mode)</u> Dead time = PDC[6:0] x instruction clock | | | PWM1CON[6:0] | RW\000 0000 |
| ECCPASE | <u>PWM auto-off state</u> 1 = An auto-shutdown event has occurred and the PWM output is turned off 0 = <u>PWM output is OK</u> | | | ECCPAS[7] | RW\0 |
| ECCPAS | <u>ECCP automatic shutdown source</u> 000 = disable automatic shutdown 001 = Comparator 1 output (C1OUT) goes high 010 = Comparator 2 output (C2OUT) goes high 011 = Comparator 1/2 output (CxOUT) goes high 100 = INT pin voltage is low 101 = INT pin voltage is low, or Comparator 1 output (C1OUT) goes high 110 = INT pin voltage is low, or Comparator 2 output (C2OUT) goes high 111 = INT pin voltage is low, or Comparator 1/2 output (CxOUT) goes high | | | ECCP [6:4] | RW\000 |

| name | state | | Register address | reset value |
|--------|---|--|------------------|--------------------|
| PSSAC | <u>After the PWM is automatically turned off, the P1A and P1C pin states</u> 00 = <u>output 0</u> 01 = output 1 1x = tri-state | | ECCPAS [3:2] | RW _y 00 |
| PSSBD | <u>P1B and P1D pin states after PWM auto-off</u> 00 = <u>output 0</u> 01 = output 1 1x = tri-state | | ECCPAS[1:0] | RW _y 00 |
| AUX1EN | <u>PWM auxiliary function (valid in half-bridge mode)</u> 1 = enable 0 = <u>disable</u> | | PWM1AUX[7] | RW _y 0 |
| P1OS | <u>PWM single pulse output (valid when AUX1EN=1)</u> 1 = Enable (automatically stop after outputting a pulse, P1x is GPIO) 0 = <u>off (PWM continuous output)</u> | | PWM1AUX[6] | RW _y 0 |
| P1FOE | P1F output | <u>1 = Enable (PWM output) 1</u> <u>0 = Disabled (GPIO)</u> | PWM1AUX[5] | RW _y 0 |
| P1EOE | P1E output | | PWM1AUX[4] | RW _y 0 |
| P1DOE | P1D output | | PWM1AUX[3] | RW _y 0 |
| P1COE | P1C output | | PWM1AUX[2] | RW _y 0 |
| P1BOE | P1B output | | PWM1AUX[1] | RW _y 0 |
| P1AOE | P1A output | | PWM1AUX[0] | RW _y 0 |

Table 10-4 PWM (Enhanced) Related User Control Registers

| name | state | Register address | reset value |
|-----------|---|------------------|------------------------|
| GIE | <u>global interrupt</u> 1 = Enabled (PEIE, CCP1IE applies) 0 = <u>global shutdown (wakeup not affected)</u> | INTCON[7] | RW _y 0 |
| LIKE THIS | <u>Peripheral total interrupt</u> 1 = Enabled (for CCP1IE) 0 = <u>off (no wakeup)</u> | INTCON[6] | RW _y 0 |
| CCP1IE | <u>CCP1 capture/match interrupt control</u> 1 = enable 0 = <u>off (no wakeup)</u> | PIE2[0] | 0x8D RW _y 0 |
| CCP1IF | <u>CCP1 capture/match interrupt flag</u> 1 = Capture/Match occurred (latch) 0 = <u>No capture/mismatch occurred</u> | PIR2[0] | 0x0D RW _y 0 |

Table 10-5 ECCP Interrupt Enable and Status Bits

1 When P1OS = 1, this bit will be automatically cleared to 0 when the next PWM cycle arrives;

10.2 Capture Mode

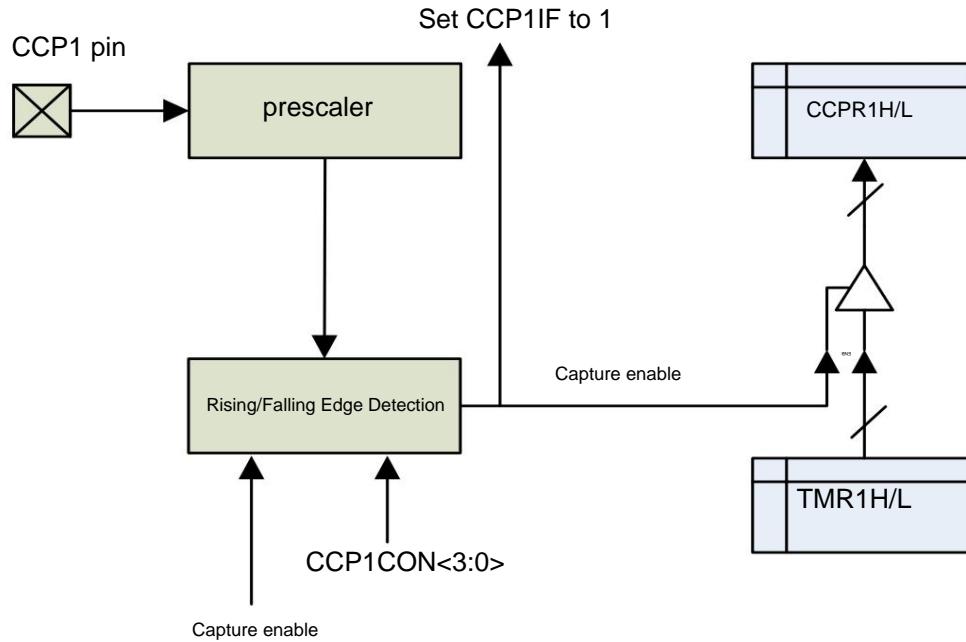


Figure 10-1 Block Diagram of Capture Mode

Capture mode, that is to capture the event of the CCP1 pin, the configurable 4 capture events (refer to "CCP1M") are as follows:

- Every 1 falling edge
- Every 1 rising edge
- Every 4th rising edge
- Every 16 rising edges

When a capture occurs, CCPR1H:CCPR1L captures the value of TMR1H:TMR1L, the interrupt flag bit CCP1IF is set, and the triggering of an interrupt and/or wake-up from sleep depends on the corresponding enable control bits (GIE, PEIE, CCP1IE).

Note:

1. In capture mode, the CCP1 (PC5) pin needs to be configured as an input. If CCP1 is configured as an output, writing the corresponding value to PORTC[5] will generates a capture event.
2. After a capture occurs, if another capture occurs before the CCPR1H:CCPR1L register is read, the captured value will be updated;
3. When changing the capture event, first set CCP1M=0000 to turn off the ECCP module to avoid false triggering of interrupts. The prescaler for capture events will be cleared when any Reset is generated, the ECCP module is turned off or switched to another mode.

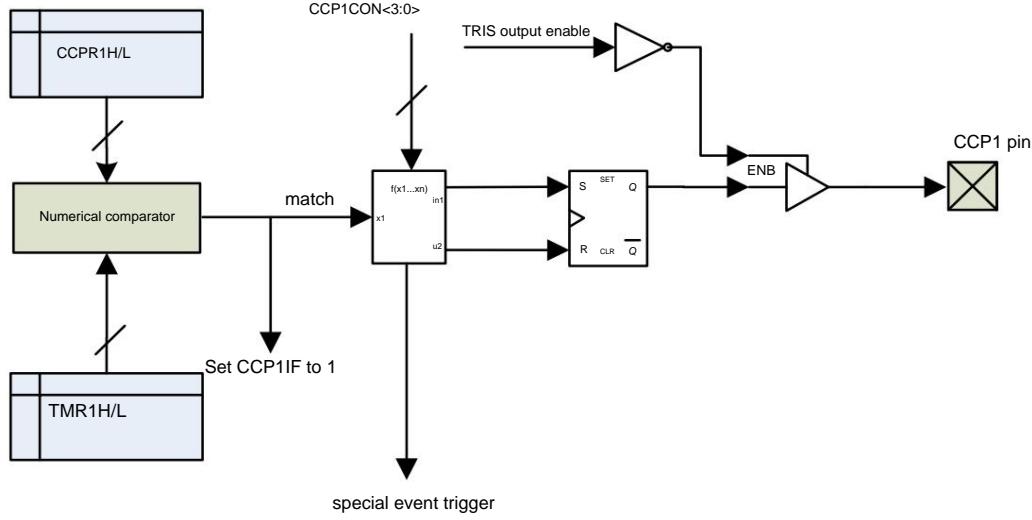
10.3 Compare Mode

Figure 10-2 Comparison Mode Block Diagram

Compare mode, which continuously compares the values of CCPR1H:CCPR1L and TMR1H:TMR1L, and can be configured to generate a
The following events (see "CCP1M"):

- CCP1 toggle output
- CCP1 output high
- CCP1 output low
- CCP1 pin is not affected
- Trigger a special event (CCP1 pin is not affected)

ÿ TMR1H:TMR1L is cleared (the interrupt flag bit TMR1IF will not be set to 1)

ÿ If the ADC is enabled, start an ADC conversion

When a match occurs, the interrupt flag bit CCP1IF is set, and whether an interrupt is triggered and/or wake-up from sleep depends on the corresponding enable control bit
(GIE, PIE, CCP1IE)ÿ

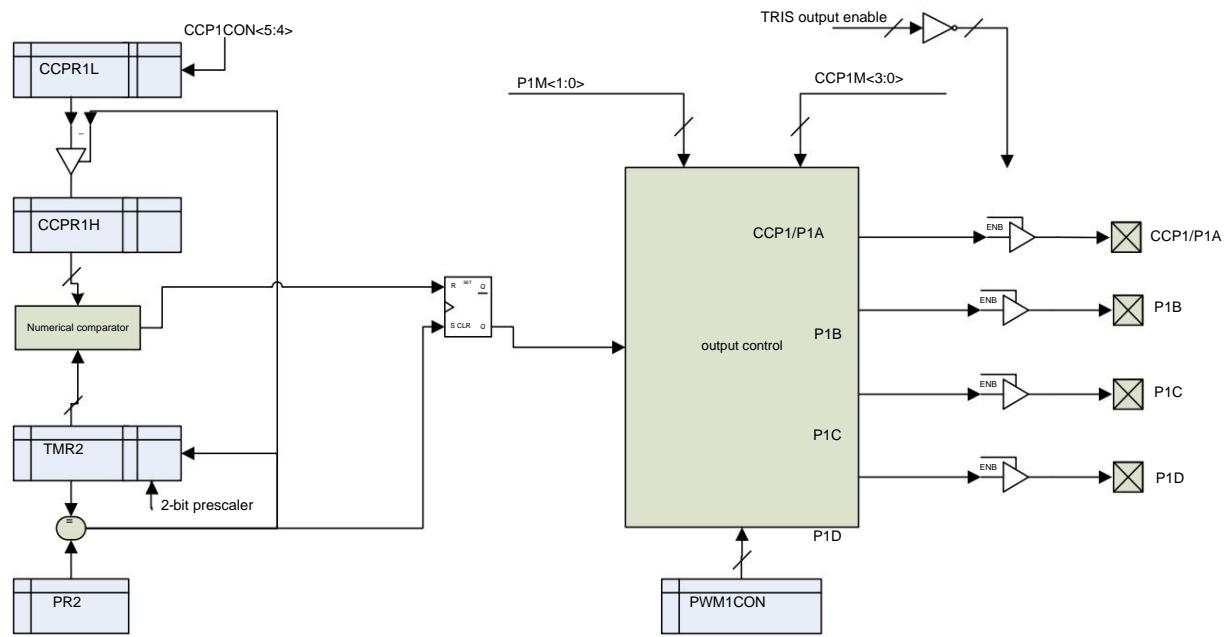
Note:

1. In compare mode, the CCP1 (PC5) pin needs to be configured as an output.

2. When a special event is triggered, the TMR1H:TMR1L registers will not be cleared until the next rising edge of the Timer1 clock.

Changing the value of CCPR1H:CCPR1L will clear the match condition, ie CCPR1H:CCPR1L can be used as a 16-bit programmable cycle register.

3. When a write operation to TMR1H:TMR1L occurs at the same time as the ECCP special event trigger, the write operation has priority;

10.4 PWM Enhanced Mode

Note: The 8-bit timer TMR2 register and the 2-bit prescaler form a 10-bit time base.

Figure 10-3 Enhanced PWM block diagram

Enhanced PWM Mode Features:

- Single PWM: P1A
- Half-bridge PWM:
 - ÿ Complementary outputs with dead time control: P1A, P1B
 - ÿ Auxiliary functions (3 pairs of complementary outputs with dead zone control, single pulse output): P1A, P1B, P1C, P1D, P1E, P1F
- Full -bridge PWM (forward, reverse): P1A, P1B, P1C, P1D
- 10-bit resolution
- PWM output polarity selectable
- Auto shutdown, auto restart mode

In SLEEP mode, Timer2 will stop counting and the PWM output will maintain its state before entering SLEEP.

Note:

1. Timer2 can be used for enhanced PWM mode or slow clock measurement, but both cannot be used at the same time;

10.4.1 Cycle

The PWM period is determined by the PR2 period register of Timer2, as shown in Equation 10-1:

$$\text{Equation 10-1 } \text{PWM cycle} = (PR2+1)*4*T2CK*(TMR2 \text{ prescale value}) \text{ for Timer2 clock source}$$

When TMR2 is incremented to equal PR2, on the next increment cycle:

1. TMR2 is reset to 0x00;
2. The upper 8 bits of the PWM duty cycle are latched from CCPR1L to CCPR1H;
3. PWM channel P1A~P1D, according to the selected polarity, the output is set to 1 or cleared to 0;

10.4.2 Duty Cycle

The PWM duty cycle is set by (CCPR1L, DC1B), CCPR1L is the upper 8 bits and DC1B is the lower 2 bits. Due to the internal double buffering
The CCPR1L and DC1B registers can be updated and written to at any time.

The calculation formulas of PWM pulse width and duty cycle are as follows:

$$\text{Formula 10-2} \quad \text{pulse width} = (\text{CCPR1L:DC1B}) * \text{TT2CK} * (\text{TMR2 prescaler value})$$

$$\text{Formula 10-3} \quad \text{duty cycle} = (\text{CCPR1L:DC1B}) / (4 * (\text{PR2} + 1))$$

10.4.3 PWM output

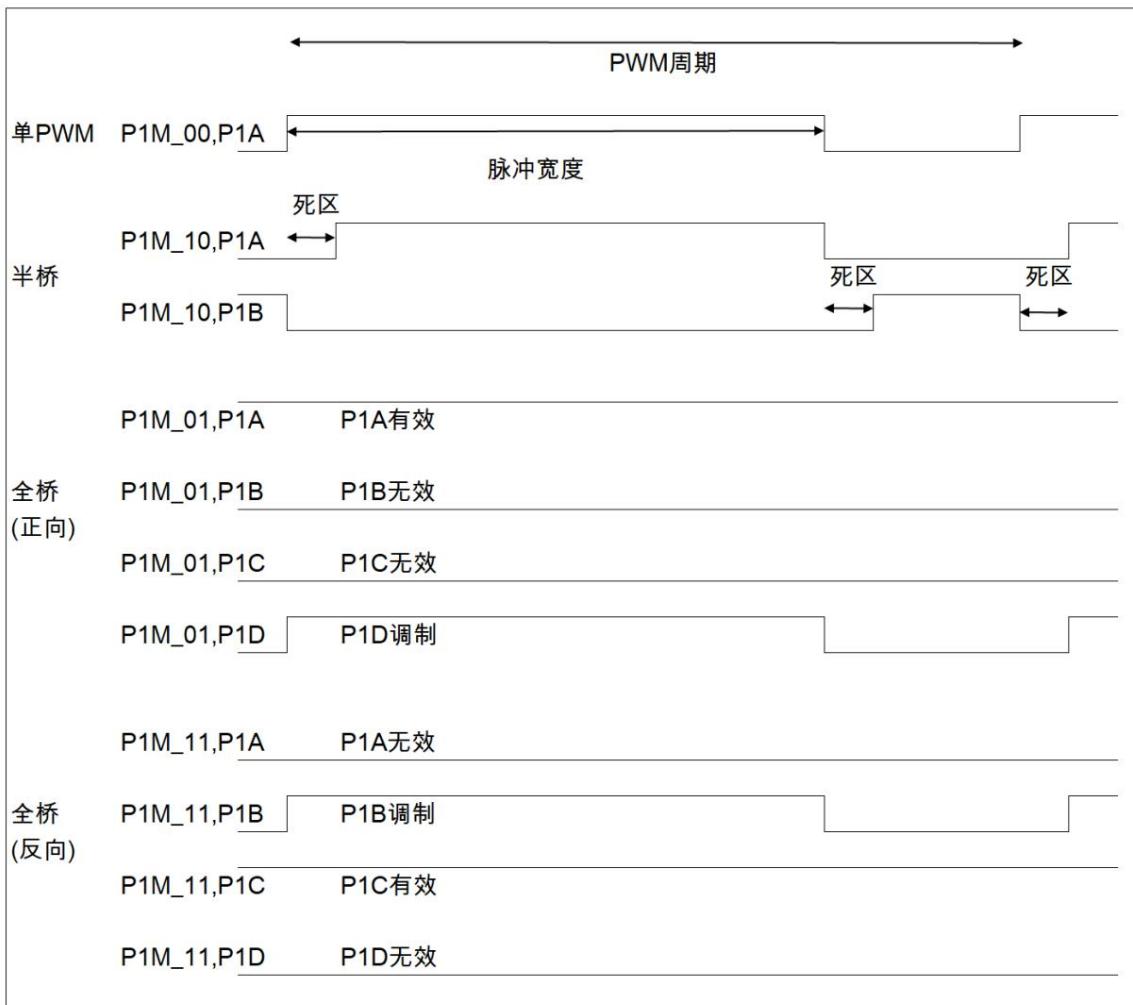


Figure 10-4 Schematic diagram of PWM output relationship (P1A~P1D active high)

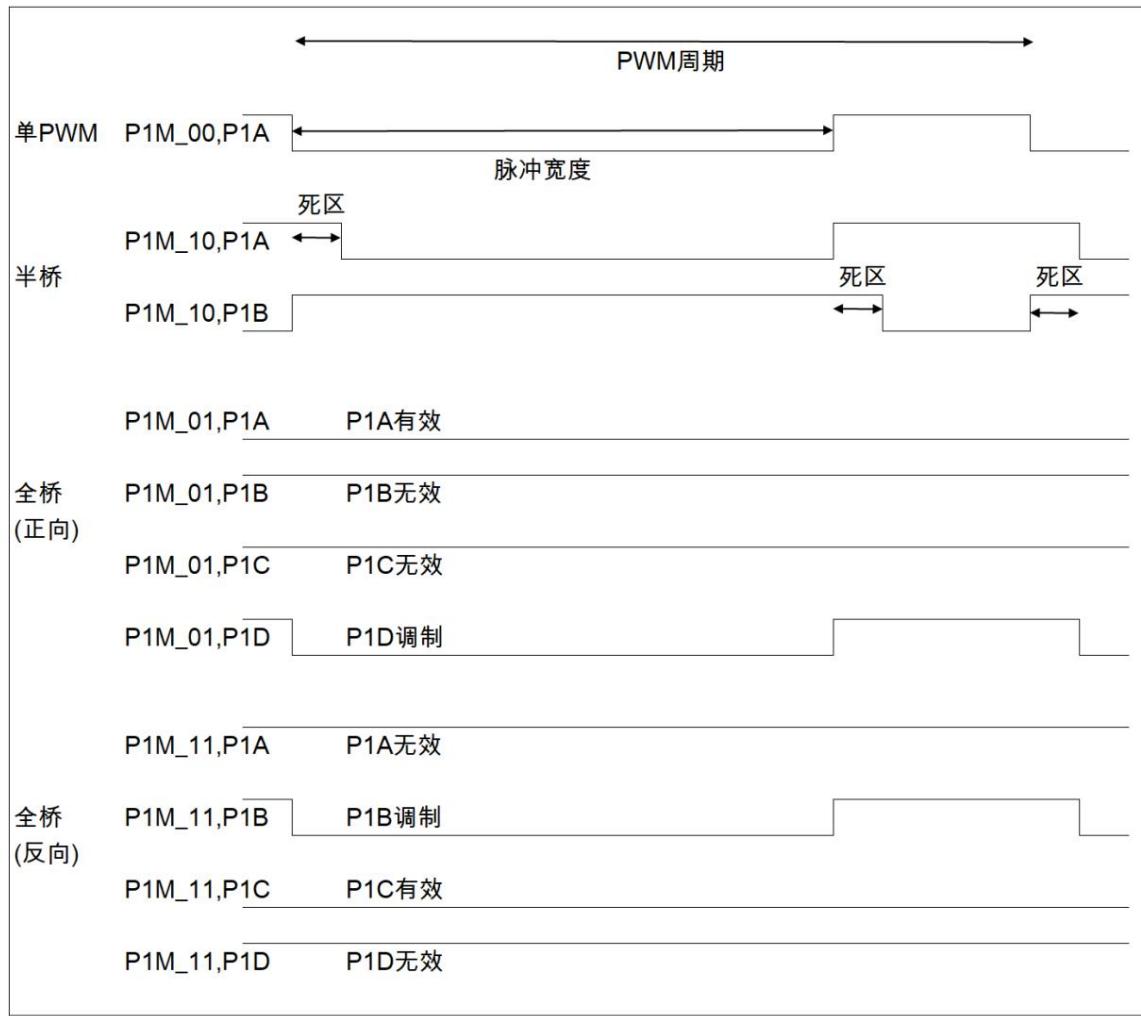


Figure 10-5 Schematic diagram of PWM output relationship (P1A~P1D active low)

Single **PWM** — 1 PWM channel P1A.

Half -Bridge **PWM** - 2 complementary PWM channels P1A and P1B with dead-time control. Dead time (see "PDC") should be set appropriately to Avoid shoot-through current when multiple power switches are turned on and off at the same time. In addition, through external 4* NMOS, or 2*PMOS plus 2*NMOS to drive the full bridge circuit. Application examples are shown in Figure 10-6, Figure 10-7 and Figure 10-8.

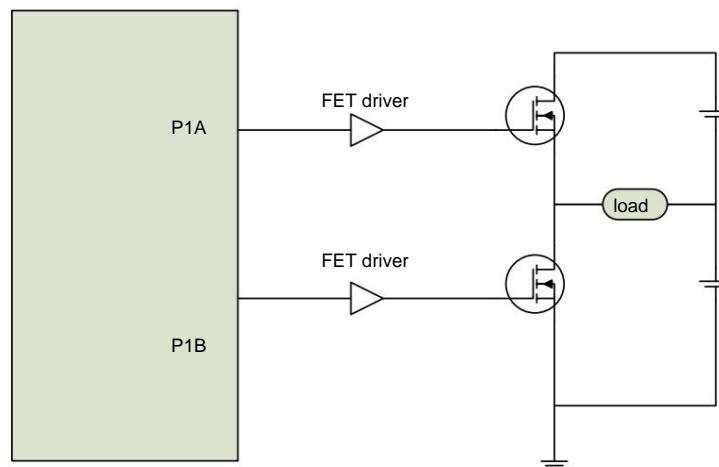


Figure 10-6 Standard half-bridge circuit (push-pull, P1A~P1B active high)

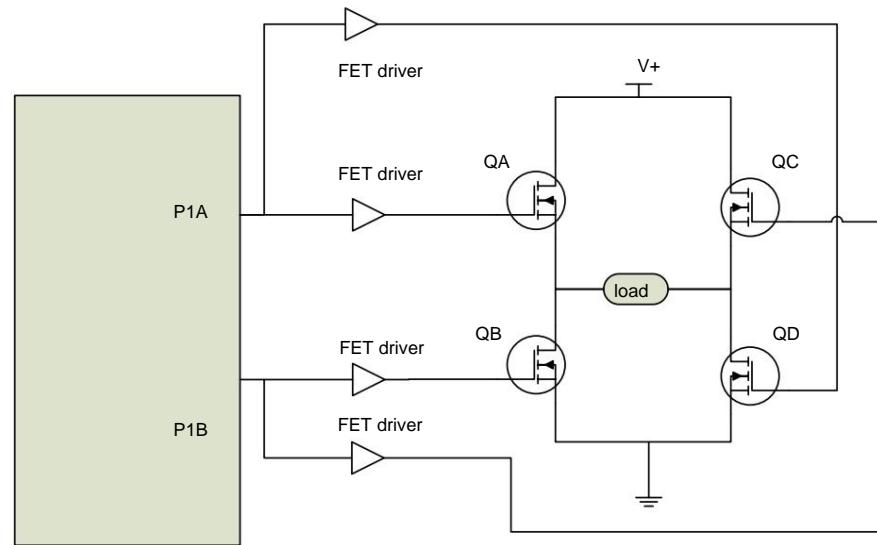


Figure 10-7 Half-bridge output driving full-bridge circuit (4NMOS, P1A–P1B active high)

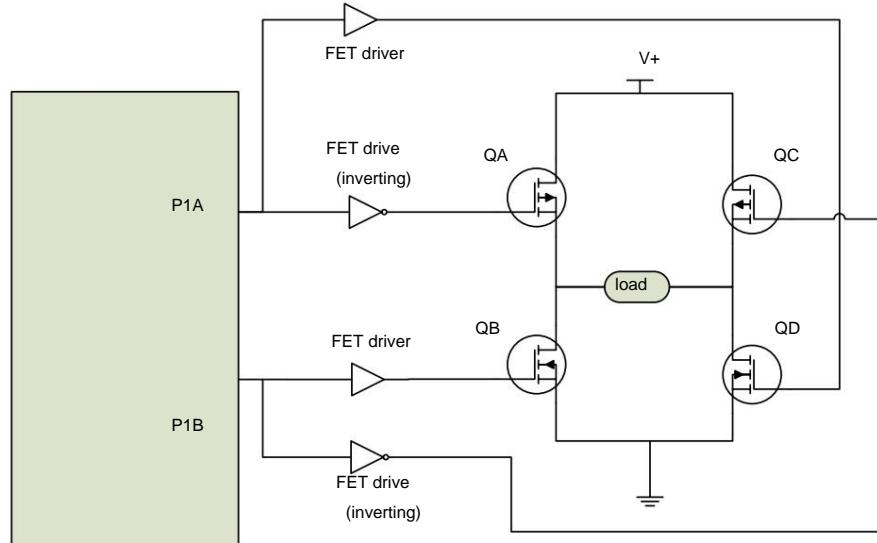


Figure 10-8 Half-bridge output driving full-bridge circuit (2PMOS+2NMOS, P1A–P1B active high)

Full-Bridge PWM (Forward, Reverse) — 4 PWM channels P1A, P1B, P1C, P1D. An application example is shown in Figure 10-9.

In full-bridge mode, software can switch forward/reverse by writing to the P1M register at any time of the PWM cycle, the PWM module will

The cycle changes direction. When changing direction, the P1B and P1D modulation waveforms will have a $4 \cdot TT2CK$ delay. The application example is shown in Figure 10-10, Input

The output waveform is shown in Figure 10-11.

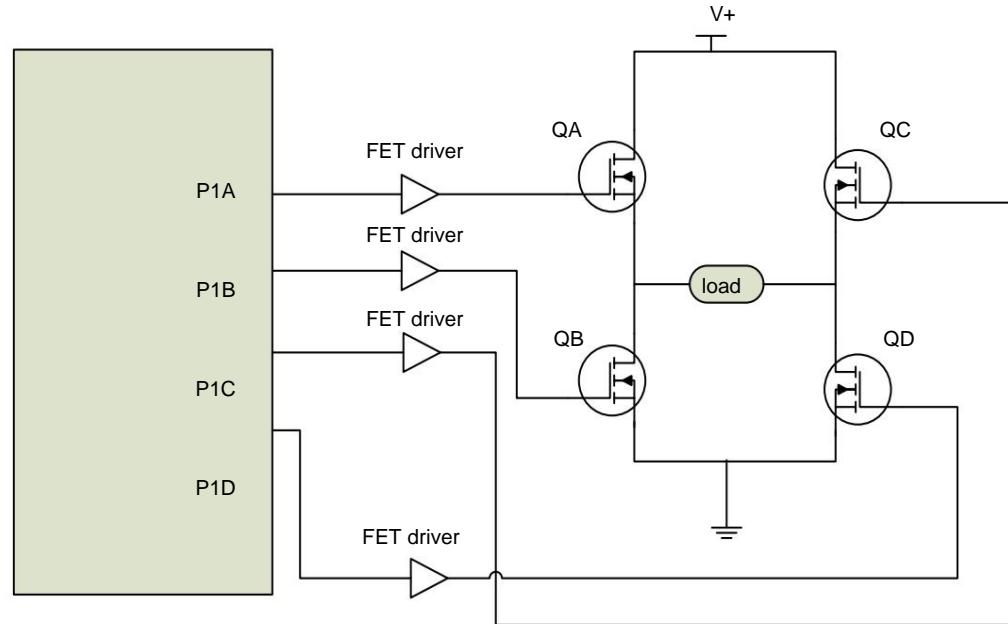


Figure 10-9 Full-bridge application example (4NMOS, P1A~P1D active high)

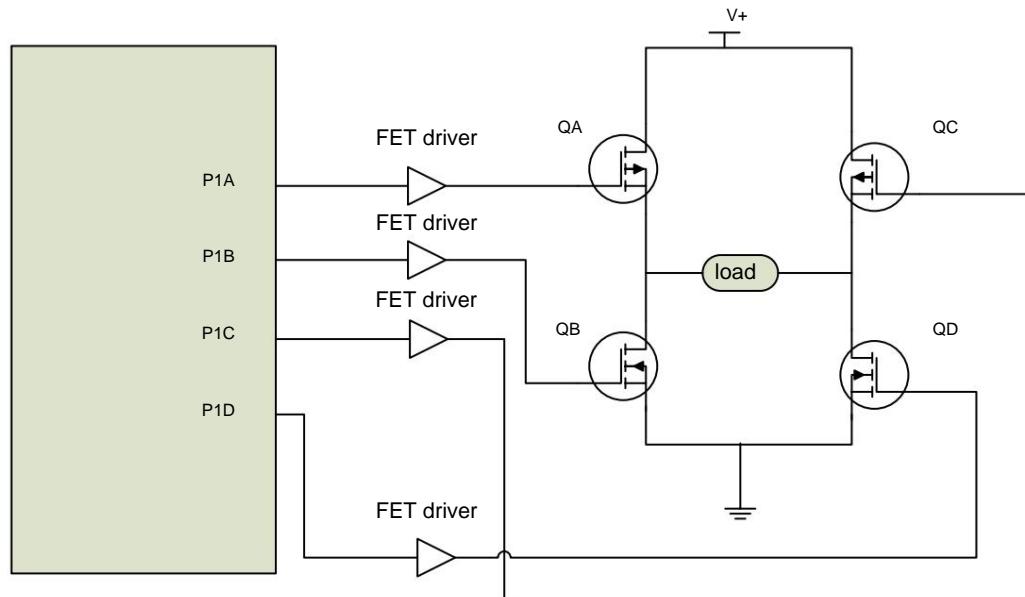


Figure 10-10 Full-bridge application example (2 PMOS+2NMOS, P1A and P1C active low, P1B and P1D active high)

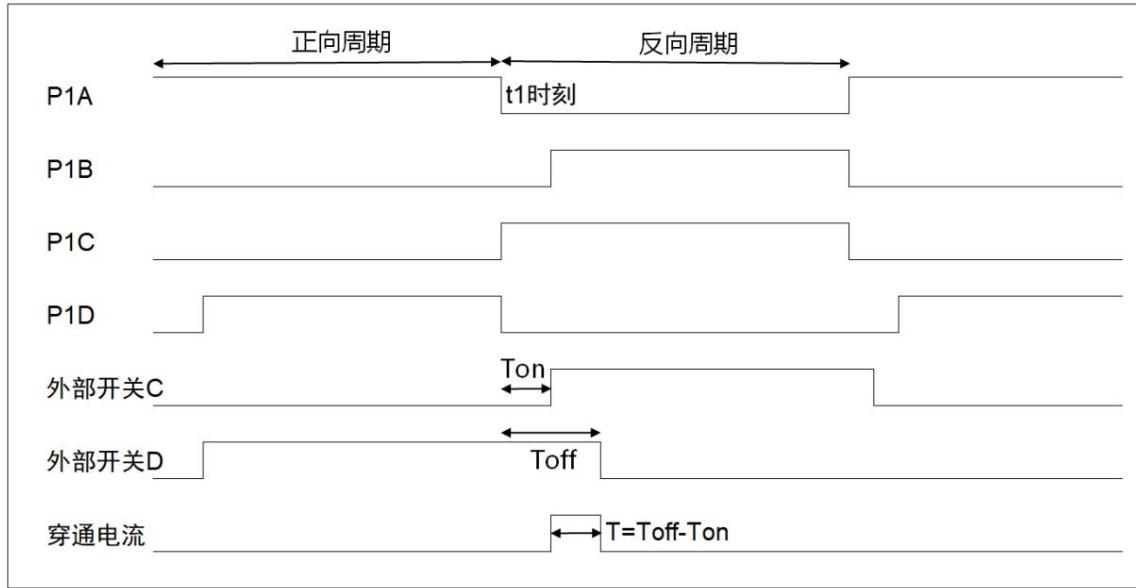


Figure 10-11 Full-bridge PWM output waveform (P1A and P1C are active low, P1B and P1D are active high)

There is no dead-time delay in full-bridge mode. In general, the modulation output also does not require dead-time delay. However, when the following two conditions are met at the same time, special attention should be paid:

1. When the duty cycle is close to or reaches 100%, the PWM output direction changes; 2.

The turn-off time of the power switch (including the power device and the driver circuit) is greater than the turn-on time;

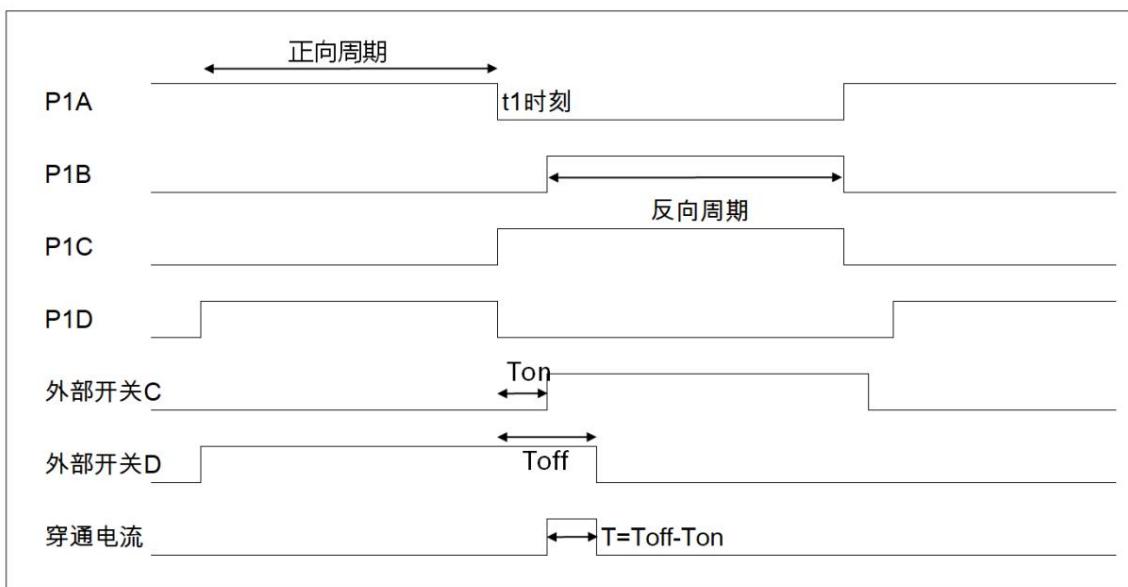


Figure 10-12 Example of PWM direction change when the duty cycle is close to 100% (P1A-P1D are active high)

As shown in [Figure 10-12](#), when the duty cycle of P1D is close to 100%, the PWM switches from forward to reverse. At time t1, the P1A and P1D outputs become inactive, and the P1C output becomes active. And since the off time (Toff) of the power device is greater than the on time (Ton), the punch-through current will flow through the power device QC and QD (as shown in Figure 10-9) for the duration "T (Toff-Ton)". The same will happen to power devices QA and QB when the PWM direction is switched from reverse to forward. Two methods of eliminating punch-through current are as follows:

1. Decrease the PWM duty cycle before changing direction.
2. Use switch drivers with off-time less than on-time.

10.4.4 PWM auto-shutdown and auto-restart

Enhanced PWM supports auto-shutdown and auto-restart (see "PRSEN"). When an external shutdown event occurs, the PWM will stop outputting. The automatic shutdown source (refer to "ECCPAS[2:0]") is as follows:

- Comparator 1 output (C1OUT) goes high
- Comparator 2 output (C2OUT) goes high
- Comparator 1/2 output (CxOUT) goes high
- INT pin voltage is low

- INT pin voltage is low, or Comparator 1 output (C1OUT) goes high • INT pin voltage is low, or

Comparator 2 output (C2OUT) goes high • INT pin voltage is low, or Comparator 1/2 Output (CxOUT) goes high

When a shutdown event occurs, the following happens:

1. ECCPASE is set. ECCPASE will remain set until cleared by software or until an auto-restart occurs.

2. The PWM output pins are placed in a preset state (refer to "PSSAC", "PSSBD"):

ÿ High output

ÿ Output low ÿ Tri-

state (high impedance state)

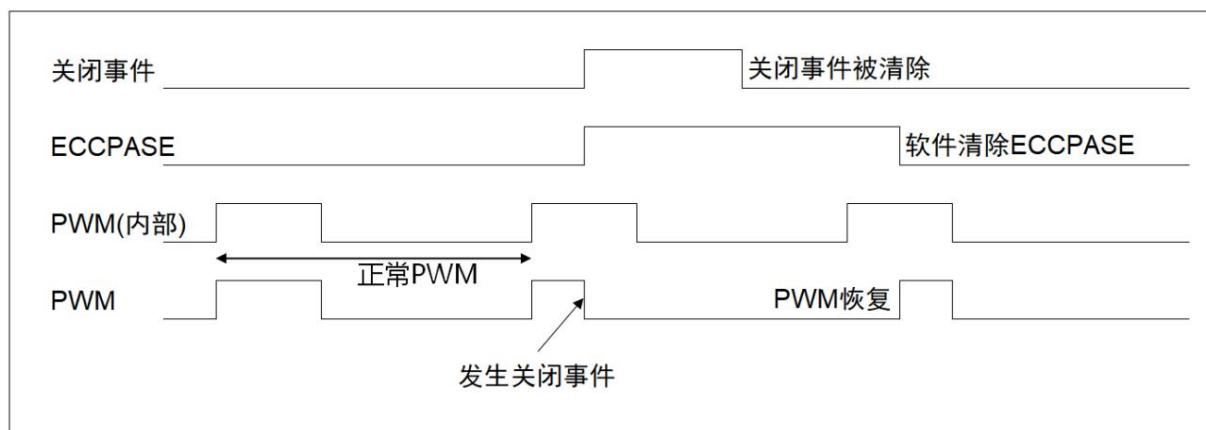


Figure 10-13 When PWM is automatically shut down, it is not restarted automatically

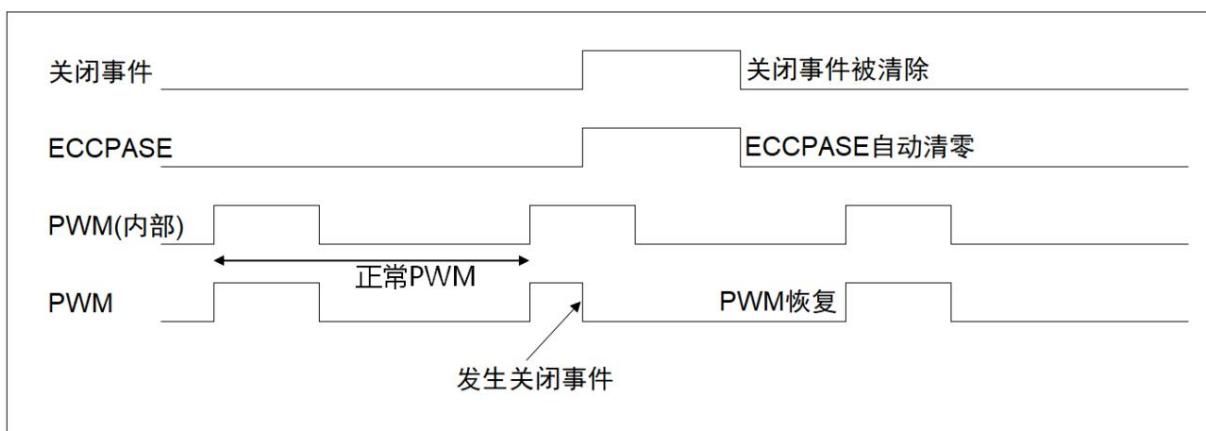


Figure 10-14 Automatic restart when PWM is automatically turned off

Note:

1. The auto-shutdown event is based on a level signal, not an edge. The auto-off condition is maintained as long as the level remains the same.
2. When the auto-shutdown condition is valid, the PWM stops output but the Timer2 count continues to run, when the auto-shutdown condition is cleared, PWM will resume output immediately.

3. ECCPASE will remain set and cannot be cleared by software until the auto-shutdown condition is cleared.

4. When the auto-shutdown condition is cleared:

 In automatic restart mode (PRSEN=1), ECCPASE will be automatically cleared by hardware, and the PWM output signal will restart automatically.

 In non-auto-restart mode (PRSEN=0), ECCPASE must be cleared by software to restart PWM output.

5. The shutdown state is indicated by the ECCPASE (Auto Shutdown Event Status) bit in the ECCPAS register. If ECCPASE = 0, PWM

The pin works normally, if ECCPASE = 1, the PWM output is turned off.

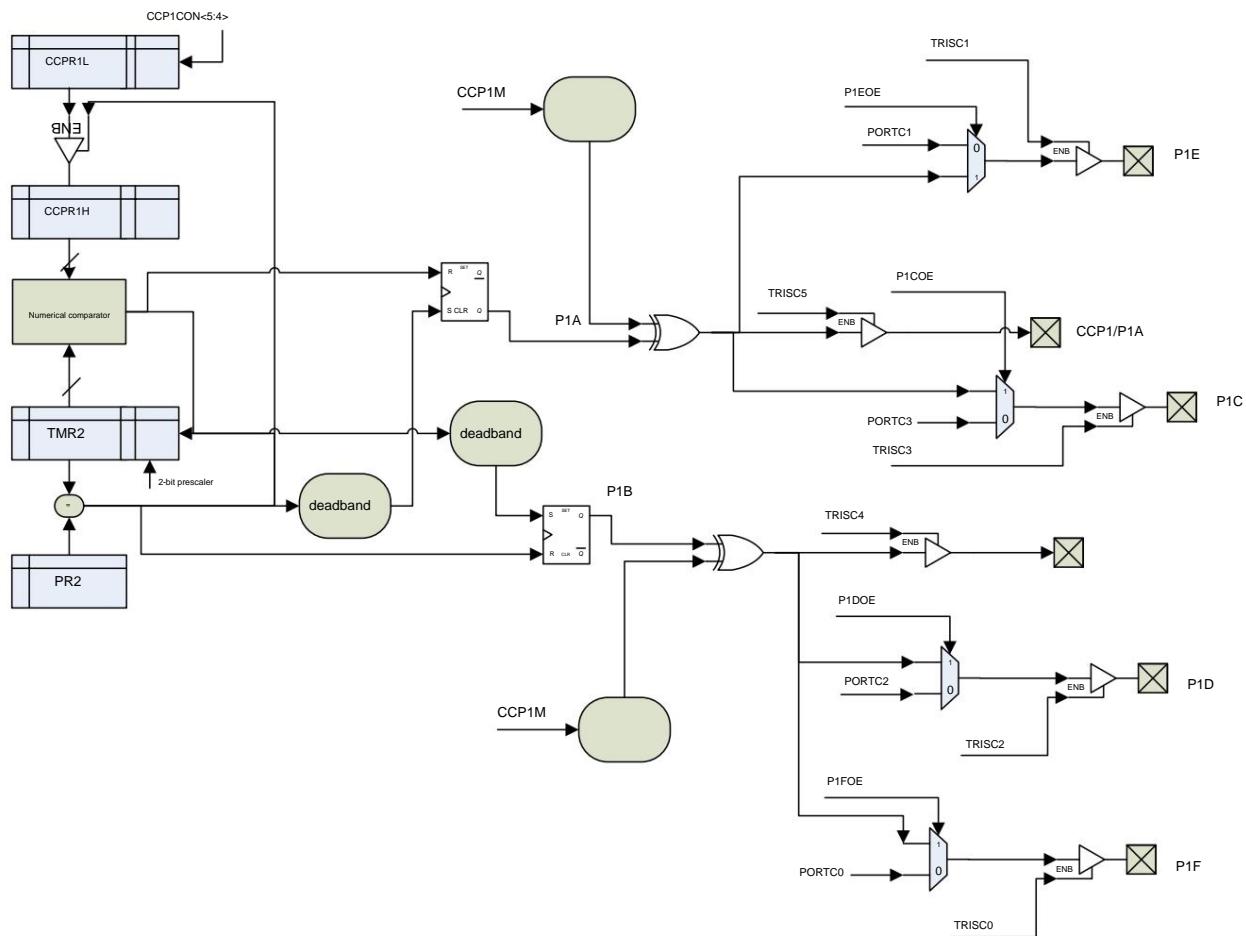
10.4.5 PWM auxiliary function

Figure 10-15 Principle block diagram of PWM auxiliary function

When the enhanced PWM works in half-bridge mode, the following auxiliary functions can be realized by setting the PWM1AUX register:

- At the same time, there can be up to 3 pairs of complementary outputs with dead-time control (when P1xOE=1): P1A, P1B, P1C, P1D, P1E, P1F;
- Single pulse mode (when P1OS=1, and P1xOE=1): After outputting PWM signal once, P1xOE is automatically cleared, PWM output

The output is

automatically closed; •The output polarity is optional (see CCP1M);

Note:

1. P1A and P1B are the first pair of half-bridge PWM outputs with dead time, and the other two pairs of P1C and P1D, P1E and P1F and the first pair

The waveforms are the same, as shown in Figure [10-16](#);

2. In single-pulse mode, after outputting a pulse waveform, P1xOE is automatically cleared, but the PWM counter keeps running. If software sets P1xOE (x=A~F) to 1 again, in the next PWM cycle, PWM pin P1x (x=A~F) will output a pulse waveform again, as shown in Figure [10-17](#).

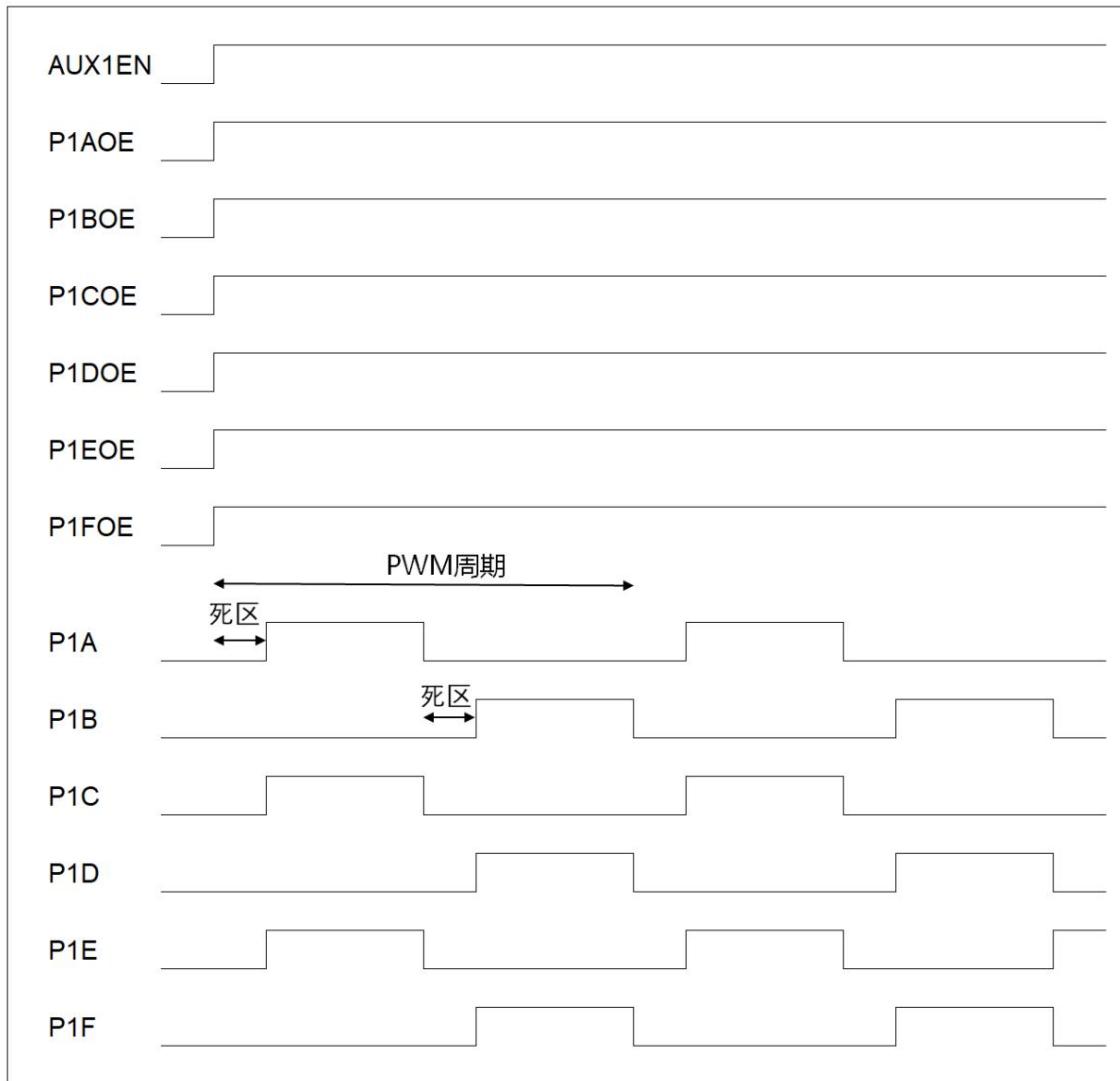


Figure 10-16 3 pairs of PWM outputs (auxiliary function)

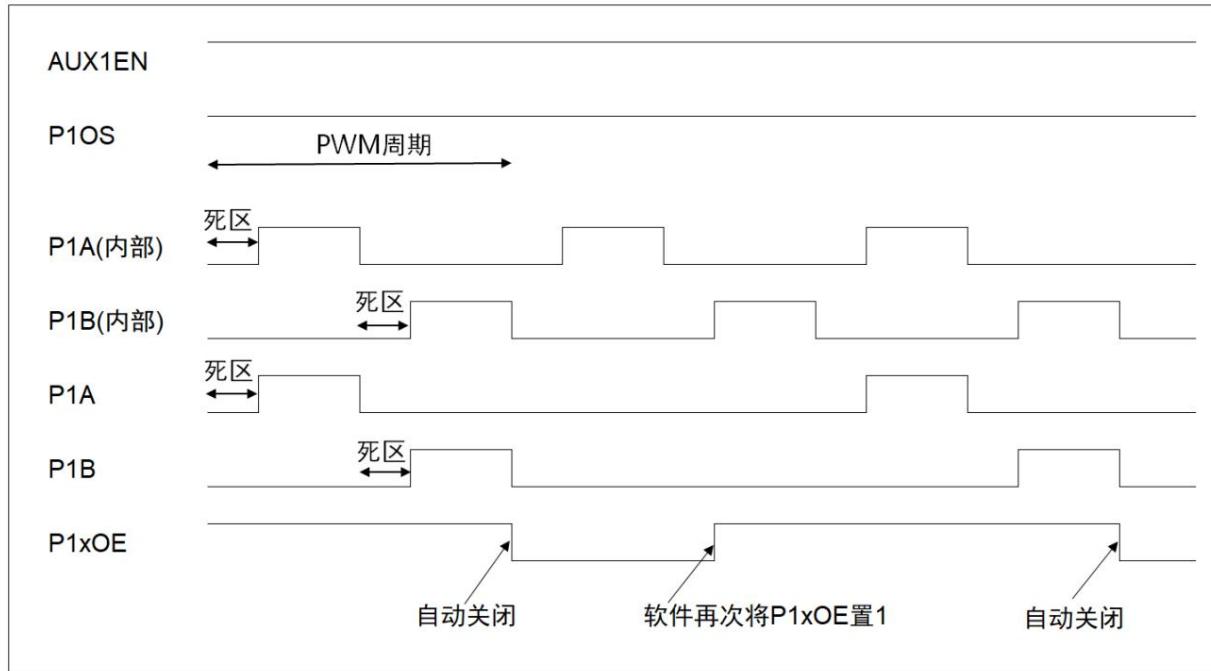


Figure 10-17 PWM single pulse output (auxiliary function)

10.4.6 PWM configuration steps

1. Configure the relevant PWM pins as inputs (TRISx=1), and an appropriate pull-up/pull-down resistor must be connected to the hardware circuit to turn off the power.
switch;

2. Set the PWM period (refer to "PR2"); 3. Configure

the ECCP module for PWM mode and select the output mode and polarity (refer to "P1M", "CCP1M"); 4. Set the PWM duty cycle (refer to "CCPR1L", "DC1B"); 5. Configure Timer2:

- a. Clear the TMR2IF interrupt flag bit; b. Set the
Timer2 prescaler (refer to "T2CKPS"); c. Select the Timer2 clock
source (refer to "T2CKSRC"); d. Enable Timer2 (refer to "TMR2ON");

6. After waiting 1 PWM cycle, enable the PWM output:

- a. Wait for Timer2 to overflow (TMR2IF is set to 1); b. If
necessary, enable auxiliary functions in half-bridge mode (refer to "AUX1EN", "P1OS", "P1xOE"); c. Configure the relevant
PWM pins as inputs (TRISx=0);

Note:

1. When PWM output, it is not recommended to change the output polarity to avoid damage to the application circuit.

2. To stop the PWM output, you cannot simply turn off the ECCP mode (CCP1M=0), because the I/O is still in the
Output status, and its output value is indeterminate. The two methods to stop PWM output are as follows:

- a. Configure the relevant PWM pins as inputs (TRISx=1) and connect with appropriate pull-up/pull-down resistors. b. Set
ECCPASE to 1, and ECCPAS[2:0]=000, make ECCP output in off state.

11. Data EEPROM (DATA EEPROM)

The FT61F02x integrates a 256 x 8-bit non-volatile DATA EEPROM storage area on-chip and is independent of the main program area. This data store. The typical erase and write cycles of the storage area can be up to 1 million times. Read/write access can be performed through instructions, and the unit that can be read or written at a time is 1 byte (8-bit), and there is no page mode (page mode). Erase/Program implements hardware self-timing without software polling to save limited code space between. Therefore, write operations can run in the background without affecting the CPU to execute other instructions, and even enter the SLEEP state. A read operation requires 1 instruction clock cycles, while the time required for a write operation is TWRITE-EEPROM (2 ~ 4 ms). The chip has a built-in charge pump, so no external high voltage, the EEPROM area can be erased and programmed. The corresponding interrupt flag bit EEIF will be set when the write operation is complete.

Sequential READ or sequential WRITE is not supported, so each read/write must update the corresponding site.

As long as VDD ≥ VPOR, the CPU can run at 8 MHz / 2T, even as low as around 1.5V at high temperatures. The voltage required to write DATA EEPROM (VDD-WRITE) is higher. The minimum VDD-WRITE for operating temperature grade 2 and grade 1 is 1.9V and 2.2V. Reading DATA EEPROM does not have this minimum voltage limit (see VDD-READ).

11.1 Summary of DATA EEPROM related registers

| name | state | Register address | reset value |
|-------|---|------------------|--------------------------|
| EEDAT | DATA EEPROM data | EEDAT[7:0] 0x9A | RW 0000 0000 |
| EEADR | DATA EEPROM address | EEADR[7:0] 0x9B | RW 0000 0000 |
| WR | <u>DATA EEPROM write enable (bit 3)</u> 111 = enable, reset to 000 when done (other) = off | EECON1[5] | RW 00 0x9C |
| | <u>DATA EEPROM write enable (bit 2)</u> | EECON1[4] | |
| | <u>DATA EEPROM write error flag</u> 1 = Abort (MCLR or WDT reset occurred) 0 = normal completion | EECON1[3] | |
| | <u>DATA EEPROM write enable (bit 1)</u> | EECON1[2] | |
| | <u>DATA EEPROM read control bits</u> 1 = Enable (hold for 4 SysClk cycles, then clear) 0 = off | EECON1[0] | |
| | <u>DATA EEPROM write control bits</u> 1 = Initiate a write or write in progress (reset to 0 when complete) 0 = done | EECON2[0] 0x9D | |

Table 11-1 EEPROM related user control registers

| name | state | | Register address | reset value |
|-----------|--|---|---------------------------------|------------------------|
| GIE | global interrupt | 1 = enabled (PEIE, EEIE applicable) 0 = global shutdown <u> </u> (wake up is not affected) | INTCON[7] 0x0B 0x8B 0x10B | RW _y 0 |
| LIKE THIS | Peripheral total interrupt | 1 = Enabled (for EEIE) 0 = off (no wakeup) | INTCON[6] | RW _y 0 |
| THIS | EEPROM write complete interrupt | 1 = enable 0 = off (no wakeup) | PIE1 [7] | 0x8C RW _y 0 |
| EEIF | EEPROM write complete interrupt flag bit | 1 = Yes (latched) 0 = No <u> </u> | PIR1[7] | 0x0C RW _y 0 |

Table 11-2 EEPROM Interrupt Enable and Status Bits

11.2 Write DATA EEPROM

1. Set "GIE=0";
2. Determine GIE, if "GIE = 1", repeat step (1);
3. Write the target address into EEADR;
4. Write the target data to EEDAT;
5. Set "WREN3, WREN2, WREN1" = "1, 1, 1" and keep this setting throughout the programming process;
6. "WR = 1" must be set immediately to start writing (otherwise it will be aborted);
7. After programming (please refer to TWRITE-EEPROM for programming time) , "WR" and "WREN3, WREN2, WREN1" will be cleared automatically
0_y

Example program:

```

BCR INTCON, GIE
BTSC INTCON, GIE
LUMP $-2
BANKSEL EEADR
LDWI 55H
STR EEADR ; The address 0x55
EEDAT STR ; is the data as 0x55
LDWI 34H
STR EECON1 ; WREN3/2/1      set at the same time 1
BSR EECON2, 0 ; start write
BSR INTCON, GIE ; GIE set 1

```

Note:

1. Reading the Data EEPROM while programming is in progress will result in an incorrect read result.
2. If any bit of WREN3, WREN2 or WREN1 is cleared to 0 before programming is completed, the EEIF flag needs to be cleared before the next programming bit.



11.3 Read DATA EEPROM

Write the target address to the EEADR register, then initiate a read ("RD = 1"). On the next instruction clock cycle, the EEPROM data is written into the EEDAT register. The EEDAT register will hold this value until the next read or write operation.

The sample program to read DATA EEPROM is as follows:

```
BANKSEL EEADR  
LDWI dest_addr  
STR EEADR  
BSR EECON1, RD  
LDR EEDAT, W ; At this point, the data can be read by the instruction
```

11.4 Auto Erase Function

The process of writing data to a byte consists of two steps: first erasing the byte, and then programming the byte. The erase operation erases all bits of a byte into "1", while programming operations selectively write individual bits as "0". This chip has built-in automatic erasing function, that is, it will automatically execute erasing before programming. remove operation.

Programming FF data multiple times actually erases the corresponding byte multiple times. However, multiple programming of non-FF data actually only program the corresponding byte once. process, because it is automatically erased before each programming.

12. 10-bit A/D Converter (ANALOG TO DIGITAL CONVERTER, ADC)

The ADC module can convert analog input signals into 10-bit digital signals. ADCs can operate at different clock speeds and up to

True 10-bit accuracy at 1 MHz clock speed (ie 60 kHz sample rate, 16 μ s/sample).

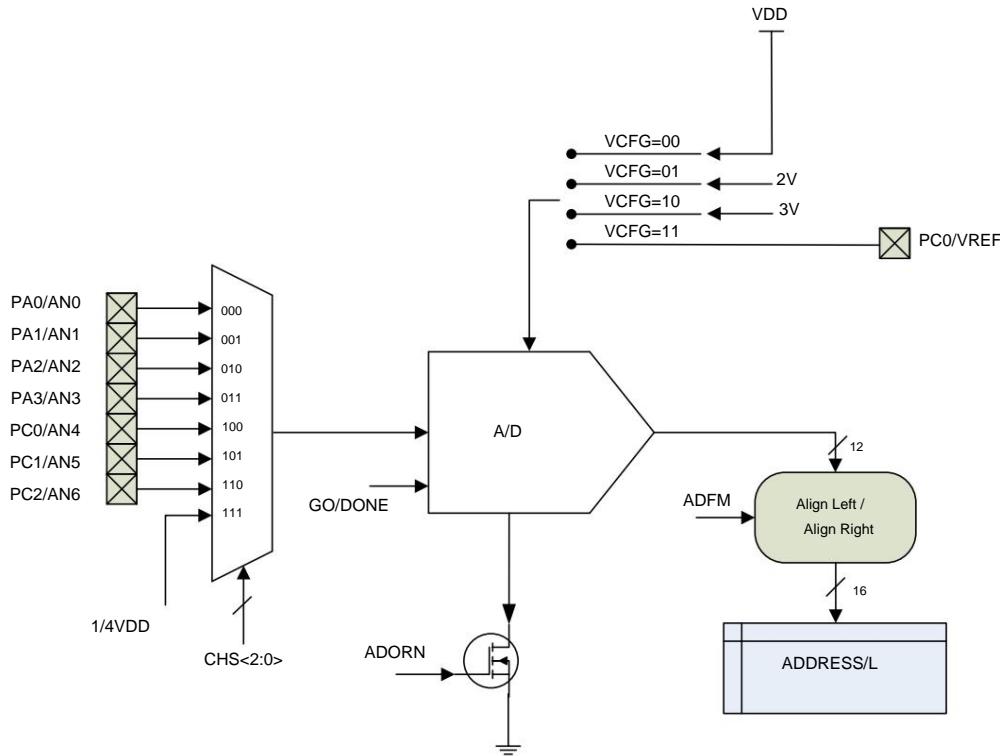


Figure 12-1 Block diagram of ADC structure

The analog input signal can be selected as one of 7 I/O (ANx) channels or 1 internal channel (Internal 1/4VDD). ADC by instruction or ECCP special event trigger fires. A delay can be added between triggering and ADC sampling.

When the ADC conversion is complete, the corresponding interrupt flag bit is set and can trigger an interrupt and/or wake-up from sleep.

ADC reference voltage (VADC_yREF) can be selected by command as VDD, one of 2 internal reference voltages (2V, 3V), or input externally through I/O reference voltage.

ADC does not require calibration. In addition, the ADC conversion process runs in the background, and the CPU can execute other instructions during the conversion.

If the ADC needs to keep running under SLEEP, its conversion clock source should be selected as LIRC (no frequency division), otherwise it will enter SLEEP mode. The ADC module will automatically shut down after the mode.

When the ADC is configured as hardware trigger (ECCP special event trigger), GO/DONE is directly set by the hardware trigger event and starts the A/D conversion, software set GO/DONE will be ignored (see Section 10 Enhanced Capture/Compare/PWM).

In high sample rate applications, there are 3 time points to be aware of when using the ADC:

1. The moment when the selected channel starts sampling.
2. Time to end sampling. Immediately before the sample-and-hold circuit is disconnected, the voltage value on the selected channel is used to measure the conversion.
3. Data conversion completion time.

12.1 Summary of ADC related registers

| name | state | Register address | reset value | |
|-----------------|--|------------------|---------------|-------------------|
| GIE | global interrupt 1 = enabled (PEIE, ADCIE applicable) 0 = <u>global shutdown</u> (wake up is not affected) | INTCON[7] 0x0B | 0x8B 0x10B | RW ^y 0 |
| PEIE peripheral | general interrupt 1 = Enabled (for ADCIE) 0 = off (<u>no wakeup</u>) | INTCON[6] | | |
| CHICKEN | ADC conversion complete interrupt 1 = enabled 0 = off (<u>no wakeup</u>) | PIE2[1] | 0x8D | RW ^y 0 |
| ADIF | ADC conversion complete interrupt flag 1 = Yes (latched) 0 = No | PIR2[1] | 0x0D | RW ^y 0 |

Table 12-1 ADC Interrupt Enable and Status Bits

| name | state | Register address | reset value |
|---------|--|----------------------------------|------------------------------|
| ADDRESS | <u>ADC Conversion Result Low Significant Bit (LSB)</u> ADFM=0: ADRESL[7:6] = lower 2 bits (the rest are "0") ADFM=1: ADRESL[7:0] = lower 8 bits | ADDRESS[7:0] 0x9E | RW ^y xxxx xxxx |
| ADRESH | <u>ADC conversion result most significant bit (MSB)</u> ADFM=0: ADRESH[7:0] = upper 8 bits ADFM=1: ADRESH[1:0] = upper 2 bits (the rest are "0") | ADDRESS[7:0] 0x1E | RW ^y xxxx xxxx |
| ADFM | <u>A/D conversion result format (refer to "ADRESH")</u> 1 = right-aligned 0 = left-aligned | ADCON0[7] | RW ^y 0 |
| VCFG | <u>VADC^yREF (reference voltage)</u> 00 = VDD 01 = Internal 2V (*) Only valid when ANSEL[4] = 1; | ADCON0[6:5] | RW ^y 00 |
| CHS | <u>ADC analog input channel</u> 000 = AN0 001 = AN1 010 = AN2 011 = AN3 (*) Only valid when ANSEL[7] = 1; | ADCON0[4:2] | 0x1F RW ^y 000 |
| GO/DONE | <u>ADC conversion start and status bits</u> 1 = A/D conversion initiated by software or ECCP (automatically cleared after conversion is complete) 0 = conversion done/not in progress | ADCON0[1] | |
| ADORN | 1 = ADC is enabled 0 = <u>ADC is off (no current consumption)</u> | ADCON0[0] | RW ^y 0 |
| TWO | <u>ADC frequency division clock source selection</u> 1 = LIRC 0 = <u>Sysclk</u> | ADCON1[7] 0x9F RW ^y 0 | |

| name | state | | | Register address | reset value | | |
|------------------------------------|---|---|---|------------------|-------------|--|--|
| <u>ADC conversion clock source</u> | | | | | | | |
| ADCS | TWO = 0 TSEL = 2T 000 = Sysclk/2 001 = Sysclk/8 010 = Sysclk/32 100 = Sysclk/4 101 = Sysclk/16 110 = Sysclk/64 x11 = LIRC (*) | TWO = 1 TSEL = 4T 000 = Sysclk/4 001 = Sysclk/16 010 = Sysclk/64 100 = Sysclk/8 101 = Sysclk/32 110 = Sysclk/128 x11 = LIRC (*) | TSEL = 2T/4T 000 = LIRC/2 001 = LIRC/8 010 = LIRC/32 100 = LIRC/4 101 = LIRC/16 110 = LIRC/64 x11 = LIRC (*) | ADCON1[6:4] | RWþ000 | | |
| | (*) LIRC = 32kHz or 256kHz, depending on the value of LFMOD | | | | | | |
| | 1 = turn off pull-up/pull-down, and digital input (only for 8 ADC channels) | | | | | | |
| | 0 = <u>(no action)</u> | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

Table 12-2 ADC related user registers

| name | address | bit 7 | | bit 6 | bit 5 | bit 4 | bit 3 | Bit 2 | bit 1 | bit 0 | Reset value | |
|--------------|---------|-------|--|--|----------|-------|-------|--------------|-----------|-------|-------------|--|
| ADDRESS 0x9E | | | | A/D conversion result low significant bit | | | | | | | | |
| ADDRESS 0x1E | | | | A/D conversion result high significant bit | | | | | | | | |
| ADCON0 0x1F | ADFM | | | VCFG<1:0> | CHS<2:0> | | | GO/DONE ADON | 0000 0000 | | | |
| ADCON1 0x9F | | TWO | | ADCS<2:0> | | | | | | | | |

Table 12-3 ADC related user register address

12.2 ADC Configuration

Configuring the ADC includes the following settings (when changing the configuration, set ADON=0 to turn off A/D conversion or external trigger):

- ÿ Channel selection
- ÿ ADC reference voltage
- ÿ ADC conversion clock source
- ÿ Conversion result format
- ÿ Trigger source
- ÿ Response (interrupt setting)

Channel Selection – The input channel is selected by the CHS register, which is connected to the sample and hold circuit for ADC conversion. The corresponding I/O needs to be set TRISx = 1 and ANSELx = 1 to configure as analog input.

ADC Reference Voltage (VADCÿREF) – The ADC measures the input analog voltage relative to the positive reference voltage VREF, the negative reference voltage is always GND, the positive reference voltage can be selected as:

- ÿ VDD
- ÿ Internal reference voltage 2V
- ÿ Internal reference voltage 3V

External reference voltage (VREF is PC0)

ADC Conversion Clock Selection – The ADC can be commanded to select 13 clock frequencies (see "ADCS", Table 12-2):

- SysClk/N (TSEL = 2T) or SysClk/2N (TSEL = 4T) or LIRC when DIVS = 0; N = 2, 4, 8, 16, 32, 64
- LIRC/N at DIVS = 1; N = 1, 2, 4, 8, 16, 32, 64
- LIRC (256 kHz or 32 kHz, see "LFMOD", Table 6-2)

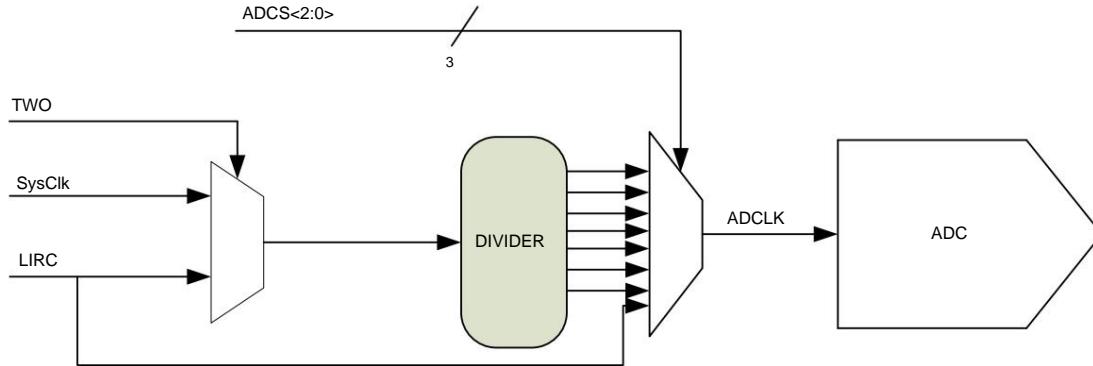


Figure 12-2 ADC Clock Configuration

Conversion Result Format – A/D conversion results can be stored in either left-justified or right-justified formats (see "ADFM", Table 12-2).

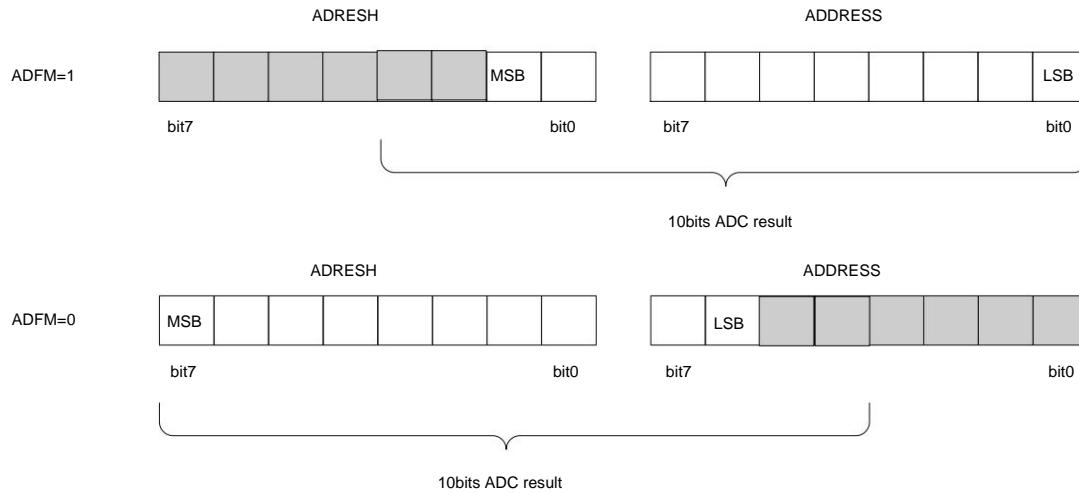


Figure 12-3 ADC conversion result format

12.2.1 ADC Triggering

ADC conversions can be triggered by an instruction (GO/DONE = 1) or an ECCP special event trigger. GO/DONE starts immediately after being set by the instruction A/D conversion. If triggered by an ECCP special event, a special event trigger occurs when TMR1H/L matches CCP1H/L output, automatically start an ADC conversion.

Note: New trigger conditions are ignored until the ADC conversion is complete.

12.2.2 ADC aborted conversion

Sometimes ADC conversions need to be aborted, for example to start a new ADC sampling.

- ÿ The ADC can be stopped by software setting GO/DONE = 0.
- ÿ When the special event trigger is selected, the ADC must be aborted by turning off the ADC module (ADON = 0).
- ÿ When ADC conversion is aborted, ADRESH and ADRESL will not be updated, but keep the previous conversion result value.
- ÿ When the system is reset, since the corresponding registers are reset, the ADC will be aborted and the ADC module will be turned off.

12.2.3 Interrupts

The interrupt flag bit ADCIF is set when the ADC conversion is complete. Whether to trigger an interrupt and/or wake up from sleep depends on the corresponding interrupt enable Control bits (GIE, PEIE, ADCIE).

12.3 ADC Sample and Hold Time

The sample and hold time , TACQ, must be long enough to ensure that the internal ADC voltage is stable within 0.01% of the input channel voltage to achieve 10bit precision (0.097%). The relationship between the sampling time and the external series resistance is as follows (Table 12-4):

$$TACQ > 0.09 \times (R + 1) \text{ ys}; R \text{ is in k} \Omega.$$

When the sampling time TACQ is 2ÿs, the external series resistance must be $\geq 21 \text{ k} \Omega$. If a larger series resistor is used, the TACQ will increase proportionally add. Junction leakage current limits the maximum allowable series resistance value. For a junction leakage current of 5nA, add a series resistance of 50 kÿ to This produces a voltage drop of 0.25mV (0.0125% of the 2V reference voltage). However, when the temperature exceeds 100°C, the junction leakage current will increase significantly. because Therefore, the smaller the series resistance, the better.

| Series resistance | TACQ |
|-------------------------------|-----------------------|
| value $> 50 \text{ k} \Omega$ | (Not recommended) |
| 43 kÿ | $\geq 4.0 \text{ ys}$ |
| 21 kÿ | $\geq 2.0 \text{ ys}$ |
| $< 21 \text{ k} \Omega$ | $\geq 2.0 \text{ ys}$ |

Table 12-4 Correspondence between different external series resistors and the shortest TACQ

The sample and hold time is the time that the internal ADC observes the voltage of the input channel.

Start of sample hold time = after channel switching (refer to "CHS") or after ADC stabilization (refer to TST), whichever is longer.

End of sample and hold time = TSysClk / N 1 after CCP1 trigger or software GO/DONE set (N = 2 for 2T, 4 for 4T)

At the same time, the sample and hold circuit is disconnected.

Sample point = the moment before the sample-and-hold circuit is turned off.

Data conversion begins after sampling is turned off, and the conversion process takes 13.5 x TAD to 14.5 x TAD. Therefore a trigger from CCP1 or software It takes 13.5 x TAD to 14.5 x TAD 2 to complete the data conversion after GO/DONE is set . After the data conversion is completed, the sample and hold power The circuit is closed again to start the next sampling cycle, and the A/D conversion can only be started again after waiting for a long enough sampling time TACQ.

12.4 ADC Minimum Sampling Time

TAD is the clock period of the ADC. Minimum time required for complete 10-bit conversion:

$$TACQ + 14.5 \times TAD$$

¹ TSysClk / N = 0.125ÿs (16M/2T) or 0.250ÿs (16M/4T);

² The process of GO set to 1 to sample off (TSysClk / N time) occurs at the same time as the process of synchronization after GO set (2 – 3 x TAD time);

The highest conversion sample rate that guarantees true 10-bit accuracy is approximately 60 kHz (~16 μ s/sample).

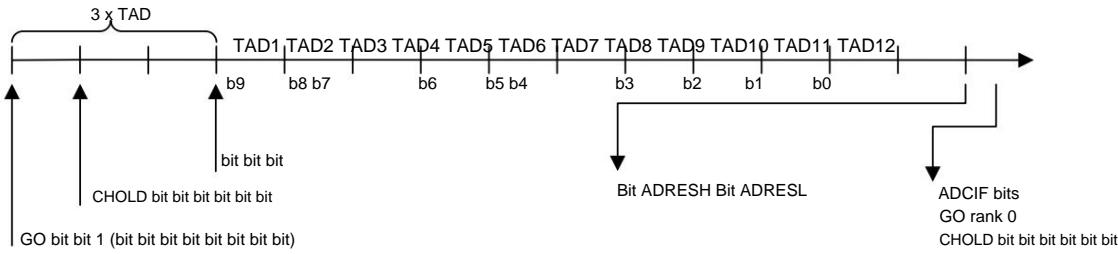


Figure 12-4 Analog-to-digital conversion TAD cycle

12.5 Example of ADC Conversion Steps

Set up ADC:

1. Configure the ports:

- Set TRISx = 1 to disable pin output drive
- Set ANSELx = 1 to disable digital input, weak pull-up and weak pull-down

2. Configure the ADC module:

- Select the ADC conversion clock source
- Select ADC reference voltage
- Select ADC trigger condition: GO/DONE or CCP1 special event trigger
- Select the conversion result format

3. Configure ADC interrupt (optional):

- Enable ADC interrupt
- Enable peripheral total interrupt
- Turn off the global interrupt (enable if the interrupt service routine needs to be executed)

4. Turn on the ADC module. Then wait for the desired ADC stabilization time TST (~15 μ s), when VADC \bar{y} REF selects the internal reference voltage, then

Wait for the internal reference voltage stabilization time TVRINT (see "TVRINT", chapter 18.7) and the TST time, whichever is longer, i.e.

$$\max(TVRINT \bar{y} TST)$$

At this point, the ADC is ready to sample the different channels. When sampling an input channel:

- The ADC input is selected as the channel to be measured (refer to "CHS").
- If necessary, clear the ADC conversion complete interrupt flag.
- There is a minimum requirement for the sampling time TACQ. The TACQ must be long enough to ensure that the internal ADC input capacitor is fully charged to the voltage of the input channel.
Within 0.01% error. In addition, depending on the trigger type, a certain amount of time is required after switching channels or after the ADC is stable (whichever is longer).
Delay retriggering.
 - For software triggering, additional TACQ time is required.
 - For ECCP special event trigger, additional TACQ time is also required.

5. After waiting the desired delay, set GO/DONE by the instruction, or wait for the CCP1 special event trigger to automatically set GO/DONE to Start A/D conversion.
6. Wait for the ADC conversion to complete by:
 - a. Query the GO/DONE bit
 - b. Wait for ADC interrupt (when interrupt is enabled)
7. Read the ADC conversion result.
8. If necessary, clear the ADC conversion complete interrupt flag bit.

Note:

1. Although GO/DONE and ADON are in the same register (ADCON0), they should not be set at the same time.

2. The configuration cannot be changed during ADC conversion or while waiting for a special event to trigger. Changes are recommended when ADON = 0.

The following is an example of ADC program (input sampling channel is PA0, ADC clock is LIRC):

```

BANKSEL ADCON1
LDWI B'00110000' ; ADC LIRC clock
STR ADCON1

TRISA BANKSEL
BSR TRISA, 0 ; Set PA0 to input
BANKSEL ANSEL
BSR ANSEL, 0 ; Set PA0 to analog

BANKING ADCONO
LDWI B'10000001' ; Right justify,
STR ADCONO ; VDD, Vref, AN0, On

LCALL StableTime ; ADC stable time
LCALL SampleTime ; Acquisition delay, TACQ

BSR ADCON0, GO ; Start conversion
BTSC ADCON0, GO ; Conversion done?
LUMP $-1 ; No, test again

BANKSEL ADRESH;
LDR ADRESH, W ; Read upper 2 bits
STR RESULTHI ; Store in SRAM space

BANKSEL ADDRESS;
LDR ADRESL, W ; Read lower 8 bits
STR RESULTLO ; Store in SRAM space

```

13. Comparator

The FT61F02x integrates two analog comparators on-chip, which can be used to compare the magnitudes of two analog input voltage values and output the comparison results. Compare

Comparator C1/C2 can be configured as a variety of input and output connection modes, the polarity of the output result can be selected, and can be output to the I/O pin (PA2/PC4), the internal

A partially programmable reference voltage CVREF can also be used for the comparator input. Comparator C2 can also be used in conjunction with Timer1.

The comparator can keep running in SLEEP (when CM₀₀₀ or 111). When the output state of the comparator C1/C2 changes, the corresponding bit will be set interrupt flags and can trigger interrupts and/or wake-up from sleep.

13.1 Summary of Comparator Related Registers

| name | Status | Register address | reset value | |
|------------------|---|------------------|-------------|-------------------|
| C2OUT | <u>Comparator C2 Output Result</u> when C2INV = 0: 1 = VIN+ > VIN 0 = VIN+ < VIN <u>When C2INV = 1:</u> 1 = VIN+ < VIN 0 = VIN+ > VIN | CMCON0[7] | | RW ₀ |
| C1OUT | <u>Comparator C1 output result</u> When C1INV = 0: 1 = VIN+ > VIN 0 = VIN+ < VIN <u>When C1INV = 1:</u> 1 = VIN+ < VIN 0 = VIN+ > VIN 1 = | CMCON0[6] | | RW ₀ |
| C2INV Comparator | <u>C2 output polarity</u> Reverse 0 = normal | CMCON0[5] | | RW ₀ |
| C1INV Comparator | <u>C1 output polarity</u> 1 = reverse 0 = normal | CMCON0[4] | | RW ₀ |
| CIS | <u>Comparator Input Switching</u> When CM = 001: 1 = C1 VIN- is connected to C1IN+(PA0) 0 = C1 VIN- to C1IN- (PA1) <u>When CM = 010:</u> 1 = C1 VIN- is connected to C1IN+(PA0), C2 VIN- is connected to C2IN+(PC0) 0 = C1 VIN- to C1IN- (PA1), C2 VIN- to C2IN- (PC1) | CMCON0[3] | 0x19 | RW ₀ |
| CM | <u>Comparator mode</u> 000 = off (CxIN is an analog IO pin) 001 = 2 comparators, common reference, 3 inputs 010 = 2 comparators, common internal reference voltage CVREF, 4 inputs 011 = 2 comparators, common reference, 2 inputs 100 = 2 independent comparators 101 = 1 independent comparator 110 = 2 comparators with output, common reference, 2 inputs 111 = off (CxIN pins are digital IO pins) | CMCON0[2:0] | | RW ₀₀₀ |
| VREN | <u>Internal reference voltage CVREF</u> 1 = enable 0 = off (no current consumption) | VRCON[7] | 0x99 | RW ₀ |

| name | state | Register address | reset value | |
|--------|---|------------------|-------------|-------------------|
| VRR | <u>CVREF range</u> 1 = low level = high | VRCON[5] | | RW \ddot{y} 0 |
| VR | <u>CVREF value</u> When VRR = 1: CVREF = (VR<3:0>/24)*VDD When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32)*VDD | VRCON[3:0] | | RW \ddot{y} 000 |
| T1GSS | <u>Timer1 gate source</u> 1 = T1G pin (configured as digital input) 0 = output of comparator C2 | CMCON1[1] | | RW-1 |
| C2SYNC | <u>Comparator C2 output synchronization control</u> 1 = Synchronize to falling edge of Timer1 clock 0 = Asynchronous output | CMCON1[0] | 0X1A | RW-0 |

Table 13-1 Comparator related user registers

| name | state | Register address | reset value | |
|-----------|---|------------------|-----------------------|-----------------|
| GIE | global interrupt 1 = enabled (for PEIE, C2IE, C1IE) 0 = global shutdown (wake up is not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW \ddot{y} 0 |
| LIKE THIS | Peripheral total interrupt 1 = Enabled (C2IE, C1IE apply) 0 = off (no wakeup) | INTCON[6] | | RW \ddot{y} 0 |
| C2IE | Comparator 2 output change interrupt 1 = enabled 0 = off (no wakeup) | PIE1 [4] | 0x8C | RW \ddot{y} 0 |
| C2IF | Comparator 2 output change interrupt flag bit 1 = Yes (latched) 0 = No | PIR1[4] | 0x0C | RW \ddot{y} 0 |
| C1IE | Comparator 1 output change interrupt 1 = enable 0 = off (no wakeup) | PIE1 [3] | 0x8C | RW \ddot{y} 0 |
| C1IF | Comparator 1 output change interrupt flag bit 1 = Yes (latched) 0 = No | PIR1[3] | 0x0C | RW \ddot{y} 0 |

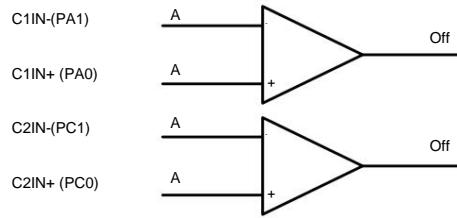
Table 13-2 Comparator Interrupt Enable and Status Bits

13.2 Comparator Configuration

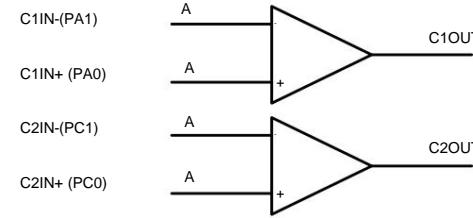
There are 8 configuration modes for Comparator 1/2, as shown in Figure 13-1 . It is necessary to turn off the comparator and its interrupt first, and then switch the comparator 1/2 input and output.

out mode.

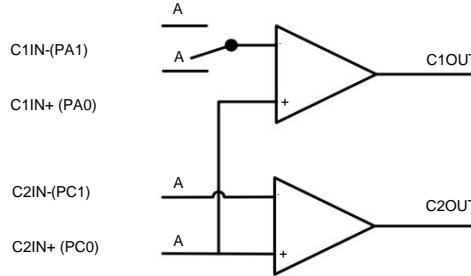
Comparator reset (power-on reset value)
CM<2:0> = 000



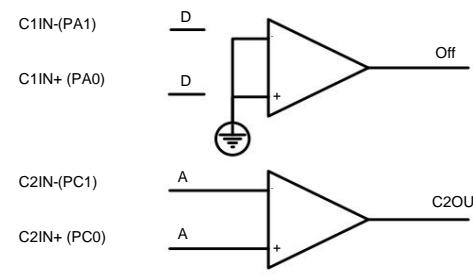
2 independent comparators
CM<2:0> = 100



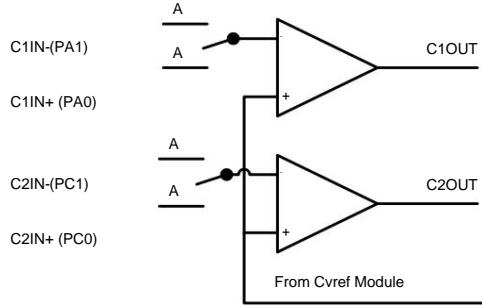
2 comparators, common reference terminal, 3 inputs
CM<2:0> = 001



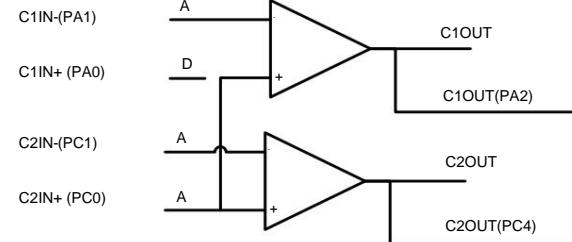
1 independent comparator
CM<2:0> = 101



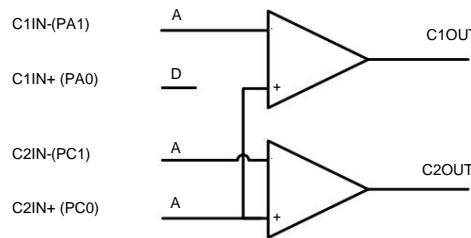
2 comparators, common internal reference voltage CVREF, 4 inputs
CM<2:0> = 010



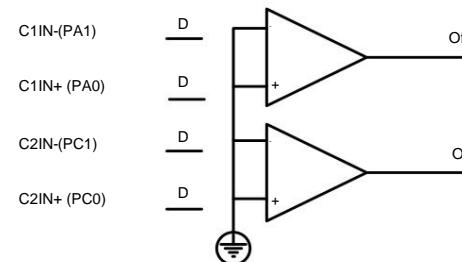
2 comparators with output, common reference terminal, 2 inputs
CM<2:0> = 110



2 comparators, common reference terminal, 2 inputs
CM<2:0> = 011



Comparator off (lowest power mode)
CM<2:0> = 111



Note:

A: Analog input (ANSELx = 1), port read as '0'

D: digital input

Figure 13-1 Comparator 1/2 Input and Output Mode

Analog Input Port - The corresponding I/O should be configured as an analog input by setting TRISx = 1 and ANSELx = 1.

The analog input ports are multiplexed with I/O pins, these pins have reverse protection diodes between VDD and GND, and the input voltage is prohibited from deviate. This protection range is above 0.6V, otherwise the diode will conduct and cause latch-up. External series resistance needs to be <10 k Ω . Additionally, if the analog input Components such as external capacitors or Zener diodes on the input pins should not generate leakage current, otherwise the results may be inaccurate.

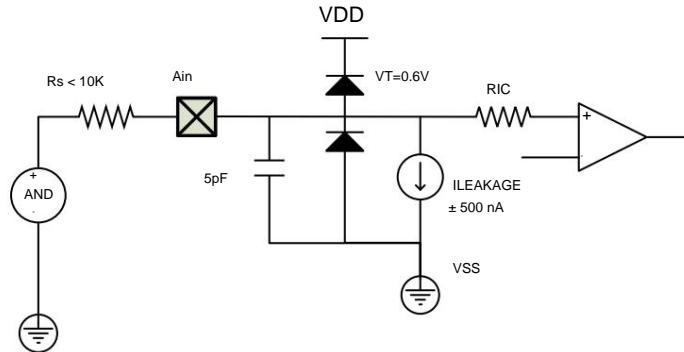


Figure 13-2 Comparator Analog Input Model

Comparison Result Output—The comparison result can be output to I/O pin PA2/PC4 (CM = 110), the corresponding I/O needs to set TRISx = 0 to enable Can output drive circuit.

Comparator Reaction Time - When a new reference voltage is input or the input source changes, the time it takes for the comparator to output a valid level is the reaction time time. In addition, when the reference voltage changes, a certain settling time is also required. Please refer to [Section 18.8 for details](#).

Note: When the comparator module is enabled, a stabilization time of about 1 μ s is required. During this period, the comparator output is invalid, and the interrupt should be turned off to avoid false alarms. trigger.

Programmable Voltage Reference CVREF — One of the comparator inputs can be selected as an internal programmable voltage reference , CVREF (CM = 010), reference voltage Independent enable (refer to “VREN”) to output 16 levels of high range and 16 levels of low range, proportional to VDD.

High Voltage Range (VRR = 0): $CVREF = VDD/4 + (VR<3:0>/32)*VDD$

Low Voltage Range (VRR = 1): $CVREF = (VR<3:0>/24)*VDD$

As shown in [Figure 13-3](#) , the full scale of GND to VDD cannot be achieved due to the construction of the module. CVREF can be output by the following configuration The output voltage is clamped to GND, where the comparator can be used for zero-crossing detection without consuming additional CVREF block current.

```
BCR VRCON,VREN ;closure CVREF
CLRR VRCON ;VR<3:0> = 0000
BSR VRCON,VRR ; CVREF low level range
```

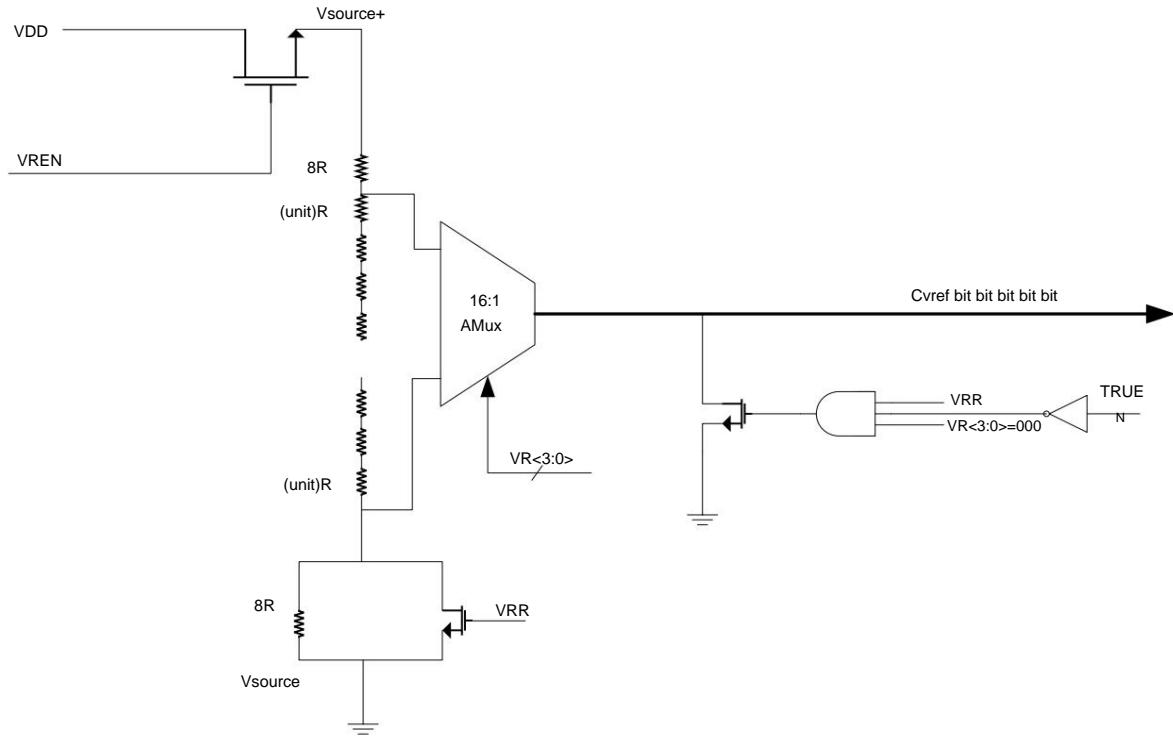


Figure 13-3 Comparator Voltage Reference Block Diagram

13.2.1 Comparator Interrupts

When the output state of the comparator 1/2 changes, the corresponding interrupt flag bit CxIF will be set. The software needs to save the state of the output bit first, that is, read CxOUT, to judge the actual change. Whether to trigger an interrupt and/or wake up from sleep depends on the corresponding enable control bits (GIE, LIKE, C1IE, C2IE).

Note:

1. A read or write to CMCON0 will end the mismatch condition and clear the interrupt.
2. The interrupt flag bit, CxIF, must be cleared by software. Before clearing, CMCON0 must be read to clear the mismatch condition. In addition, software can Set CxIF to 1 to simulate the occurrence of an interrupt.
3. If CxOUT happens to change when CMCON0 is read, the CxIF flag may not be set high.

13.2.2 Comparator 2 Gate Timer1

When Timer1's gate source is selected as the output of comparator C2, it can be used to time the duration or interval of an analog event. For details, please refer to See Section 7.3.3 "Timer1 Gating Mode".

14. Voltage Regulator (VREG)

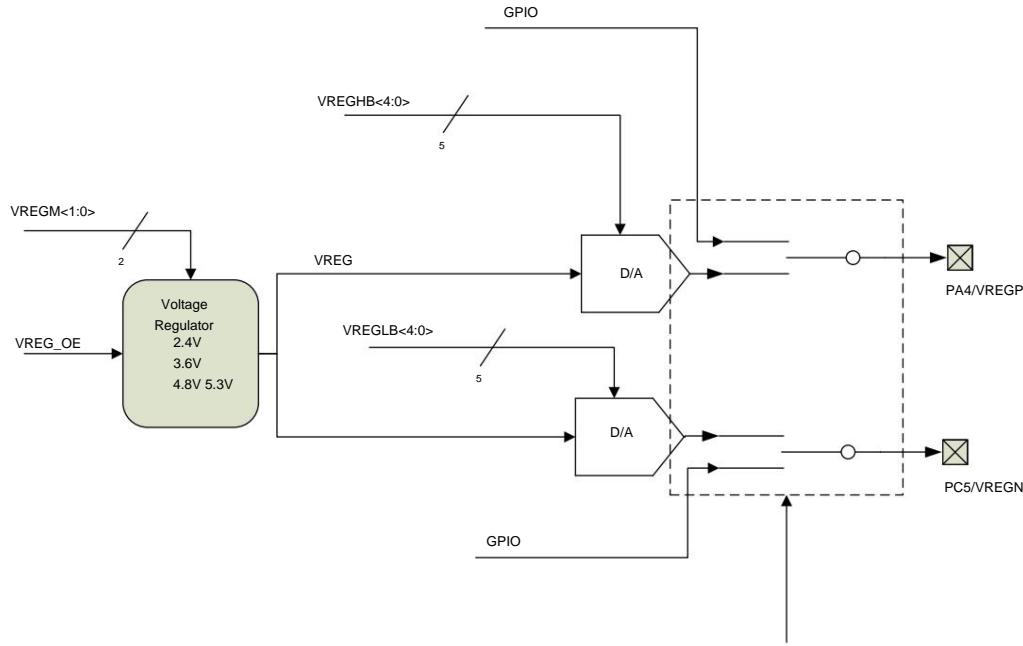


Figure 14-1 The principle block diagram of the output of the voltage regulator

The FT61F02X has two built-in voltage regulator outputs, each of which can output up to 32 voltage levels. The output voltage formula is as follows:

$$\text{Formula 14-1 } VOUT = VREG * (VREGHB + 1) / 32 \quad (\text{VREGP, PA4 voltage output})$$

$$\text{Formula 14-2 } VOUT = VREG * (VREGLB + 1) / 32 \quad (\text{VREGN, PC5 voltage output})$$

14.1 Summary of Regulator Output Related Registers

| name | State | Register address | reset value |
|---------|---|------------------|-------------|
| VREG_OE | <u>Regulator Output</u> 1 = Enable (PA4 and PC5 output regulator voltage) 0 = off (PA4 and PC5 are normal IO) | MSCKCON[6] 0x1B | RW\0 |
| VREGM | <u>Regulator Voltage VREG Select Bits</u> 00 = 2.4V 01 = 3.6V 10 = 4.8V 11 = 5.3V | VCON1[6:5] | 0x108 |
| VREGHB | <u>High Voltage Range (PA4) Output Voltage</u> $VOUT = VREG * (VREGHB + 1) / 32$ | VCON1[4:0] | RW\0000 |
| VREGLB | <u>Low Voltage Range (PC5) Output Voltage</u> $VOUT = VREG * (VREGLB + 1) / 32$ | VCON2[4:0] 0x109 | RW\0000 |

Table 14-1 Regulator Output Related Registers

15. Memory area read/write protection

The program area (PROM) and the data EEPROM area (DROM) can be configured for global read protection. The selection configuration is made by the IDE interface.

| name | Function | default |
|------|--------------------------------|---------|
| CPB | PROM full area read protection | closure |

Table 15-1 Memory Area Read/Write Protection Initialization Configuration Register

16. INSTRUCTION SET

| assembly syntax | Function | operation | status bit |
|---|---|--------------------------------------|------------|
| NOP | No | None | NONE |
| SLEEP | operation Enter SLEEP | 0 ÿ WDT; Stop OSC 0 ÿ WDT | /PF, /TF |
| CLRWD | mode Clear watchdog | | /PF, /TF |
| LJUMP N | (feed the dog) Unconditional | N ÿ PC | NONE |
| LCALL N | jump Call subroutine | N ÿ PC; PC + 1 ÿ Stack | NONE |
| RARELY | Return from interrupt | Stack ÿ PC; 1 ÿ GIE | NONE |
| RIGHT | Return from subroutine | Stack ÿ PC | NONE |
| BCR R, b | Clear the b bit of register R to 0 | 0 ÿ R(b) 1 ÿ | NONE |
| BSR R, b | Set the b bit of register R to 1 Clear | R(b) 0 ÿ R | NONE |
| CLRR R | register R to 0 | | FROM |
| LDR R, d (MOVF) save R to d | | R ÿ d | FROM |
| COMR R, d | one's complement of R | /R ÿ d | FROM |
| INCR R, d | R + 1 | R + 1 ÿ d | FROM |
| INCRSZ R, d | R + 1, if the result is 0, skip | R + 1 ÿ d | NONE |
| DECR R, d | R ÿ 1 | R ÿ 1 ÿ d | FROM |
| DECRSZ R, d | R ÿ 1, skip if the result is 0 | R ÿ 1 ÿ d | NONE |
| SWAPR R, d Swap the nibble of register R R(0-3)R(4-7) ÿ d | | | NONE |
| RRR R, d | R rotate right with carry | R(0) ÿ C; R(n) ÿ R(nÿ1); C ÿ R(7); C | |
| RLR R, d | R rotate left with carry | R(7) ÿ C; R(n) ÿ R(n+1); C ÿ R(0); C | |
| BTSC R, b | Bit test, skip if the result is 0 Skip if R(b)=0 | | NONE |
| BTSS R, b | Bit test, if the result is 1 then skip Skip if R(b)=1 | | NONE |
| CLRW 0 ÿ W Save the content of W to OPTION | | | FROM |
| STTMD | | W ÿ OPTION Set I/ | NONE |
| CTLIO R | O direction control register TRISr W ÿ TRISr | | NONE |
| STR R (MOVWF) store W to R | | W ÿ R | NONE |
| ADDWR R, d W is added to R | | W + R ÿ d | C, HC, Z |
| SUBWR R, d | R minus W | R ÿ W ÿ d | C, HC, Z |
| ANDWR R, d W and R | | R & W ÿ d | FROM |
| IORWR R, d W or R | | W R ÿ d | FROM |
| XORWR R, d W XOR with R | | W ^ R ÿ d | FROM |
| LDWI I (MOVLW) store immediate data to W | | I ÿ W. | NONE |
| ANDUI I | W and immediate I | I & W ÿ W | FROM |
| IORWI I | W is ORed with immediate I | I W ÿ W | FROM |
| XORWI I | W XOR with immediate I | I ^ W ÿ W | FROM |
| ADDWI I | Add W and immediate I Add | I + W ÿ W | C, HC, Z |
| SUBWI I | immediate I to subtract W | I ÿ W ÿ W | C, HC, Z |
| RETW I | and return, store immediate I to W | Stack ÿ PC; I ÿ W | NONE |

Table 16-1 37 RISC instructions

| field | describe |
|-------------|---|
| R(F) | SFR/SRAM address |
| In | working register |
| b | 8-bit register R/bit address in RAM |
| I / Imm (k) | immediate |
| X | Don't care, value can be 0 or 1 |
| d | Destination register selection 1 = Result is placed in register R / RAM 0 = Result is placed in W |
| N | program absolute address |
| PC | program counter |
| /PF | power-down flag |
| /TF | time-out flag |
| TRISr | TRISr register, r can be A, B, C carry/borrow |
| C | |
| HC | Half-carry/half-borrow |
| FROM | 0 flag bit |

Table 16-2 Opcode Fields

| name | Status | Register address | reset value | |
|------|--|------------------|-----------------------|------------------|
| FROM | 0 Flag: The result of an arithmetic or logical operation is zero? 1 = Yes 0 = No | STATUS[2] | | RW _{jx} |
| HC | Digit Carry/ Digit Borrow (ADDWR, ADDWI, SUBWI, SUBWR): A carry or borrow from the 4th low-order bit of the result to the high-order bit? 1 = Carry, or no borrow 0 = no carry, or borrow | STATUS[1] | 0x03 0x83 0x103 | RW _{jx} |
| C | carry/borrow (ADDWR, ADDWI, SUBWI, SUBWR): result A carry or borrow occurred in the most significant bit of ? 1 = Carry, or no borrow 0 = no carry, or borrow | STATUS[0] | | RW _{jx} |

Table 16-3 Calculation Status Flag Bits

17. SPECIAL FUNCTION REGISTERS (SFR)

There are 2 special function registers (SFRs):

- Initialize configuration registers: set by the emulator interface (Integrated Development Environment, IDE);
- User registers;

17.1 Initializing Configuration Registers



Figure 17-1 Initial configuration registers set by IDE

| name | Function | |
|---|--|----------------|
| CPB | PROM full area read protection | closure |
| MCLRE External I/O reset | | closure |
| PWRTEB Power-on delay timer (PWRT), additional delay ~64ms after initial configuration is completed | | closure |
| WDTE | WDT •Enable (command cannot be disabled) •Controlled by command | SWDTEN control |
| DARK | (SWDTEN) • LP: PA7 (+) and PA6 (ÿ) connect to external low-speed crystal oscillator • XT: PA7 (+) and PA6 (ÿ) connect to external high-speed crystal oscillator • EC: PA7 (+) is connected to external clock input, PA6 is I/O • INTOSC: PA6 outputs "instruction clock", PA7 is I/O • INTOSCI0: PA7 and PA6 are I/O | INTOSCI0 |
| CSUMENB | program space checksum verification function | closure |
| TSEL | <u>Correspondence between instruction clock and system clock SysClk (2T or 4T):</u> •ÿ2 (instruction clock = SysClk/2) •ÿÿ4 (instruction clock = SysClk/4) Fail-safe clock monitor • Enable • Disable | 2 |
| FCMEN | _____ | Enable |
| IESO | <u>XT / LP two-speed clock enabled</u> • enabled • disabled | Enable |
| RDCTRL | <u>When TRISx = 0, the return value of reading the PORTx register •</u> Input latch • Output latch | output |
| LVREN | LVR •Enable •Disable •Enable in non- SLEEP mode •Control by instruction (SLVREN) | Enable |
| LVRS | 7- level VBOR voltage (V): 2.0 / 2.2 / 2.5 / 2.8 / <u>3.1</u> / 3.6 / 4.1 | 2.0 |

Table 17-1 Initialize configuration registers (set by IDE)

17.2 User Register

User registers, that is, special function registers (SFR) and SRAM are distributed in 4 banks . Since BANK3 is not implemented, it is implemented

The number of addressable registers is 384. Before accessing a register, it must first switch to the corresponding bank.

Any instruction that uses the INDF register actually accesses the location pointed to by the file select register {FSR_B8, FSR}. when

When FSR_B8 is 1 and indirect addressing is used to access SFR space, {FSR_B8, FSR} will point to BANK2.

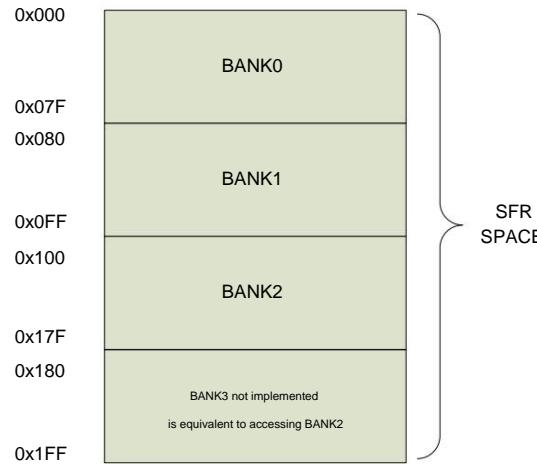


Figure 17-2 Indirect addressing

Since switching banks requires additional instructions, some commonly used SFRs are stored in 3 banks at the same time to reduce switching operations.

The register values common to these three banks are synchronized.

| address | name bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 Rese | value |
|---------------|--------------------------|---|-----------|-------|-------|-------|-------|------------|-----------|
| 0, 80, 100 | INC | Use the contents of FSR to access data memory (not a physical register) | | | | | | | xxxx xxxx |
| 2, 82, 102 | PCL | Program Counter (PC) lower 8 bits | | | | | | | 0000 0000 |
| 3, 83, 103 | STATUS FSR _{B8} | PAGE[1:0] | /TF | /PF | FROM | HC | C | 0001 1xxx | |
| 4, 84, 104 | FSR | Indirect addressing pointer register | | | | | | | xxxx xxxx |
| A, 8A, 10A | PCLATH | Program Counter (PC) Upper 5-bit Latch | | | | | | | ÿÿ0 0000 |
| B, 8B, 10B | INTCON | GIE | LIKE THIS | T0IE | NOT | PAY | T0IF | INTF | PAIF |
| 0x70 ~ 0x7F | Public BANK SRAM area | | | | | | | xxxx xxxx | |
| 0xF0 ~ 0xFF | | | | | | | | | |
| 0x170 ~ 0x17F | | | | | | | | | |

Table 17-2 Registers common to 4 banks

| address | name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | reset value | | | | | |
|-------------------|--|---|-----------|-----------------------------------|------------|---------------|------------|-------------|-----------|-------------|--|--|--|--|--|
| 0 | INC | Data memory accesses (not physical registers) using the contents of the FSR | | | | | | xxxx xxxx | | | | | | | |
| 1 | TMRO | Timer0 counter | | | | | | xxxx xxxx | | | | | | | |
| 2 | PCL | Program counter lower 8 bits | | | | | | 0000 0000 | | | | | | | |
| 3 STATUS | FSRB8 | PAGE[1:0] | | /TF | /PF | FROM | | HC | C | 0001 1xxx | | | | | |
| 4 FSR | Indirect addressing pointer register | | | | | | xxxx xxxx | | | | | | | | |
| 5 DOOR | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | xxxx xxxx | | | | | | |
| 7 PORTC | | | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | ÿÿxx xxxx | | | | | | |
| A PCLATH | | | | Program counter upper 5-bit latch | | | | | ÿÿ00 0000 | | | | | | |
| B INTCON | GIE | LIKE THIS | T0IE | NOT | PAY | T0IF | INTF | PAIF | 0000 0000 | | | | | | |
| C PIR1 | EEIF | CKMEAIF | | C2IF | C1IF | OSFIF | TMR2IF | TMR1IF 0000 | 0000 0000 | | | | | | |
| D PIR2 | | | | | | | ADIF | CCP1IF | ÿÿy0 | ÿy00 | | | | | |
| E TMR1L | Timer1[7:0] | | | | | | xxxx xxxx | | | | | | | | |
| F TMR1H | Timer1[15:8] | | | | | | xxxx xxxx | | | | | | | | |
| 10 T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | TMR1CS | TMR1ON | 0000 0000 | | | | | | |
| 11 TMR2 | TMR2 [7:0] | | | | | | 0000 0000 | | | | | | | | |
| 12 T2CON | | TOUTPS [3:0] | | | TMR2ON | T2CKPS [1:0] | | | ÿ000 0000 | | | | | | |
| 13 CCP1R1L | Capture, Compare, PWM Register 1 Lower 8 Bits | | | | | | xxxx xxxx | | | | | | | | |
| 14 CCP1R1H | Capture, compare, PWM register 1 upper 8 bits | | | | | | xxxx xxxx | | | | | | | | |
| 15 CCP1CON | P1M[1:0] | | DC1B[1:0] | | CCP1M[3:0] | | | | | 0000 0000 | | | | | |
| 16 PW1CON PRSEN | | PDC[6:0] | | | | | | 0000 0000 | | | | | | | |
| 17 ECOPAS ECCPASE | | ECCPAS [2:0] | | | PSSAC[1:0] | | PSSBD[1:0] | | | 0000 0000 | | | | | |
| 18 WDTCON | | | | | WDTPS[3:0] | | | | SWDTEN | ÿÿ00 1000 | | | | | |
| 19 CMCON0 | C2OUT | C1OUT | C2INV | C1INV | CIS | CM[2:0] | | | 0000 0000 | | | | | | |
| 1A CMCON1 | | | | | | | T1GSS | C2SYNC | ÿÿy0 | ÿy10 | | | | | |
| 1B MSCON | VREG_OE | T2CKSRC | SLVREN | | | CKMAVG | CKCNTI | | 0000 ÿ00ÿ | | | | | | |
| 1C SOSCPRL | SOSCPR [7:0] | | | | | | 1111 1111 | | | | | | | | |
| 1D SOSCPRH | | | | | | SOSCPR [11:8] | | | | ÿÿÿÿ 1111 | | | | | |
| 1E ADDRESS | A/D conversion result high significant bit | | | | | | xxxx xxxx | | | | | | | | |
| 1F ADCON0 | ADFM | VCFG1 | VCFG0 | CHS[2:0] | | | GO/DONE | ADON | 0000 0000 | | | | | | |
| 20-7F | SRAM BANK1 (96Bytes), physical address 0x00–0x5F | | | | | | xxxx xxxx | | | | | | | | |

Table 17-3 SFR, BANK 0

| address name | | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | reset value | | | |
|--------------|--------|---|------------|-----------------------------------|-------|---------|-------|---------|-----------|-----------------|--|--|--|
| 80 | INC | Data memory accesses (not physical registers) using the contents of the FSR | | | | | | | | xxxx xxxx | | | |
| 81 | OPTION | /PAPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | | | |
| 82 | PCL | Program counter lower 8 bits | | | | | | | | 0000 0000 | | | |
| 83 | STATUS | FSRB8 | PAGE[1:0] | | /TF | /PF | FROM | HC | C | 0001 1xxx | | | |
| 84 | FSR | Indirect addressing pointer register | | | | | | | | xxxx xxxx | | | |
| 85 | TRISA | TRISA [7:0] | | | | | | | | 1111 1111 | | | |
| 87 | TRISC | | | TRISC [5:0] | | | | | | ÿÿ11 1111 | | | |
| 88 | WPUC | | | WPUC [5:0] | | | | | | ÿÿ00 0000 | | | |
| 89 | WPD | | | WPDA4 | WPDC1 | WPDC2 | WPDC3 | | | ÿÿ00 000ÿ | | | |
| 8A | PCLATH | | | Program counter upper 5-bit latch | | | | | | ÿÿ00 0000 | | | |
| 8B | INTCON | GIE | LIKE THIS | T0IE | NOT | PAY | T0IF | INTF | PAIF | 0000 0000 | | | |
| 8C | PIE1 | THIS | CKMEAIE | | C2IE | C1IE | OSFIE | TMR2IE | TMR1IE | 0000 0000 | | | |
| 8D | PIE2 | | | | | | | CHICKEN | CCP1IE | ÿÿÿÿ ÿÿ00 | | | |
| 8E | PCON | VREF_OE | LVDL [2:0] | | LVDEN | LVDW | | /BY | /THERE IS | 0000 0xqq | | | |
| 8F | OSCCON | LFMOD | IRCF[2:0] | | OSTS | HTS | LTS | SCS | 0101 x000 | | | | |
| 90 | PWM | AUX AUX1EN | P1OS | P1FOE | P1EOE | P1DOE | P1CCE | P1BOE | | P1AOE 0000 0000 | | | |
| 91 | ANSEL | ANSEL[7:0] | | | | | | | | 1111 1111 | | | |
| 92 | PR2 | PR2[7:0], Timer2 period register | | | | | | | | 1111 1111 | | | |
| 95 | WPUA | WPUA [7:0] | | | | | | | | 1111 1111 | | | |
| 96 | JOKE | JOKE [7:0] | | | | | | | | 0000 0000 | | | |
| 99 | VRCN | VREN | | VRR | | VR[3:0] | | | | 0ÿ00 0000 | | | |
| 9A | EEDAT | EEDAT [7:0] | | | | | | | | 0000 0000 | | | |
| 9B | EEADR | EEADR [7:0] | | | | | | | | 0000 0000 | | | |
| 9C | EECON1 | | | WREN3 | WREN2 | WRERR | WREN1 | | | ÿÿ00 x0ÿ0 | | | |
| 9D | EECON2 | | | | | | | | | WR ÿÿÿÿ ÿÿ0 | | | |
| 9E | ADRESL | A/D conversion result low significant bit | | | | | | | | xxxx xxxx | | | |
| 9F | ADCN1 | TWO | ADCS[2:0] | | | | | | | 0000 ÿÿÿ | | | |
| A0-BF | | SRAM BANK1 (32Bytes), physical address 0x00–0x1F | | | | | | | | xxxx xxxx | | | |
| C0-EF | | | | | | | | | | --- | | | |
| F0-FF | | SRAM, access BANK0's 0x70–0x7F | | | | | | | | xxxx xxxx | | | |

Table 17-4 SFR, BANK 1

| address | name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | reset value | | | | | | |
|-------------------------------|---|---|-------------|--------------|---|-------|-----------|-----------|-----------|-------------|--|--|--|--|--|--|
| 100 | INC | Data memory accesses (not physical registers) using the contents of the FSR | | | | | | xxxx xxxx | | | | | | | | |
| 102 PCL | | Program counter lower 8 bits | | | | | | 0000 0000 | | | | | | | | |
| 103 STATUS | FSRB8 | PAGE[1:0] | /TF | /PF | FROM | HC | C | 0001 1xxx | | | | | | | | |
| 104 FSR | | Indirect addressing pointer register | | | | | | xxxx xxxx | | | | | | | | |
| 108 VCON1 | | VREGM[1:0] | VREGHB[4:0] | | | | | | ÿ000 0000 | | | | | | | |
| 109 VCON2 | | | VREGLB[4:0] | | | | | | ÿÿ0 0000 | | | | | | | |
| 10A PCLATH | | Program counter upper 5-bit latch | | | | | | ÿÿ0 0000 | | | | | | | | |
| 10B INTCON | GIE | LIKE THIS | T0IE | NOT | PAY | T0IF | INTF | PAIF | 0000 0000 | | | | | | | |
| 10C TMR3L | TMR3 [7:0], TMR3 lower 8 bits | | | | | | xxxx xxxx | | | | | | | | | |
| 10D TMR3H | TMR3 [11:8], TMR3 upper 4 bits | | | | PR3[11:8] High 4 bits of Timer3 period register | | | | | | | | | | | |
| 10E PR3L | PR3[7:0] Timer3 period register lower 8 bits | | | | | | 1111 1111 | | | | | | | | | |
| 10F PWM3CR0 P3INTS | P3PER[2:0] | | | P3CKSRC[2:0] | | | | P3BZR | 0000 0000 | | | | | | | |
| 110 PWM3CR1 P3EN | P3POL TMR3PS[2:0] | TMR3ON TMR3IE TMR3IF | | | | | | | | | | | | | | |
| 111 T3CKDIV | Timer3 Clock Divider Register | | | | | | 0000 0000 | | | | | | | | | |
| 112 TMR4L | TMR4 [7:0], TMR4 lower 8 bits | | | | | | xxxx xxxx | | | | | | | | | |
| 113 TMR4H | TMR4 [11:8], TMR4 upper 4 bits | | | | PR4[11:8] High 4 bits of Timer4 period register | | | | | | | | | | | |
| 114 PR4L | PR4[7:0] Timer4 period register lower 8 bits | | | | | | 1111 1111 | | | | | | | | | |
| 115 PWM4CR0 P4INTS P4PER[2:0] | P4POL TMR4PS[2:0] | | | P4CKSRC[2:0] | | | | P4BZR | 0000 0000 | | | | | | | |
| 116 PWM4CR1 P4EN | P4POL TMR4PS[2:0] | TMR4ON TMR4IE TMR4IF | | | | | | | | | | | | | | |
| 117 T4CKDIV | Timer 4 Clock Divider Register | | | | | | 0000 0000 | | | | | | | | | |
| 118 TMR5L | TMR5 [7:0], TMR5 lower 8 bits | | | | | | xxxx xxxx | | | | | | | | | |
| 119 TMR5H | TMR5 [11:8], TMR5 upper 4 bits | | | | PR5[11:8] High 4 bits of Timer5 period register | | | | | | | | | | | |
| 11A PR5L | PR5[7:0] Lower 8 bits of Timer5 period register | | | | | | 1111 1111 | | | | | | | | | |
| 11B PWM5CR0 P5INTS P5PER[2:0] | P5POL TMR5PS[2:0] | | | P5CKSRC[2:0] | | | | P5BZR | 0000 0000 | | | | | | | |
| 11C PWM5CR1 P5EN | P5POL TMR5PS[2:0] | TMR5ON TMR5IE TMR5IF | | | | | | | | | | | | | | |
| 11D T5CKDIV | Timer 5 Clock Divider Register | | | | | | 0000 0000 | | | | | | | | | |
| 120 - 16F | | | | | | | — | | | | | | | | | |
| 170 - 17F | SRAM, access BANK0's 0x70-0x7F | | | | | | xxxx xxxx | | | | | | | | | |

Table 17-5 SFR, BANK 2

Note:

1. INDF is not a physical register;
2. The gray part indicates that it is not implemented;
3. Do not write to unimplemented register bits;
4. The reset value of ANSEL is 0xFF. After reset, PORTA[3:0] and PORTC[2:0] are analog pins. At this time, the read operation of these IOs returns The value is 0, regardless of its data register contents

17.3 STATUS register

| name | state | Register address | reset value | |
|-------|--|------------------|-----------------------|--------------------|
| FSRB8 | The 8th bit of the FSR register, which forms a 9-bit register with FSR, is used in indirect addressing, see chapter 17.4 for details | STATUS[7] | | RW-0 |
| PAGE | <u>Register Bank Select Bits</u> 00 = Bank 0 (0x00h – 0x7Fh) 01 = Bank 1 (0x80h – 0xFFh) 1x = Bank 2 (0x100 – 0x17F) | STATUS[6:5] | | RW _y 00 |
| /TF | <u>Timeout Flag 1</u> = After power-up, a CLRWDT or SLEEP instruction was executed 0 = A WDT time-out occurred | STATUS[4] | | RO _y 1 |
| /PF | <u>Power-down flag</u> bit 1 = After a power-on reset or a CLRWDT instruction was executed 0 = A SLEEP instruction was executed | STATUS[3] | 0x03 0x83 0x103 | RO _y 1 |
| FROM | <u>0 flag bit: the result of an arithmetic or logical operation is zero?</u> 1 = Yes 0 = No | STATUS[2] | | RW _y x |
| HC | <u>Digit Carry/ Digit Borrow (ADDWR, ADDWI, SUBWI, SUBWR):</u> <u>Does the 4th low-order bit of the result carry or borrow from the high-order bit?</u> 1 = Carry, or not borrowed 0 = Not carry, or borrow | STATUS[1] | | RW _y x |
| C | <u>Carry/Borrow (ADDWR, ADDWI, SUBWI, SUBWR): Carry or borrow from the MSB of the result?</u> 1 = Carry, or not borrowed 0 = Not carry, or borrow | STATUS[0] | | RW _y x |

Table 17-6 Status Register

Note:

1. Like other registers, the STATUS status register can also be used as the destination register for any instruction. However, if an instruction affecting the Z, HC or C bits has STATUS as the destination register, then writes to these three bits will be disabled, and the Z, HC and C bits will only be set or cleared by the result of the operation. At this time, after executing an instruction with STATUS as the target register, the content of STATUS may not be as expected.
2. It is recommended to use only BCR, BSR, SWAPR and STR instructions to manipulate the STATUS register.

17.4 PCL and PCLATH

The program area has only 1 Page (2k Words), at the end of the Page (0x7FF) it will roll back to the beginning of the Page (0x000). place of command

The address width is 11 bits and can address 2kW. LJUMP and LCALL are equal length jump instructions without setting PCLATH.

The Program Counter (PC) is 11 bits wide. Its lower 8 bits come from the readable and writable PCL register, and its upper 3 bits (PC[10:8]) come from PCLATH, not

Can read and write directly. When a reset occurs, the PC will be cleared to 0. Figure 17-3 shows two scenarios for loading the PC value.

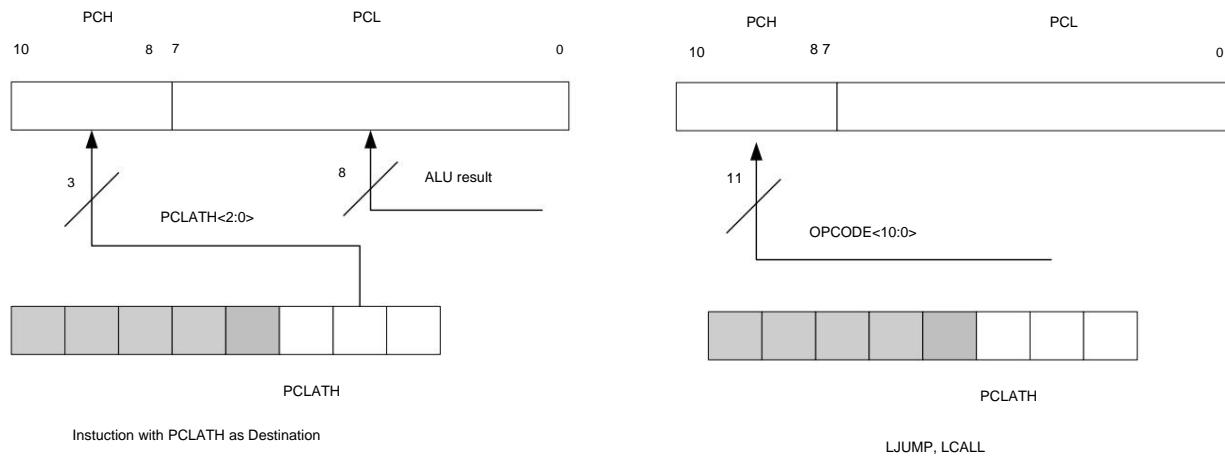


Figure 17-3 Different cases of loading PC values

Executing any instruction targeting the PCL register will also cause the PC[10:8] bits of the Program Counter to be replaced with the contents of PCLATH.

Therefore, the entire contents of the program counter PC can be changed by writing the desired upper 3 bits to the PCLATH register first.

Computing the LJUMP instruction is accomplished by adding an offset (ADDWR PCL) to the program counter PC. Therefore, by modifying the PCL Special care should be taken when jumping to a look-up table or program branch table (computing LJUMP) using a register. Assuming PCLATH is set to the start address of the table, If the length of the table is greater than 255 instructions, or the lower 8 bits of the address are in the middle of the table, it will return to 0x00 when it rolls over to 0xFF, then every table PCLATH must be incremented when a rollover occurs at the start address of the table or the destination address in the table.

INDF is not a physically present register, addressing INDF will result in indirect addressing.

Any instruction that uses the INDF register actually refers to the file select register (File Select Register, [FSRB8, FSR]) unit to access. An indirect read of INDF will return 0, and an indirect write of INDF will result in a no-op (may affect the sound status flag).



18. Electrical Characteristics

18.1 Limit parameters

| | | |
|--|---------------------|--------|
| Ambient temperature class 3..... | -40 - | + 85°C |
| Ambient operating temperature class 2..... | -40 - +105°C | |
| Ambient operating temperature class 1..... | -40 - +125°C | |
| Storage temperature..... | -40 - +125°C | |
| Supply Voltage..... | VSS-0.3V – VSS+6.0V | |
| Port Input Voltage..... | VSS-0.3V – VDD+0.3V | |

Note:

1. Exceeding the range specified in the above "limit parameters" may cause permanent damage to the chip.
 2. Unless otherwise noted, all characteristics are tested at 25°C, VDD = 2.0 – 5.5V.
 3. The values and ranges shown in this section are based on characteristic values and are not standard values for final shipment.
 4. Production tested at 25°C unless otherwise noted. Since high temperature screening is not a routine test process, the above working environment temperature is exceeded.
- Some performance parameters of the chip cannot be guaranteed when the
5. Typical data retention times greater than 10 years without stress testing at 150°C.

18.2 Operating Characteristics

| parameter | | Min | Typ | Max | Units | | | condition |
|-------------------------------------|--------------|-----------------------------|-------|-----|-------|--------------|----------------------------------|------------------------|
| Fsys (SysClk) | 2T/4T | | | 8 | | MHz | -40 – | 85°C, VDD = 2.0 – 5.5V |
| | | | | 16 | | MHz | -40 – | 85°C, VDD = 2.7 – 5.5V |
| Instruction cycle (TINSTRCLK) | 2T | | | 125 | | ns | SysClk = HIRC | |
| | 4T | | | 250 | | ns | | |
| | 2T | | | 61 | | ÿs | SysClk = LIRC | |
| | 4T | | | 122 | | ÿs | | |
| T0CKI high or low pulse width | | 0.5 | TT0CK | | | | ns no prescaler | |
| | | + 20 | | | | | | |
| | | 10 | | | | | | ns with prescaler |
| T0CKI input period | | Max. 20 and (TT0CK+40)/N | | | | ns | N = 1, 2, 4, ..., (no prescaler) | 256 (with prescaler) |
| | | | | | | | N = 1 prescaler) | |
| T1CKI high or low pulse width | Synchronize | (Tsysclk + 20) / N 10 | | | | ns | N = 1, 2, 4, 8 (with prescaler) | |
| | asynchronous | or 30 / N the greater of | | | | ns | | |
| T1CKI input period | Synchronize | 2 * (Tsysclk + 20) / N 20 | | | | ns | | |
| | asynchronous | or 60 / N the greater of | | | | ns | | |
| Power-on Reset Hold Time (TDRH) | | | 4.2 | | | ms | 25°C, PWRT disable | |
| External Reset Pulse Width (TMCLRB) | | 2000 | | | | ns | 25°C | |
| WDT period (TWDT) | | | 1 | | | ms prescaler | = 1:1 | |

Note: TT0CK refers to the clock period selected by T0CS.

18.3 POR, LVR, LVD**Power-On Reset (POR)**

| characteristic | Min | Typ | Max | Units | | | condition |
|------------------------|-----|-----|-----|-------|--|----|-----------------|
| IPOR operating current | | | | 0.14 | | ÿA | 25°C VDD = 3.3V |
| VPOR | | | | 1.65 | | IN | 25°C |

Low Voltage Reset (LVR)

| parameter | Min | Typ | Max | Units | | | condition |
|----------------------|------|-----|-----|-------|--------|----|------------------------|
| ILVR working current | | | | 18.7 | | ÿA | 25°C, VDD = 3.3V |
| VLVR, LVR threshold | 1.90 | | 2.0 | 2.10 | V 25°C | | |
| | 2.09 | | 2.2 | 2.31 | | | |
| | 2.38 | | 2.5 | 2.63 | | | |
| | 2.66 | | 2.8 | 2.94 | | | |
| | 2.95 | | 3.1 | 3.26 | | | |
| | 3.42 | | 3.6 | 3.78 | | | |
| | 3.90 | | 4.1 | 4.31 | | | |
| LVR delay | | | | 125 | 157 | ÿs | 25°C, VDD = 2.0 – 5.5V |

Low Voltage Detection (LVD)

| characteristic | Min | Typ | Max | Units | | | condition |
|------------------------|------|-----|-----|-------|-----|----|------------------------|
| ILVD operating current | | | | 24.5 | | ÿA | 25°C, VDD = 3.3V |
| VLVD, LVD threshold | 1.90 | | 2.0 | 2.10 | IN | | |
| | 2.28 | | 2.4 | 2.52 | | | |
| | 2.66 | | 2.8 | 2.94 | | | |
| | 2.85 | | 3.0 | 3.15 | | | |
| | 3.42 | | 3.6 | 3.78 | | | |
| | 3.80 | | 4.0 | 4.20 | | | |
| | | | | 125 | 157 | ÿs | 25°C, VDD = 2.0 – 5.5V |

18.4 I/O port circuit

| parameter | Min | Typ | Max | Units | | | condition |
|-------------------------|----------|-----|-----|----------|----|------------------------------|-----------|
| WILL | 0 | | | 0.3* VDD | IN | | |
| HIV | 0.7* VDD | | | VDD | IN | | |
| leakage current | -1 | | | 1 | ȳA | VDD = 5V | |
| Source current (Source) | | | -30 | | mA | 25°C, VDD = 5.0V, VOH = 4.5V | |
| Sink current (Sink) | | | 23 | | mA | 25°C, VDD = 5.0V, VOL= 0.5V | |
| Pull-up resistor | | | 28 | | kȳ | 25°C, VDD = 5.0V | |
| | | | 63 | | | 25°C, VDD = 3.3V | |
| pull-down resistor | | | 93 | | kȳ | 25°C, VDD = 5.0V | |
| | | | 229 | | | 25°C, VDD = 3.3V | |

18.5 Working current (IDD)

| parameter | SysClk | Typical @VDD | | | unit |
|---------------------------------------|-----------------------------|----------------------|---------------|-------|------|
| | | 2.0V | 3.3V | 5.5V | |
| Normal Mode (2T) - IDD | 16MHz | | 1.519 | 1.654 | mA |
| | 8 MHz 0.672 | | 1.103 | 1.177 | |
| | 4 MHz 0.469 | | 0.643 | 0.680 | |
| | 2 MHz 0.289 | | 0.397 | 0.418 | |
| | 1 MHz 0.199 | | 0.274 | 0.288 | |
| | 32 kHz 0.032 | | 0.048 | 0.050 | |
| Sleep mode (WDT OFF, LVR OFF), ISB | | 0.166 | 0.386 | 0.697 | ȳA |
| Sleep mode (WDT ON, LVR OFF) | 32 kHz 2.960 | | 3.240 | 3.200 | |
| Sleep mode (WDT OFF, LVR ON) | | 17.910 | 18.730 22.150 | | |
| Sleep mode (WDT ON, LVR ON) | 32 kHz 18.940 20.450 24.730 | | | | |
| Sleep mode (WDT OFF, LVR OFF, LVD ON) | | 22.990 24.500 28.860 | | | |

Note: The test condition for sleep mode ISB is that all I/Os are set to input mode and pulled down to GND externally.



18.6 Internal Oscillator

Internal Low Frequency Oscillator (LIRC)

The test condition is 32 kHz selected for LIRC (LFMOD=0).

| characteristic | Min | Typ | Max | Units | | | condition |
|-------------------------------------|-------|-----|-----|-------|------|--|------------------------|
| Frequency Range | 29.4 | | 32 | | 33.6 | | kHz 25°C, VDD = 2.5V |
| Range with temperature | -2.0% | | | | 2.0% | | -40 – 85°C, VDD = 2.5V |
| Variation range with supply voltage | -2.5% | | | | 1.0% | | 25°C, VDD = 2.0 – 5.5V |
| ILIRC operating current | | | | 1.1 | | | mA 25°C, VDD = 3.0V |
| Start Time | | | | 4.6 | | | µs 25°C, VDD = 3.0V |

Internal High Frequency Oscillator (HIRC)

| parameter | Min | Typ | Max | Units | | | condition |
|-------------------------------------|-------|-----|-------|-------|-------|--|------------------------|
| Frequency Range | 15.84 | | 16 | | 16.16 | | MHz 25°C, VDD = 2.5V |
| Range with temperature | -6.0% | | ±4.0% | | 4.0% | | -40 – 85°C, VDD = 2.5V |
| Variation range with supply voltage | -1.0% | | | | 1.0% | | 25°C, VDD = 2.0 – 5.5V |
| IHIRC working current | | | | 30 | | | mA 25°C, VDD = 3.0V |
| Start Time | | | | 2.5 | | | µs 25°C, VDD = 3.0V |

18.7 ADC (10 bit) and ADC VREF

ADC (10 bit)

| parameter | Min | Typ | Max | Units | | | condition |
|---------------------------------------|-----|-----|-------|-------|--|----------------------------|-----------|
| ADC working voltage VDD | 2.7 | | | 5.5 | | IN | |
| ADC operating current IVDD | | | 90 | | | mA VREF = VDD = 5.5V | |
| Analog input voltage VAIN | VSS | | | VREF | | IN | |
| External reference voltage VREF | 2.0 | | | VDD | | IN | |
| Resolution | | | | 10 | | bit | |
| Integration error EIL | | | ± 1.0 | | | LSB VREF = VDD = 5.0V | |
| Differential error EDL | | | ± 0.5 | | | LSB FADC CLK = 250KHZ | |
| Offset error EOFF | | | ± 5.0 | | | LSB VREF = VDD = 5.0V | |
| Gain Error EGN | | | ± 2.0 | | | LSB FADC CLK = 250KHZ | |
| Conversion clock period TAD | | | 2 | | | µs VREF > 3.0V, VDD > 3.0V | |
| Number of conversion clocks | | | 14.5 | | | THEN | |
| Settling Time (TST) | | | 15 | | | µs | |
| Sampling Time (TACQ) | | | 2 | | | µs | |
| Analog Voltage Source Impedance (ZAI) | | | | 10 | | kΩ (recommended) | |

Differential error **DNL**

| typical DNL Error (LSB) @ VDD = 5 V | | | |
|-------------------------------------|------|------|------|
| VREF+ FADCLK | 2 | 3 | VDD |
| ÿ 1 MHz | ±0.5 | ±0.5 | ±0.5 |
| 2 MHz | ±2.0 | ±1.0 | ±1.0 |
| 4 MHz | | | ±3.5 |

Integral error **INL**

| typical INL Error (LSB) @ VDD = 5 V | | | |
|-------------------------------------|------|------|------|
| VREF+ FADCLK | 2 | 3 | VDD |
| ÿ 1 MHz | ±0.5 | ±0.5 | ±0.5 |
| 2 MHz | ±2.0 | ±1.5 | ±1.0 |
| 4 MHz | | | ±3.5 |

ADC VREF (internal voltage reference)

| parameter | Min | Typ | Max | Units | | | condition |
|--|-----------------------|-------|-----|-------|-------|----|------------------------|
| Internal reference voltage VADC-REF | VADC-REF = 2.0V | 1.990 | | 2 | 2.010 | IN | 25°C, VDD = 5.0V |
| | VADC-REF = 3.0V | 2.985 | | 3 | 3.015 | IN | 25°C, VDD = 5.0V |
| Variation range with voltage | VADC-REF = 2.0V -1.0% | | | | 1.0% | IN | 25°C, VDD = 2.7~5.5V |
| | VADC-REF = 3.0V | -0.5% | | | 0.5% | IN | 25°C, VDD = 3.5~5.5V |
| Range with temperature | VADC-REF = 2.0V -2.0% | | | | 2.0% | | -40 ~ 85°C, VDD = 5.0V |
| | VADC-REF = 3.0V | -2.0% | | | 2.0% | | -40 ~ 85°C, VDD = 5.0V |
| Settling time TVRINT | VADC-REF = 2.0V | | 450 | | | ÿs | |
| | VADC-REF = 3.0V | | 450 | | | ÿs | |

18.8 Comparator Comparator Circuit

| parameter | Min | Typ | Max | Units | | | condition |
|---------------------------------------|-----|-----|-----|--------|--------------------------|----------|------------|
| Ivdd working current | — | 70 | — | uA | 3V,25V | | |
| Operating Voltage | 2.0 | — | 5.5 | | | IN | |
| Input Common Mode | 0 | — | VDD | -1.5 V | 2.0V | ~5.5V | -40°C~85°C |
| Voltage Input Offset Voltage (Offset) | — | ±5 | | ±10 | mV | as above | |
| Common Mode Rejection Ratio | 55 | — | — | dB | as above | | |
| (CMRR) Hysteresis (Hysteresis) | — | — | 0 | — | mV | Same as | above |
| Response Time | — | 200 | — | ns | normal mode: output low | → high | |
| | — | 150 | — | ns | normal mode: output high | → low | |
| Reference voltage stabilization time | | | 10 | | us | | |

18.9 4bit DAC circuit (comparator reference voltage setting)

| parameter | Min | Typ | Max | Units | | | condition |
|-------------------|-----|------|-----|-------|-----------------------|-------------------|-------------------|
| Relative accuracy | — | VDD | /16 | — | V 2.0V | ~5.5V, -40°C~85°C | |
| absolute accuracy | — | — | — | ±1/2 | | LSB 2.0V | ~5.5V, -40°C~85°C |
| unit resistor | — | 5000 | — | — | 2.0V~5.5V, -40°C~85°C | | |
| Settle Time | — | — | — | 10 | us | 0000 → 1111 | |

18.10 Voltage Regulator Output Circuit

| parameter | Min | Typ | Max | Units | | Conditions/Remarks |
|----------------------|-----|-------|-----|-------|-----|----------------------------|
| Ivdd working current | — | 70.68 | — | uA | 25V | VDD =3.3V |
| The output voltage | — | — | 2.4 | — | IN | VREGM=00, VDD =3.3~5.5V |
| | — | — | 3.6 | — | IN | VREGM=01, VDD=3.8~5.5V |
| | — | — | 4.8 | — | IN | VREGM=10, VDD =5~5.5V |
| | — | 5.24 | — | V | | VREGM=11, VDD =5.5V |
| Output current | — | — | 200 | — | uA | VDD = 3.3~5.5V |

18.11 Program and Data EEPROM

| parameter | | Min | Typ | Max | Units | | | condition | | |
|---------------------------------------|------------------------------|------|---------|-----|-------|----|-------------------|-------------------------------|--|--|
| VDD-READ Program/Data EE read voltage | | VPOR | | 5.5 | | IN | -40 – 85°C | | | |
| VDD-WRITE | Program EE write voltage | 2.7 | | 5.5 | | IN | -40 – 85°C | | | |
| | Data EE write voltage | 1.9 | | 5.5 | | | | | | |
| NEND | Program EE Erase/Write Times | | 100 k | | | | cycle | 25 °C | | |
| | 40 k | | | | | | | 85 °C | | |
| | Data EE Erase/Write Times | | 1,000 k | | | | | 25 °C | | |
| | 400 k | | | | | | | 85 °C | | |
| TRET | Program EE data retention | | 20 | | | | year | After 1k erasures @ 85 °C | | |
| | Data EE data retention | | 20 | | | | | After 10k erasures @ 85 °C | | |
| TWITTER | Data EE write time | . | | 2.0 | | ms | Enable Auto Erase | | | |
| PROG | Data EE programming current | . | | 300 | | µA | 25 °C | VDD = 3 V | | |

18.12 EMC Characteristics**ESD**

| parameter | | Min | Typ | Max | Units | | | condition |
|-----------|--|-----|-----|------|-------|----|--|----------------------------|
| THROW IT | | HBM | | 4000 | | IN | | MIL-STD-883H Method 3015.8 |
| THROW IT | | MM | | 200 | | IN | | JESD22-A115 |

Latch-up

| parameter | | Min | Typ | Max | Units | | | condition |
|---------------------|--|-----|-----|-----|-------|----------------|--|-----------|
| LU, static latch-up | | 200 | | | | mA EIA/JESD 78 | | |

EFT

| parameter | | Min | Typ | Max | Units | | | condition |
|-----------|--|-----|-----|-----|-------|----|--|---|
| VEFT | | 5.5 | | | | kV | | Capacitance between VDD (5V) and GND: 1µF |

19. Feature map

Note: Characteristic graphs are based on characteristic values and are for informational purposes only, not production tested.

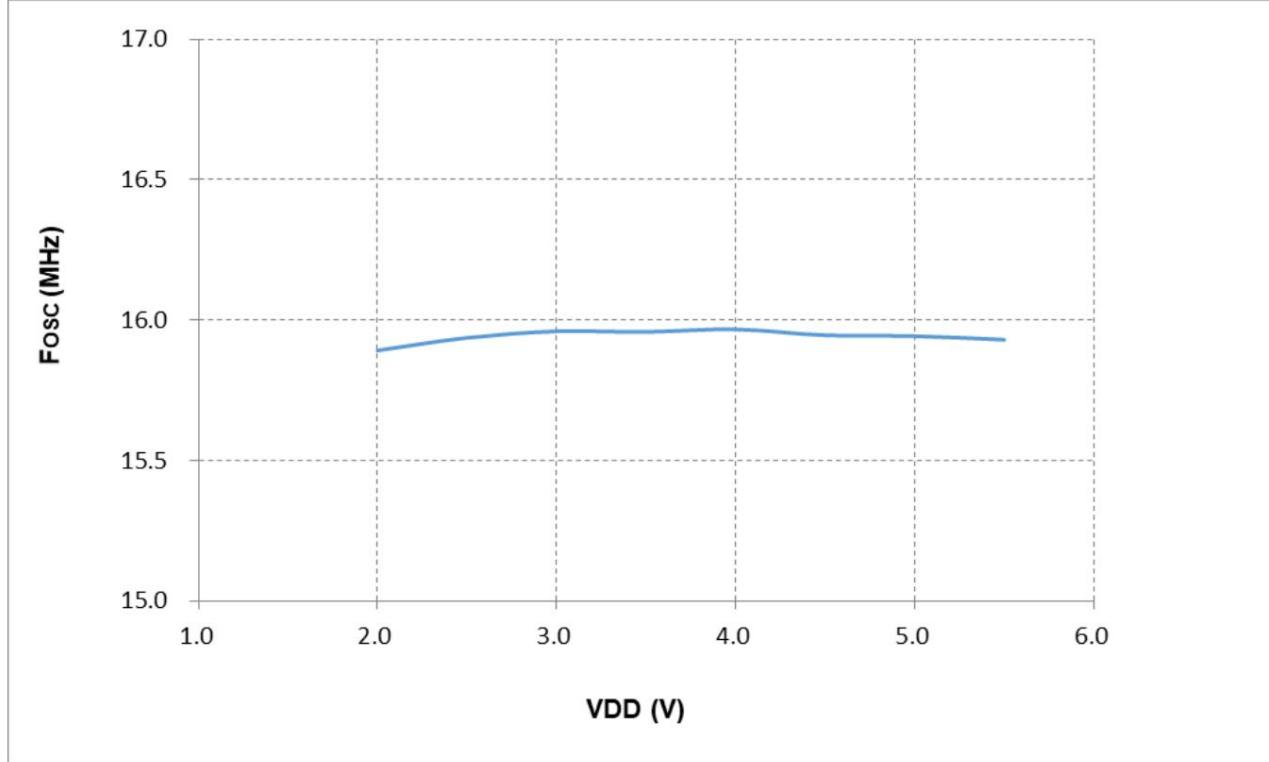


Figure 19-1 HIRC vs. VDD (TA = 25°C)

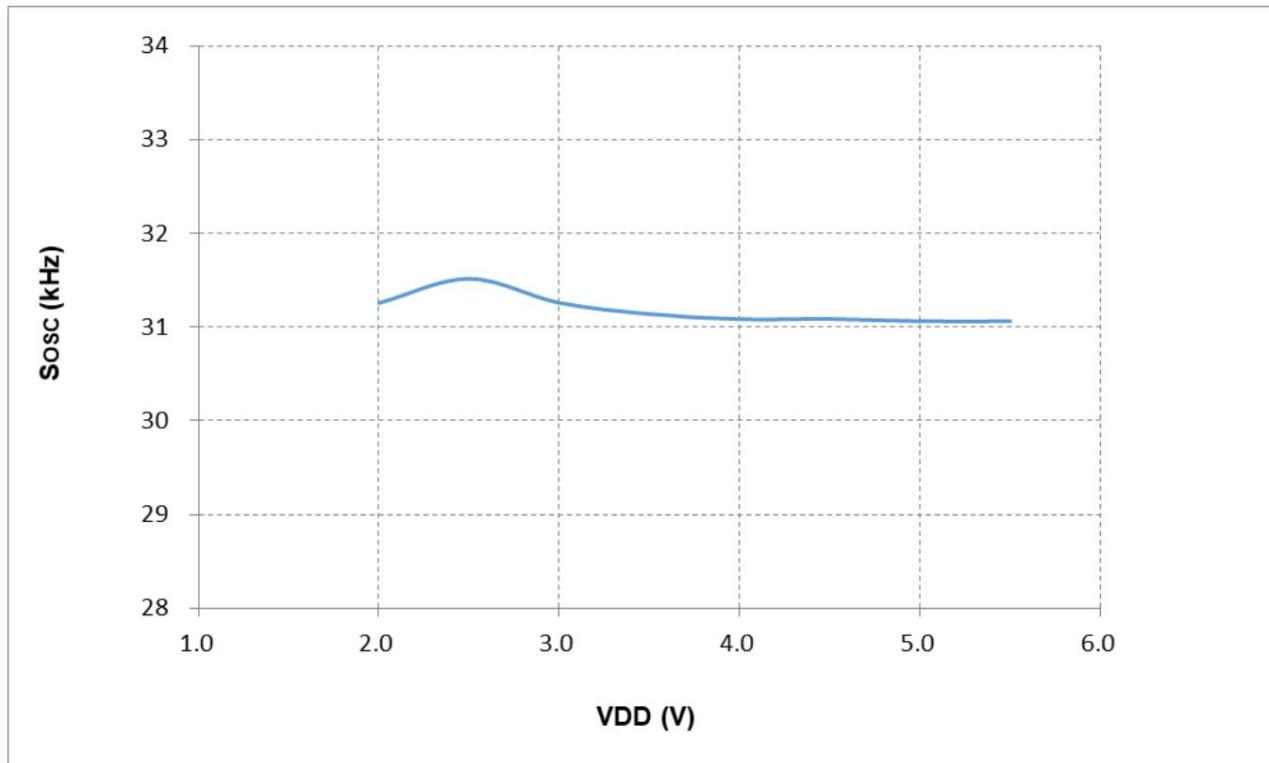
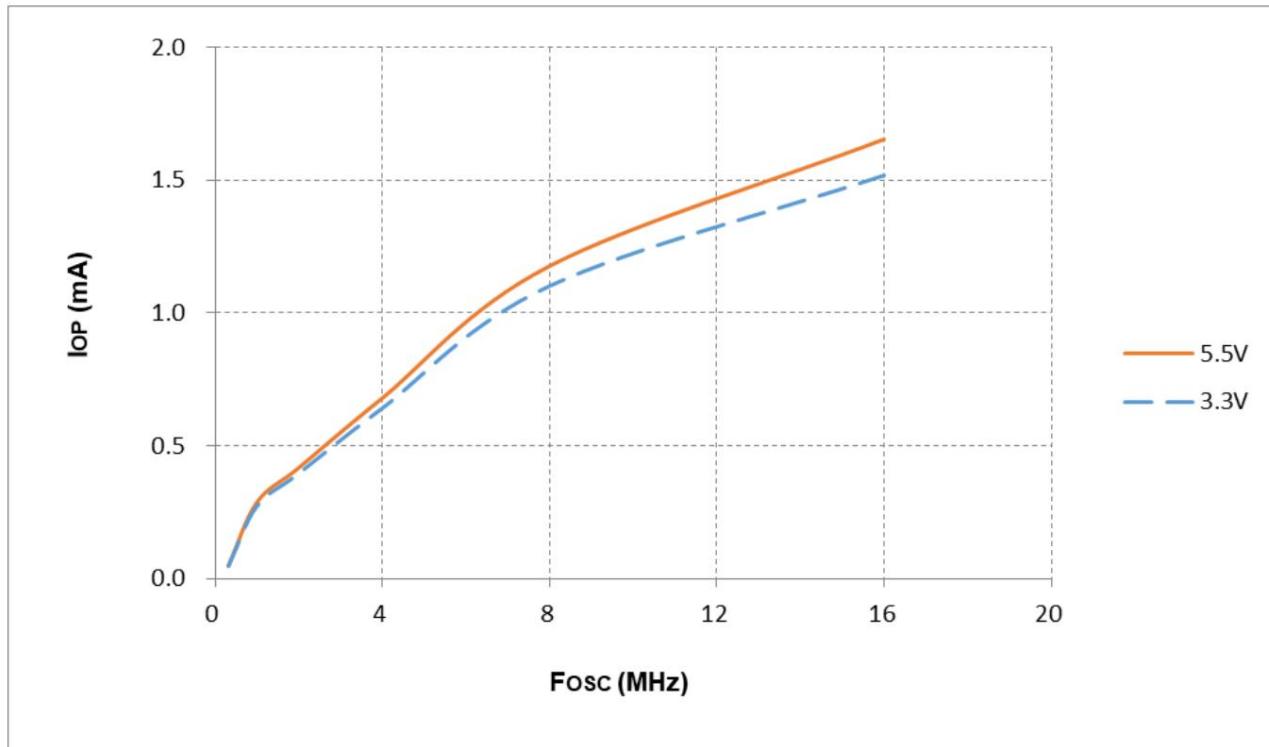
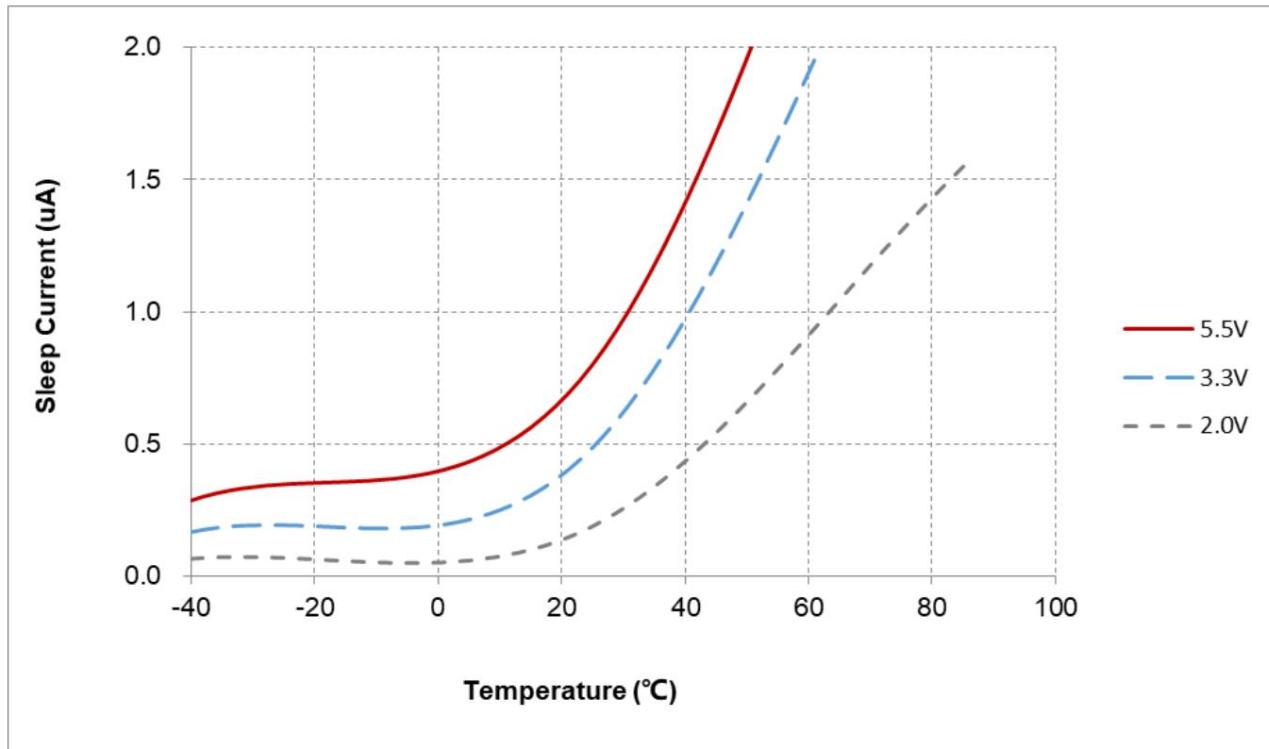


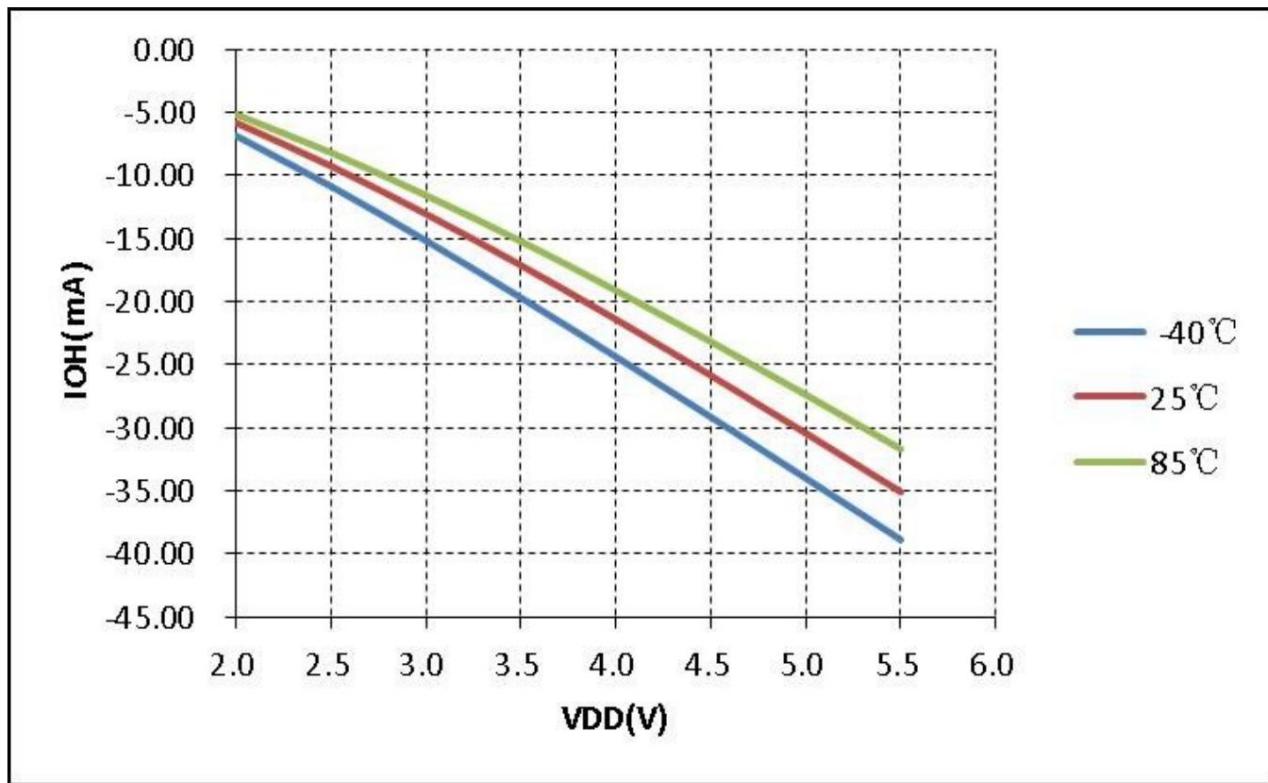
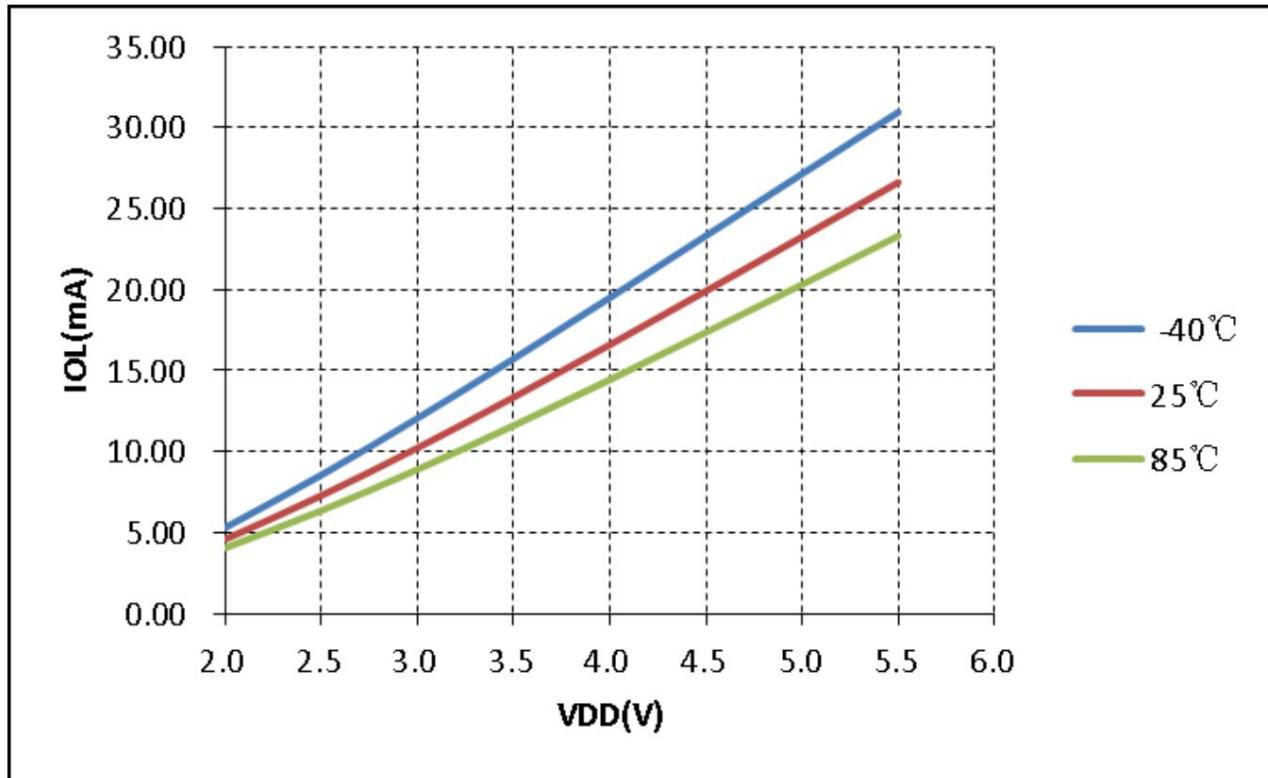
Figure 19-2 LIRC vs. VDD (TA = 25°C)



19-3 IDD vs. Frequency (2T, TA = 25°C)

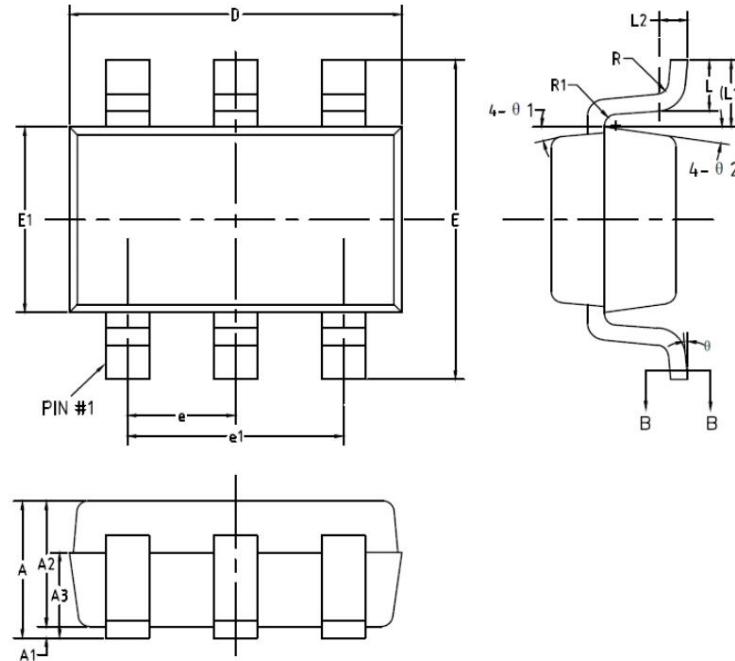


19-4 Sleep Current (ISB) vs. Temperature

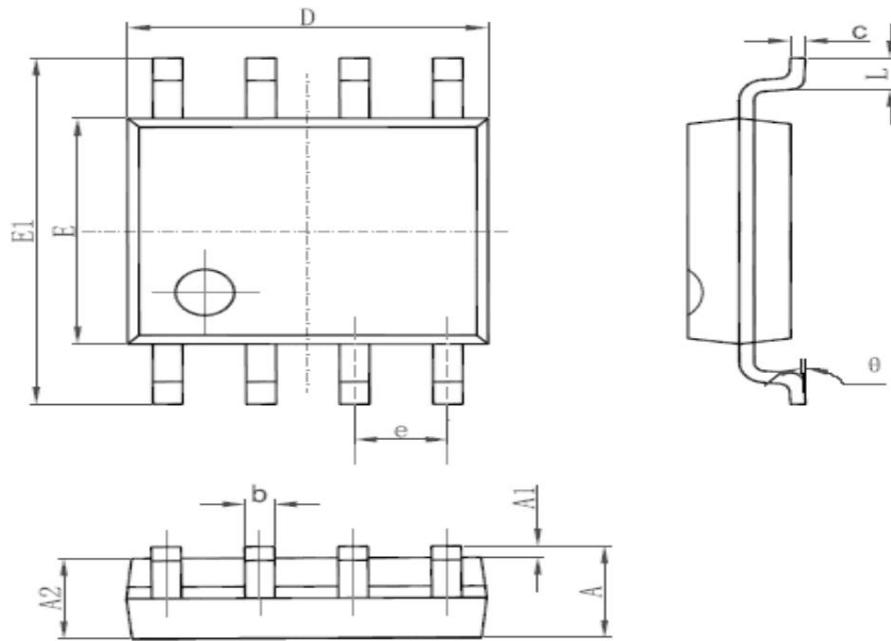
Figure 19-5 I_{OH} vs. V_{DD} , VOH @ $L = \underline{-32\text{mA}}$ Figure 19-6 I_{OL} vs. V_{DD} , V_{OL} @ $L = \underline{25\text{mA}}$

20. Package Information

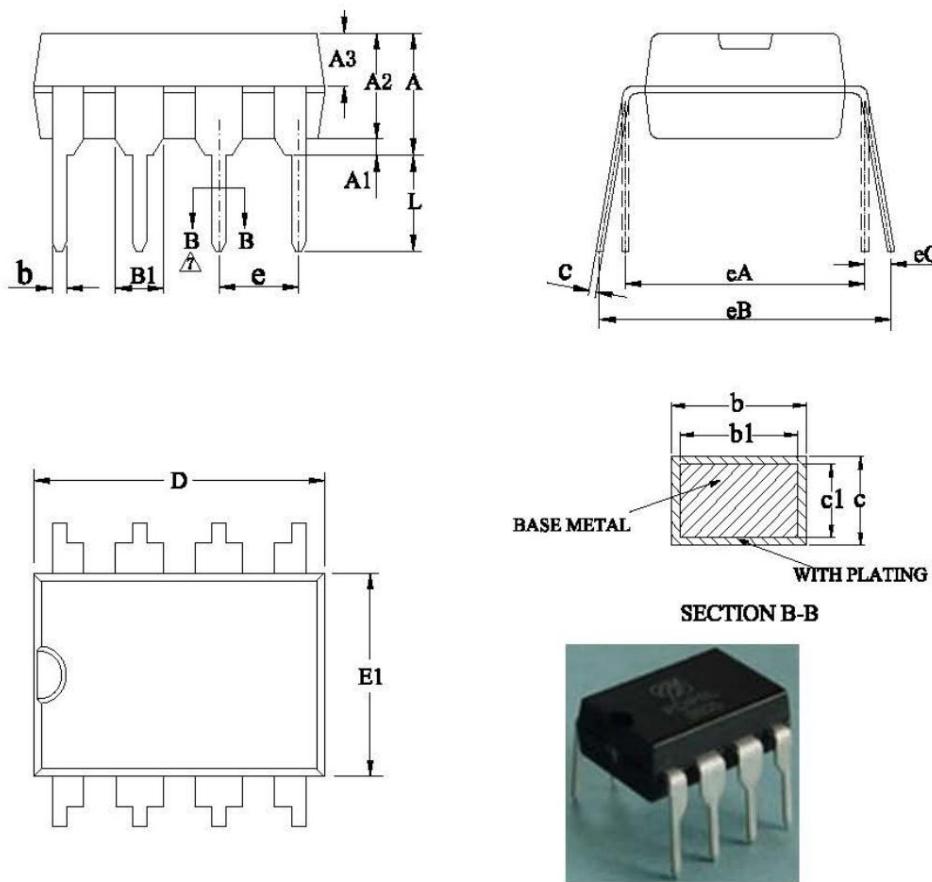
The package of this chip includes SOT23-6, SOP8, MSOP10, SOP14 and SOP16 packages. The specific package size information is as follows:

SOT23-6

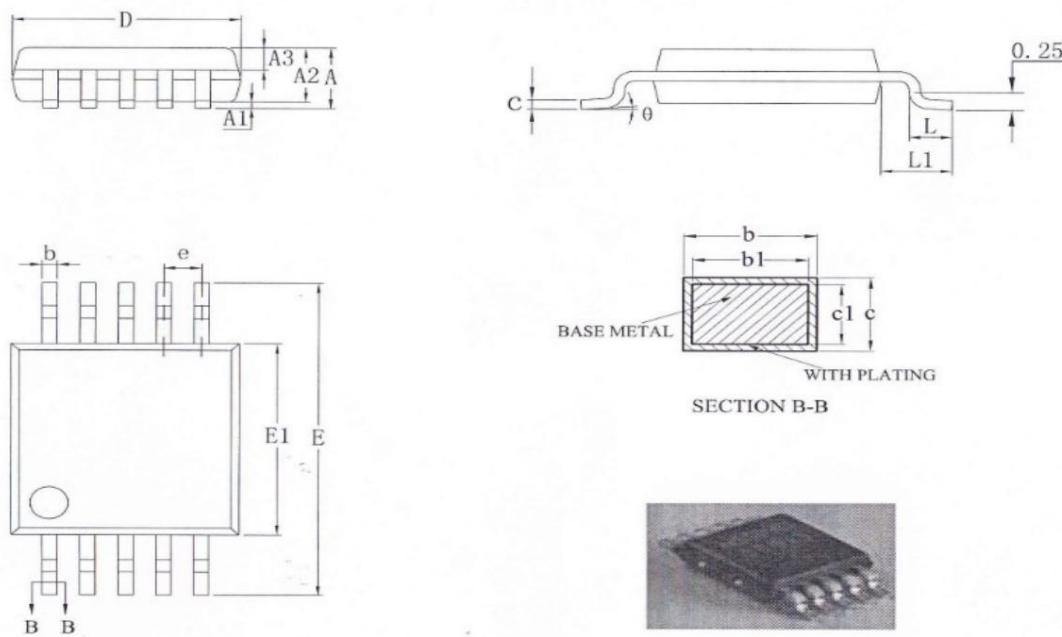
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|------|----------------------|-------|
| | Min | Max | Min | Max |
| A | | 1.45 | | 0.057 |
| A1 | 0 | 0.15 | 0 | 0.006 |
| A2 | 0.90 | 1.30 | 0.035 | 0.051 |
| A3 | 0.60 | 0.70 | 0.024 | 0.028 |
| b | 0.39 | 0.49 | 0.015 | 0.019 |
| b1 | 0.35 | 0.45 | 0.014 | 0.018 |
| c | 0.08 | 0.22 | 0.003 | 0.009 |
| c1 | 0.08 | 0.20 | 0.003 | 0.008 |
| D | 2.80 | 3.00 | 0.110 | 0.118 |
| and | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.50 | 1.70 | 0.059 | 0.067 |
| and | 0.85 | 1.05 | 0.033 | 0.041 |
| e1 | 1.80 | 2.00 | 0.071 | 0.079 |
| L | 0.35 | 0.60 | 0.014 | 0.024 |
| L1 | 0.60 REF | | 0.024 REF | |
| L2 | 0.25BSC | | 0.010BSC | |
| R | 0.10 | | 0.004 | |
| R1 | 0.10 | 0.25 | 0.004 | 0.010 |
| i | 0° | 8° | 0° | 8° |
| i1 | 7° | 11° | 7° | 11° |
| i2 | 8° | 12° | 8° | 12° |

SOP8

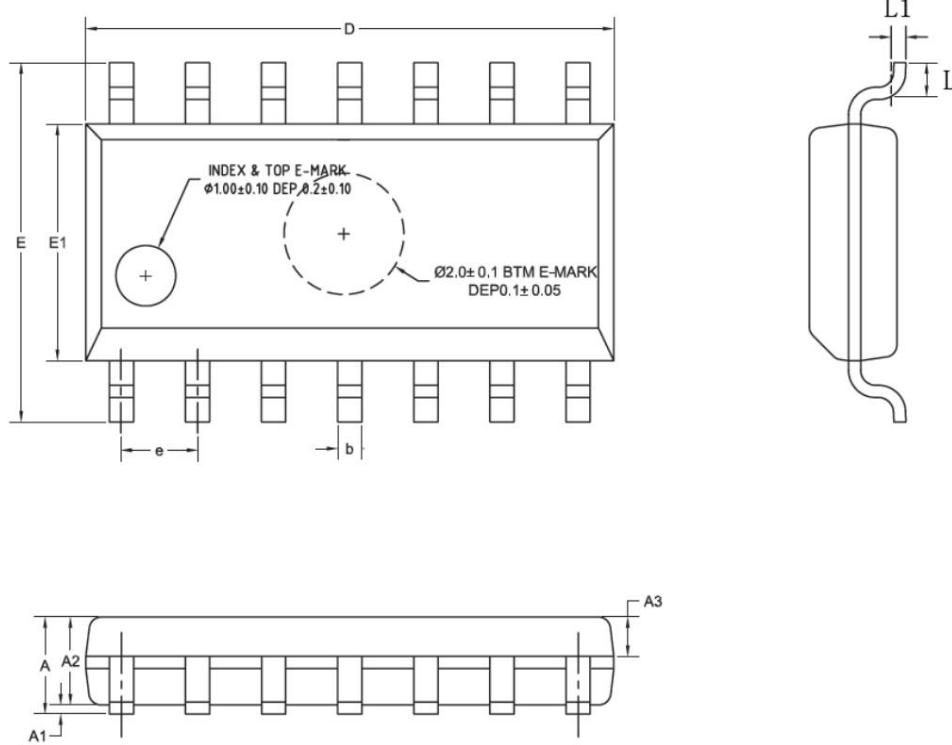
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| and | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| and | | 1.270 (BSC) | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| i | 0° | 8° | 0° | 8° |

DIP8

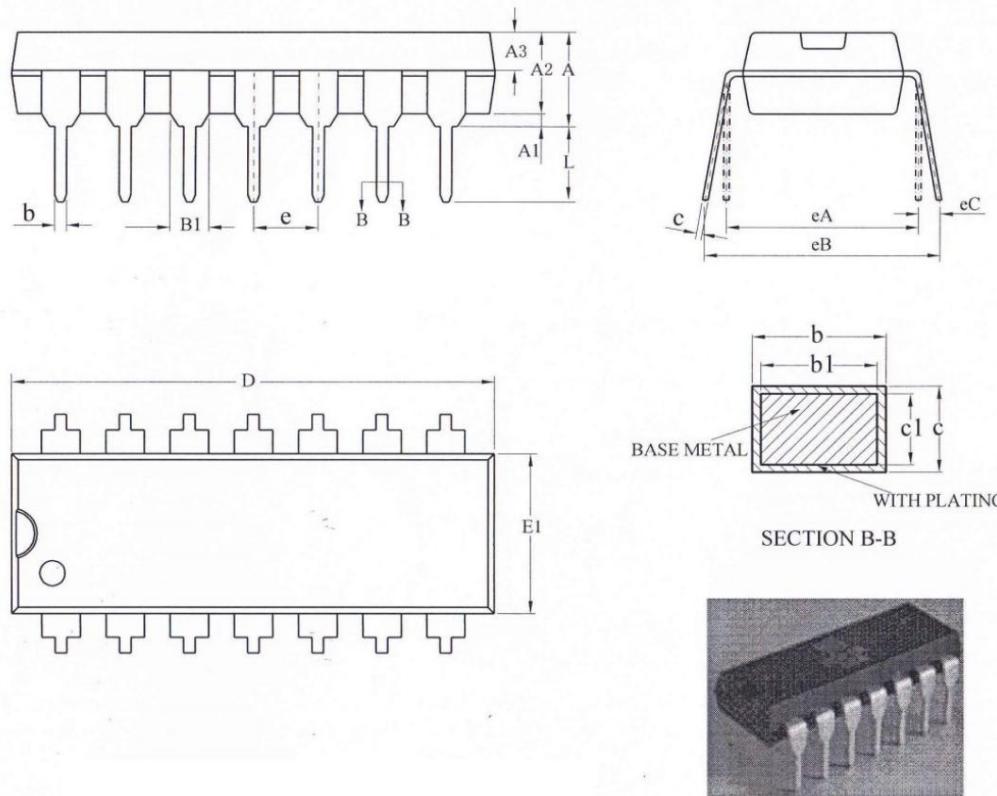
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|----------------------|----------------------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.550 | 1.650 | 0.061 | 0.065 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 9.150 | 9.350 | 0.360 | 0.368 |
| E1 | 6.250 and of A | 6.450 2.540 (BSC) | 0.246 | 0.254 |
| eB | 7.620 | 9.300 | 0.300 | 0.366 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | | 0.118 | |

MSOP10

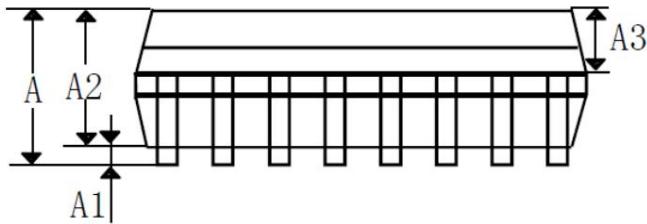
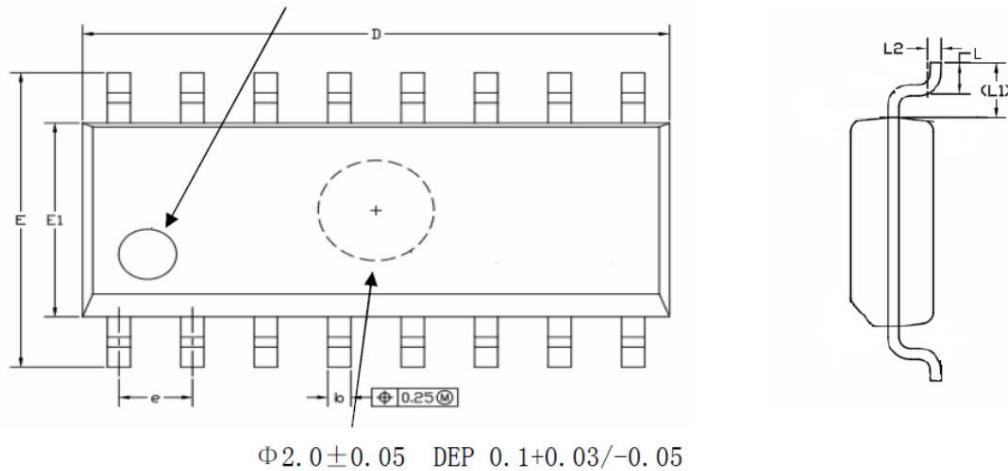
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | | 1.100 | | 0.043 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| A3 | 0.300 | 0.400 | 0.012 | 0.016 |
| b | 0.180 | 0.260 | 0.007 | 0.010 |
| b1 | 0.170 | 0.230 | 0.007 | 0.009 |
| c | 0.150 | 0.190 | 0.006 | 0.007 |
| c1 | 0.140 | 0.160 | 0.006 | 0.006 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| and | 4.700 | 5.100 | 0.185 | 0.201 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| and | 0.500 (BSC) | | 0.020 (BSC) | |
| L | 0.400 | 0.700 | 0.016 | 0.028 |
| L1 | 0.950 (REF) 0 | | 0.037 (REF) | |
| i | 8° | | 0 8° | |

SOP14

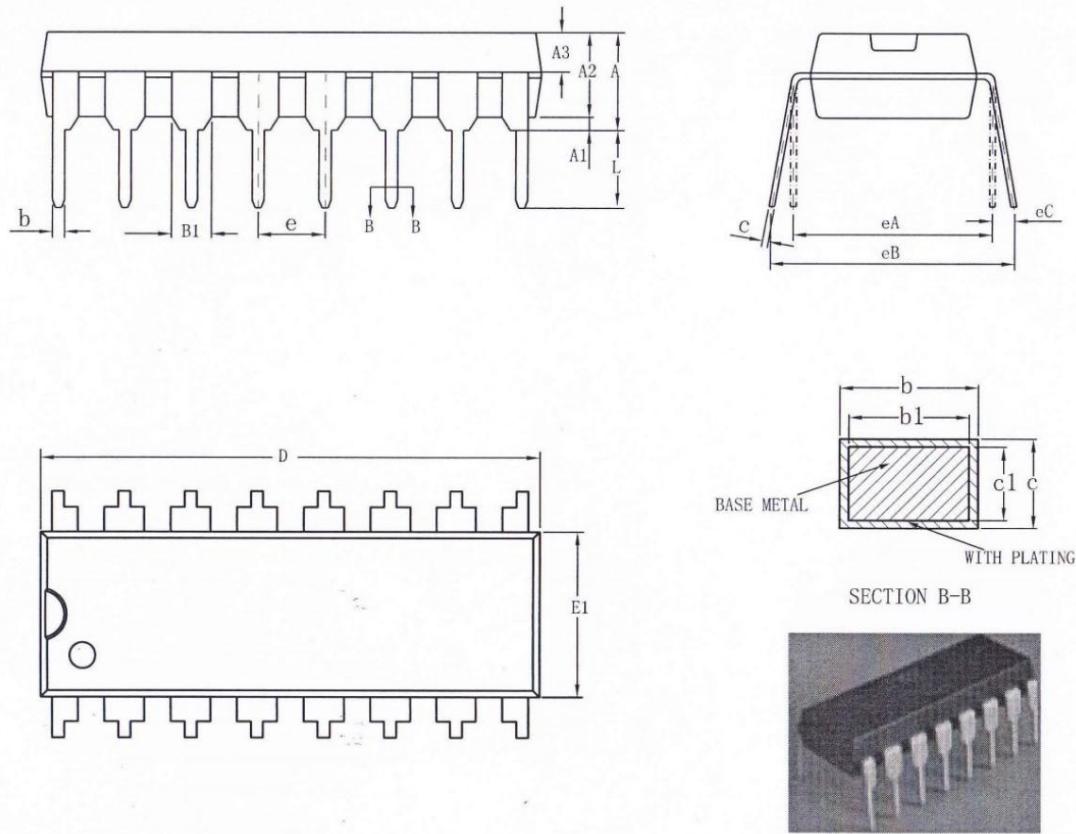
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | | 1.700 | | 0.066 |
| A1 | 0.100 | 0.200 | 0.004 | 0.008 |
| A2 | 1.400 | 1.500 | 0.055 | 0.059 |
| A3 | 0.620 | 0.680 | 0.024 | 0.027 |
| b | 0.370 | 0.420 | 0.015 | 0.016 |
| D | 8.710 | 8.910 | 0.343 | 0.347 |
| and | 5.900 | 6.100 | 0.232 | 0.238 |
| E1 | 3.800 | 3.950 | 0.150 | 0.156 |
| and | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.027 |
| L1 | 0.250 (BSC) | | 0.010 (BSC) | |

DIP14

| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-------------------------------|----------------------------|-------------------------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.470 | 1.570 | 0.058 | 0.062 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 19.000 | 19.200 | 0.748 | 0.756 |
| E1 | 6.250 and 6.450 of A | 2.540 (BSC) 7.620 (REF) | 0.246 0.100 (BSC) 0.300 (REF) | 0.254 |
| eB | 7.620 | 9.300 | 0.300 | 0.365 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | | 0.118 | |

SOP16

| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|--------|---------------------|-------|
| | Min | Max | Min | Max |
| A | - | 1.700 | - | 0.066 |
| A1 | 0.100 | 0.200 | 0.004 | 0.008 |
| A2 | 1.420 | 1.480 | 0.056 | 0.058 |
| A3 | 0.620 | 0.680 | 0.024 | 0.027 |
| D | 9.960 | 10.160 | 0.392 | 0.396 |
| and | 5.900 | 6.100 | 0.232 | 0.238 |
| E1 | 3.870 | 3.930 | 0.152 | 0.153 |
| b | 0.370 | 0.430 | 0.015 | 0.017 |
| and | 1.240 | 1.300 | 0.048 | 0.051 |
| L | 0.500 | 0.700 | 0.020 | 0.027 |
| L1 | 1.050 (REF) | | 0.041 (REF) | |
| L2 | 0.250 (BSC) | | 0.010 (BSC) | |

DIP16

| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|--------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.470 | 1.570 | 0.058 | 0.062 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 19.000 | 19.200 | 0.748 | 0.756 |
| E1 | 6.250 | 6.450 | 0.246 | 0.254 |
| and | | | 0.100 (BSC) | |
| of A | 7.620 (REF) | | 0.300 (REF) | |
| eB | 7.620 | 9.300 | 0.300 | 0.365 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | | 0.118 | |



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