Si4432 Errata (Revision V2)

Errata Status Summary

Errata #	Title	Impact	Status
1	TX output power at 18.5 dBm	Minor	Will be fixed in the next revision
2	Spur located at half of the output TX frequency	Minor	Will be fixed in the next revision
3	Spurious behavior near frequencies in multiples of 5 MHz	Minor	Will be fixed in the next revision
4	General purpose ADC in differential mode	Minor	Will be fixed in the next revision
5	RX current consumption does not meet specified data sheet value	Minor	Will be fixed in a future revision
6	Additional tuning steps required for proper RX mode operation	Minor	Software workaround—will be fixed in the next revision
7	30 MHz sensitivity de-sense	Minor	Will be fixed in a future revision
8	Incorrect preamble length in TX packet handler mode	Minor	Will be fixed in the next revision
9	Register modifications needed for correct operation	Minor	Will be fixed in the next revision
10	Device operation below –25 °C	Minor	Software workaround - will be fixed in the next revision
11	Wake Up Timer and Low Duty Cycle mode not functional	Minor	Use the micro or 32 kHz option for these functions. Will be fixed in the next revision
12	Antenna switch control in TX mode	Minor	Software work around available
13	Bi-modal phase noise at 1 kHz and 1 MHz offsets	Major	Will be fixed in the next revision
14	Some non-standard frequencies are not supported	Major	Will be fixed in the next revision
15	Register settings for RSSI	Informational	Will be fixed in the next revision
16	Reference design for harmonics	Informational	New reference design being released
17	LBD voltage read-back	Informational	Will be fixed in a future revision
18	Register modification for data-rates higher than 100 kbps	Informational	
19	Reference design from data sheet version 0.4 should be used	Informational	

Impact Definition: Each erratum is marked with an impact, as defined below:
- Minor: Workaround exists.

- Major: Errata that do not conform to the data sheet or standard.
- Information: The device behavior is acceptable the data sheet will be changed to match the device behavior.

Errata Details

1. **Description**: The TX Output Power is 18.5 dBm compared to the data sheet limit of 20 dBm.

   Impact: Will have impact on range compared to transmitter at +20 dBm.

   Workaround: No workaround exists in the current silicon.

   Resolution: Will be fixed in the next revision.

2. **Description**: A spur can be located at half of the output TX frequency with a maximum value of ~55 dBc.

   Impacts: There is no effect on the performance of the radio, but the spur may effect ETSI compliance.

   Workaround: ETSI compliance is radiated so a typical antenna will likely attenuate the spur to be below the required limit. Testing by Silicon Labs on the recommended reference design using the antenna supplied with the evaluation kits shows the device passes the ETSI unwanted emissions limits with margin.

   Resolution: Will be fixed in the next revision.

3. **Description**: Spurious tones appear when tuned to a frequency that is within a 100 kHz of a frequency that is a multiple of 5 MHz, i.e., 900 MHz ±100 kHz, 905 MHz ±100 kHz.

   Impacts: The RX sensitivity has not shown degradation but the TX spectrum exhibits spurious tones.

   Workaround: Avoid using channels within 100 kHz of frequencies that are multiples of 5 MHz.

   Resolution: Will be fixed in the next revision.

4. **Description**: The general purpose ADC does not functional in differential mode.

   Impacts: Only able to use the general purpose ADC in single-ended mode.

   Workaround: No work-around exists.

   Resolution: Will be fixed in the next revision.

5. **Description**: RX current does not meet specified value in data sheet .

   Impacts: The battery life may be affected.

   Workaround: Use the recommend register settings to adjust the current consumption.

   Resolution: Problem will be addressed in a future die revision.

6. **Description**: Additional tuning steps are required for proper RX mode operation.

Impacts: Tuning can fail if additional steps are not implemented in customer firmware.

Workaround: The following steps should be followed to ensure proper operation:

1. Program desired RX frequency minus 937.5 kHz: *Program registers 75h, 76h, and 77h*
2. Program tune mode: *Program register 07h bit 1 (pllon = 1)*
3. Disable VCO calibration: *Program register 55h bit 0 (skipvco = 1)*
4. Program desired RX frequency: *Program registers 75h, 76h, and 77h*
5. Program RX mode: *Program register 07h bit 2 (rxon = 1)*
6. Implement normal operation.

Resolution: Will be fixed in the next revision.

7. **Description**: When tuned to a channel that is a multiple of 30 MHz sensitivity is degraded.

   Impacts: Sensitivity will not meet specified value.

   Workaround: Avoid using channels that are a multiple of 30 MHz. Contact Silicon Labs' customer support for instructions on shifting the XTAL frequency if a specific frequency is required.

   Resolution: Will be fixed in the future revision.

8. **Description**: In FSK/GFSK TX mode the preamble length is one bit less than the programmed value.

   Impacts: Preamble length will be one bit less than expected if the packet handler is used in TX mode. For example, if a 32-bit preamble is selected to be added to the data payload only 31 bits will be added.

   Workaround: Add an extra nibble of preamble to the preamble length register or do not use the automatic packet handler in TX mode.

   Resolution: Will be fixed in the next revision.

9. **Description**: Register modifications needed for correct operation.

   Impacts: PLL, RX and TX current consumption.

   Workaround: Change Registers 59 = 00, 5A = 03h, and 66 = 02h.

   Resolution: Default values will be updated in the next revision.

10. **Description**: Device operation below –25 °C.

    Impacts: Frequency tuning.

    Workaround: Set register 65h to A1h prior to the PLL being enabled for the device to operate correctly at cold temperatures.

    Resolution: Will be fixed in the next revision.

11. **Description**: Wake-up Timer and Low Duty Cycle Modes not functional.

Impacts: These features are not supported.

Workaround: Use the external microcontroller or the 32 kHz XTAL option on the Si4432 to implement these functions.

Resolution: Will be fixed in the next revision.

12. **Description**: In antenna diversity mode the antenna selected for the RX packet may not be the same as the subsequent TX. The TX antenna selection will toggle between both antennas.

    Impacts: May impact link performance depending on conditions.

    Workaround: Customers can force the TX antenna control manually to a given antenna prior to sending the TX packet by setting the ANTDIV[2:0] bits in register 08h.

    Resolution: Will be fixed in the next revision.

13. **Description**: Phase Noise at 100 kHz and 1 MHz offsets can occasionally jump to be out of spec by 5 dB.

    Impacts: The 5 dB shift may impact adjacent channel selectivity and TX spectral mask.

    Workaround: The issue has a bi-modal nature and can toggle between two states of phase noise.

    Resolution: Will be fixed in the next revision.

14. **Description**: Some non-standard frequencies are not supported.

    Impacts: Operation in frequencies between 240–280 MHz and 480–560 MHz should be avoided.

    Workaround: These are non-standard bands and should result in no customer impact; no workaround at this time.

    Resolution: Will be fixed in the next revision.

15. **Description**: RSSI is not correct using default settings.

    Impacts: No impact.

    Workaround: Set the following registers: Reg 6Ah lnacomp[3:0] = 0010 and pgathres[1:0] = 11.

    Resolution: Will be fixed in the next revision.

16. **Description**: The reference design listed in the data sheet does not meet the specified harmonic suppression as listed in the data sheet.

    Impacts: May not meet harmonic specification with listed reference design.

    Workaround: Contact Silicon Labs' customer support for a new reference design.

    Resolution: Change Low Pass Filter Reference Design.

17. **Description**: LBD voltage read-back can occasionally be incorrect. If the LBD battery voltage register is read during the same cycle that the register is being updated, it will read the previously read value and not the updated value. The LBD measurement cycle is 250 μs and the update period is 30 μs.

    Impacts: May need to use majority polling or use the LBD interrupt instead.

    Workaround: Read the register two or three consecutive times to ensure it is correct or use the LBD interrupt.

    Resolution: Will be fixed in the future revision.

18. **Description**: For TX data rates higher than 100 kbps a register change is required. The cpcurr[1:0] bits in Reg 58h should be changed to 11 (default = 01).

    Impacts: May slightly degrade phase noise in the 100 to 300 kHz region.

    Workaround: Change Reg 58h to 11.

    Resolution: None planned.

    Workaround: If random selection of the TX antenna is not desired, then a single antenna may be manually selected by using the antdiv register in 08h.

    Resolution: Will be fixed in the next revision.

19. **Description**: Use the PA Reference Design in data sheet revision 0.4

    Impacts: Not using the reference design on data sheet 0.4 may create a maximum voltage swing higher than expected on the PA output.

    Workaround: See data sheet.

    Resolution: Informational only.