Digital Circuit Design

UE17CS203

Open End Experiment

Topic : 4x4 Unsigned Multiplier Using Full Adders

Name : Ratan Gundami

SRN : PES1201701556

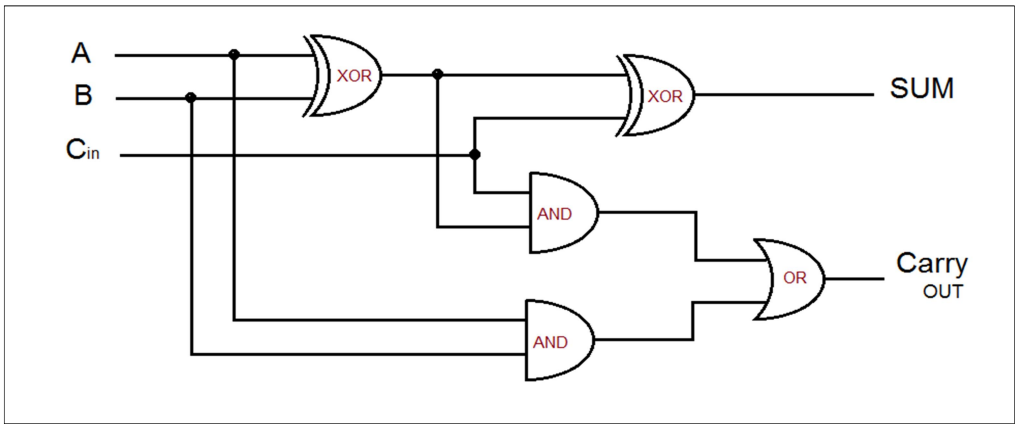
Verilog Code

Design Module

Full Adder :

```
module Full_Adder(
        input x, y, cin,
        output s, cout
        );

wire c1,c2,c3;
xor(s,x,y,cin);
and a1(c1,x,y);
and a2(c2,x,cin);
and a3(c3,y,cin);
or(cout,c1,c2,c3);

endmodule
```

Logic Diagram of Full Adder



4x4 Multiplier:

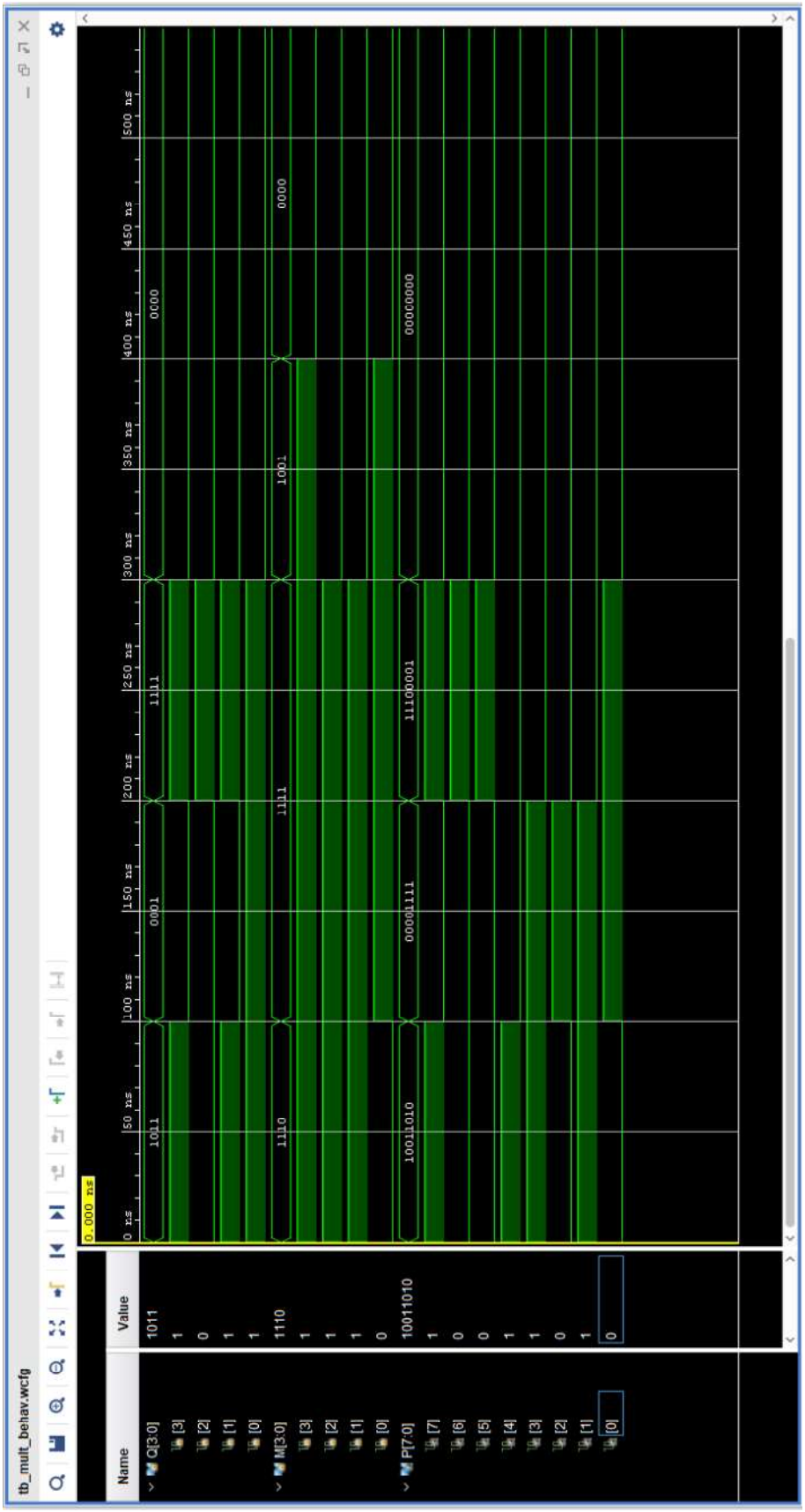
```
module M4bit(
        input [3:0] Q,
        input [3:0] M,
        output [7:0] P
        );

wire c1,c2,c3,c4,c5,c6,c7,c8,c9,c10,c11;
wire d1,d2,d3,d4,d5,d6,d7;
wire e1,e2,e3;
wire f1,f2,f3,f4,f5,f6,f7;
wire g1,g2,g3,g4;

and A1(c1,M[3],Q[1]);
and A2(c2,M[2],Q[2]);
and A3(c3,M[1],Q[3]);
and A4(c4,M[3],Q[0]);
and A5(c5,M[2],Q[1]);
and A6(c6,M[1],Q[2]);
and A7(c7,M[2],Q[0]);
and A8(c8,M[1],Q[1]);
and A9(c9,M[0],Q[2]);
and A10(c10,M[1],Q[0]);
and A11(c11,M[0],Q[1]);
and A12(P[0],M[0],Q[0]);
```

```
Full_Adder fa1(c1,c2,c3,d2,d1);
Full_Adder fa2(c4,c5,c6,d4,d3);
Full_Adder fa3(c7,c8,c9,d6,d5);
Full_Adder fa4(c10,c11,0,P[1],d7);

and A13(e1,M[2],Q[3]);
and A14(e2,M[3],Q[2]);
and A15(e3,M[0],Q[3]);

Full_Adder fa5(e1,e2,d1,f2,f1);
Full_Adder fa6(d2,d3,f5,f4,f3);
Full_Adder fa7(d4,e3,d5,f6,f5);
Full_Adder fa8(d6,d7,0,P[2],f7);

and A16(g1,M[3],Q[3]);

Full_Adder fa9(g1,f1,g2,P[6],P[7]);
Full_Adder fa10(f2,f3,g3,P[5],g2);
Full_Adder fa11(f4,0,g4,P[4],g3);
Full_Adder fa12(f6,f7,0,P[3],g4);

endmodule
```

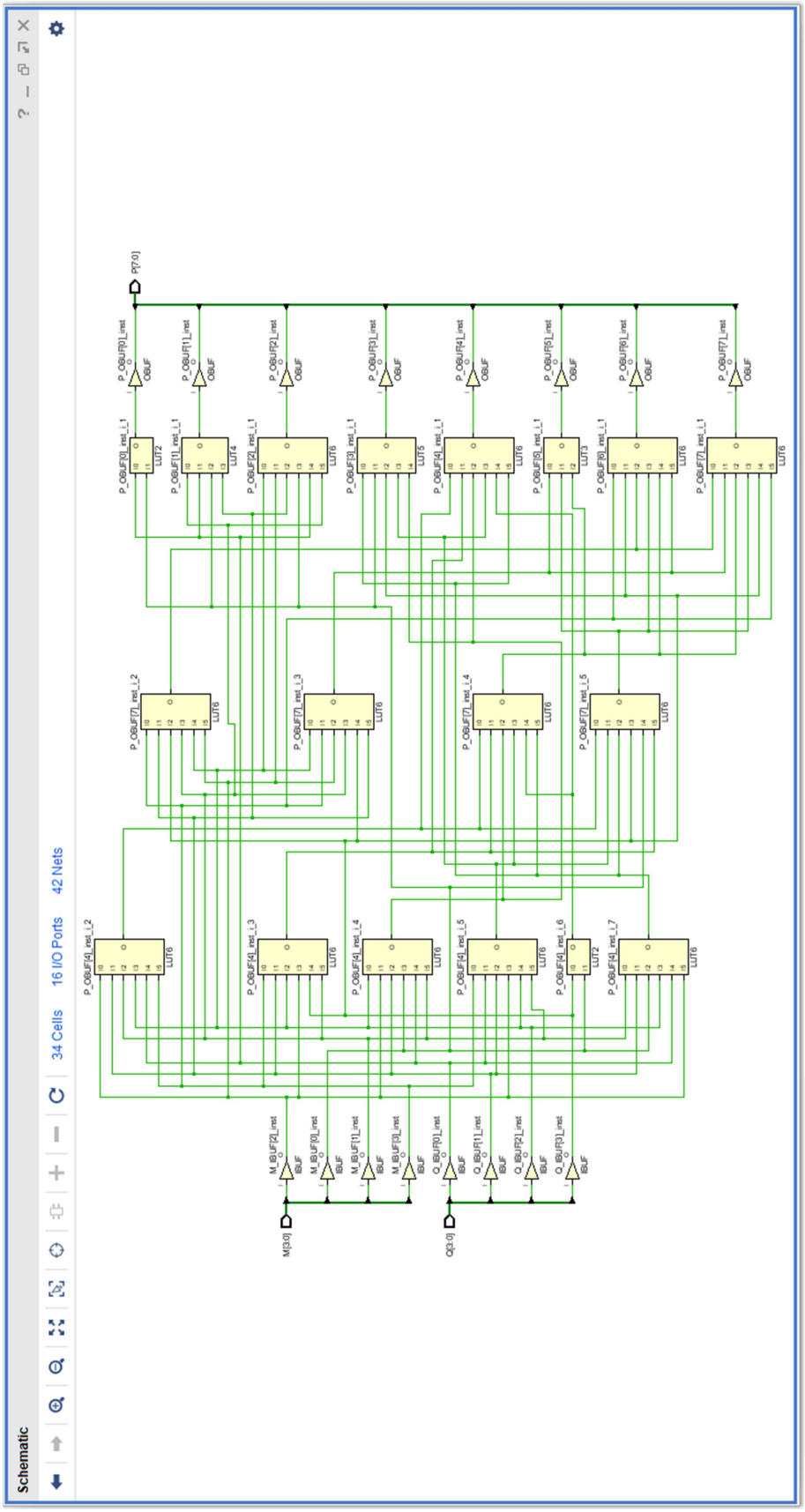
Test Bench

```
module tb_mult;
reg [3:0] Q;
reg [3:0] M;
wire [7:0] P;

M4bit dut(Q, M, P);

initial begin
    Q = 11;
    M = 14;

#100 Q = 1;
    M = 15;

#100 Q = 15;
    M = 15;

#100 Q = 0;
    M = 9;

#100 Q = 0;
     M = 0;

end
endmodule
```

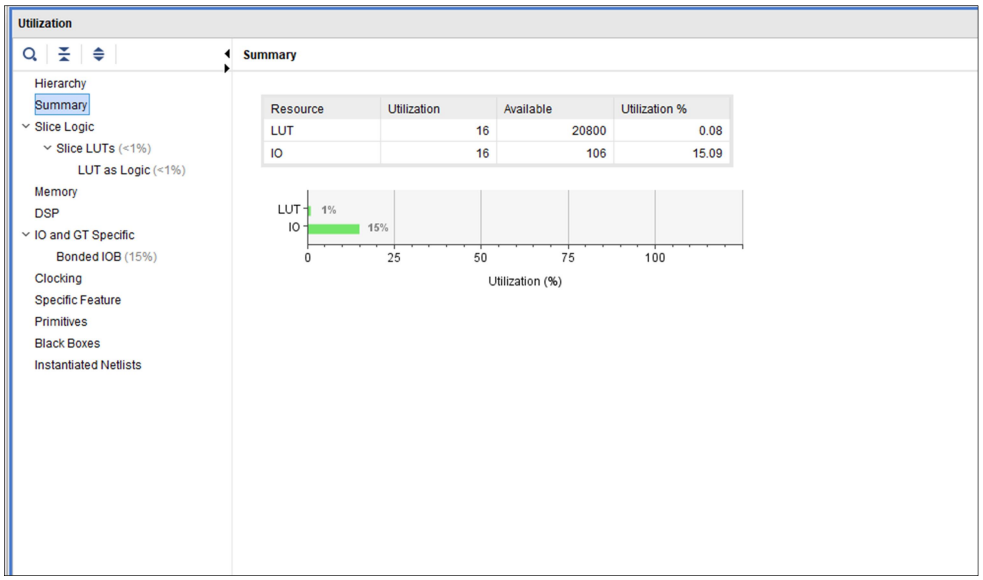
Waveform


tb_mult_behav.wcfg
Name
Value
Q[3:0]
1011
M[3:0]
1110
P[7:0]
10011010
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
500 ns
0.000 ns
1011
0001
1111
1110
1111
1001
0000
10011010
00001111
11100001
00000000

Schematic Diagram (After Synthesis)



Synthesis Report Utlization



Sample Truth Table of 4 bit Multiplier

A	A3	A2	A1	A0	B	B3	B2	B1	B0	P	P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	**6**	0	1	1	0	**0**	0	0	0	0	0	0	0	0
1	0	0	0	1	**13**	1	1	0	1	**13**	0	0	0	0	1	1	0	1
3	0	0	1	1	**9**	1	0	0	1	**27**	0	0	0	1	1	0	1	1
6	0	1	1	0	**5**	0	1	0	1	**30**	0	0	0	1	1	1	1	0
7	0	1	1	1	**7**	0	1	1	1	**49**	0	0	1	1	0	0	0	1
9	1	0	0	1	**8**	1	0	0	0	**72**	0	1	0	0	1	0	0	0
11	1	0	1	1	**3**	0	0	1	1	**33**	0	0	1	0	0	0	0	1
14	1	1	1	0	**12**	1	1	0	0	**168**	1	0	1	0	1	0	0	0
13	1	1	0	1	**14**	1	1	1	0	**182**	1	0	1	1	0	1	1	0
15	1	1	1	1	**15**	1	1	1	1	**225**	1	1	1	0	0	0	0	1

Schematic Diagram (Before Synthesis)