CS 232 - Assignment 5

1) Design a mod-10 up-down counter. As long as 'up'=1, the value of 'count' should increase by '1' every clock cycle. As long as 'up'=0, the value of 'count' should decrease by '1' every clock cycle. 'clk' is the input clock signal and 'rst' the reset signal input.

```
entity Mod10UpDown is
        port ( clk, rst, up : in std_logic;
        count: out std_logic_vector (3 downto 0) );
end entity;
```

2) Design a 4-bit Booth multiplier. 'a' and 'b' are the 4-bit unsigned input numbers and 'result' is the 8-bit multiplication result.

```
entity BoothMultiplier is
        port ( clk, rst : in std_logic;
        a, b : in std_logic_vector  (3 downto 0);
        result : out std_logic_vector (7 downto 0) );
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components (.vhd or .vhdl files).
2. Screenshot of Waveforms (Few input patterns are sufficient).
3. A report explaining how you designed (pdf format).

Submission rules:

1. **Deadline:** Tuesday (16th Feb 2022), 23:59 pm.
2. Create a folder named **lab5** (all small letters and no spaces).
3. Inside the above-mentioned folder create 2 more folders named **q1** and **q2** (all small letters and no spaces).

4. Inside the folder, **q1** put all the .vhd or .vhdl files of both top-level entity and sub-components. Also in the same folder put the related waveform screenshots and pdf report related question1. Do the same thing for **q2.**
5. Finally, before you submit the lab5 folder on moodle you will be zipping it. The zip file should have your id number as the name. For eg: if your id is 184070026 then your zip file will be 184070026.zip.