IITB-RISC

CS230 project - MULTI-CYCLE IMPLEMENTATION

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Microprocessor design

- *State elaboration*

S0	$PC \rightarrow T\_MEM (A), ALU1$ $I\_MEM (D) \rightarrow IR$ $+1 \rightarrow ALU1$ $ALU \rightarrow T4$
S1	$I_{15-12} \rightarrow$ (Decide next state) (Decoder)
S2	$I_{11-9} \rightarrow RF_{A1}$ $I_{8-6} \rightarrow RF_{A2}$ $RF_{D1} \rightarrow T1$ $RF_{D2} \rightarrow T2$ $T4 \rightarrow PC$
S3	$T1 \rightarrow ALU2$ $T2 \rightarrow ALU2$ $ALU2 \rightarrow T3$
S4	$T3 \rightarrow RF_{D3}$ $IR_{5-3} \rightarrow RF_{A3}$
S5	$IR_{11-9} \rightarrow RF_{A1}$ $RF_{D1} \rightarrow T1$
S6	$T1 \rightarrow ALU2$ $IR_{5-0} \rightarrow SE5 \rightarrow ALU2$ $ALU2 \rightarrow T3$
S7	$T3 \rightarrow RF_{D3}$ $IR_{8-6} \rightarrow RF_{A3}$

S8	$I_{8-6} \rightarrow RF_{A1}$ $RF_{D1} \rightarrow T1$
S9	$T1 \rightarrow ALU2$ $IR_{5-0} \rightarrow SE5 \rightarrow ALU2$ $ALU2 \rightarrow T3$
S10	$T3 \rightarrow MEM\_ADDR$ $MEM\_DATA\_OUT \rightarrow T3$
S11	$T3 \rightarrow RF_{D3}$ $I_{8-6} \rightarrow RF_{A3}$
S12	$I_{11-9} \rightarrow RF_{A2}$ $RF_{D2} \rightarrow T2$
S13	$T3 \rightarrow MEM\_ADDR$ $T2 \rightarrow MEM\_DATA\_IN$
S14	$IR_{8-0} \rightarrow LS7 \rightarrow RF_{D3}$ $I_{11-9} \rightarrow RF_{A3}$
S15	$I_{11-9} \rightarrow RF_{A3}$ $T4 \rightarrow RF_{D3}$ $PC \rightarrow ALU$ $IR_{5-0} \rightarrow SE5 \rightarrow ALU2$ $ALU \rightarrow PC$

S16	$I_{11-9} \rightarrow RF_{A3}$ $T4 \rightarrow RF_{D3}$ $I_{8-6} \rightarrow RF_{A2}$ $RF_{D2} \rightarrow PC$
S17	$I_{11-9} \rightarrow RF_{A1}$ $RF_{D1} \rightarrow T1$
S18	$T1 \rightarrow ALU$ $IR_{8-0} \rightarrow SE8 \rightarrow ALU$ $ALU \rightarrow PC$

S19	$I_{11-9} \rightarrow RF_{A1}$ $I_{8-6} \rightarrow RF_{A2}$ $RF_{D1} \rightarrow T1$ $RF_{D2} \rightarrow T2$
S20	$T1 \rightarrow ALU2$ $T2 \rightarrow ALU2$ $ALU2 \rightarrow T3$
S21	$PC \rightarrow ALU$ $IR_{5-0} \rightarrow SE5 \rightarrow ALU2$ $ALU \rightarrow PC$