ASSIGNMENT 1
COMPUTER ARCHITECTURE

RATNA SAI KIRAN
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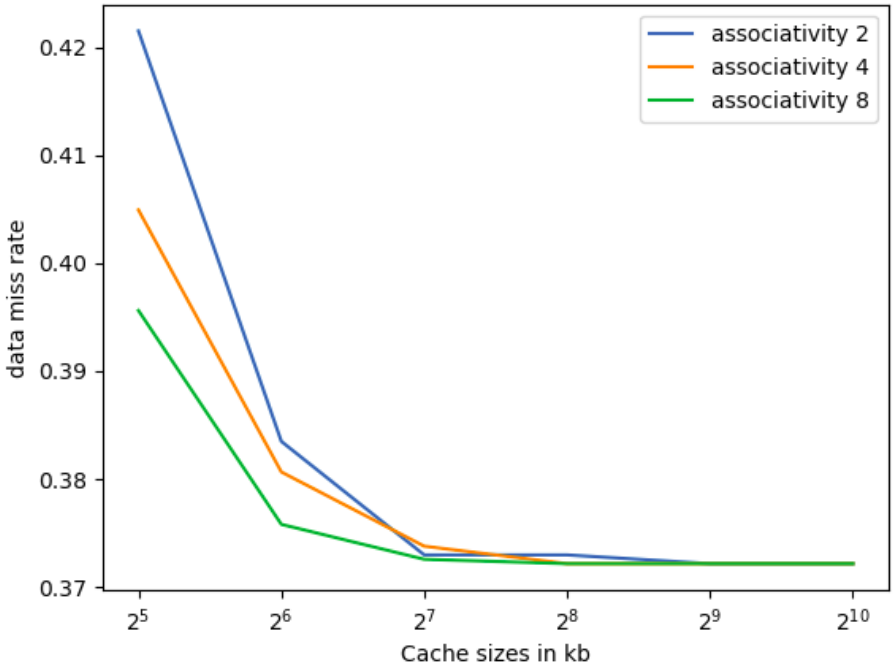
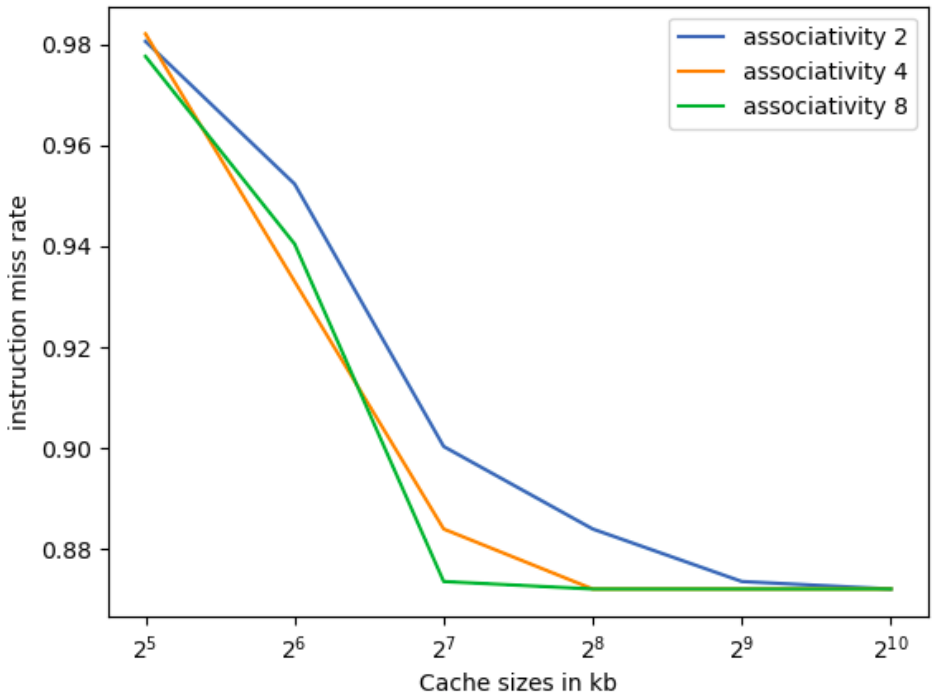
2 I have simulated with different L2 sizes =[32,64,128,256,512,1024] KB
For different associativity 2,4,8

Below are the graphs

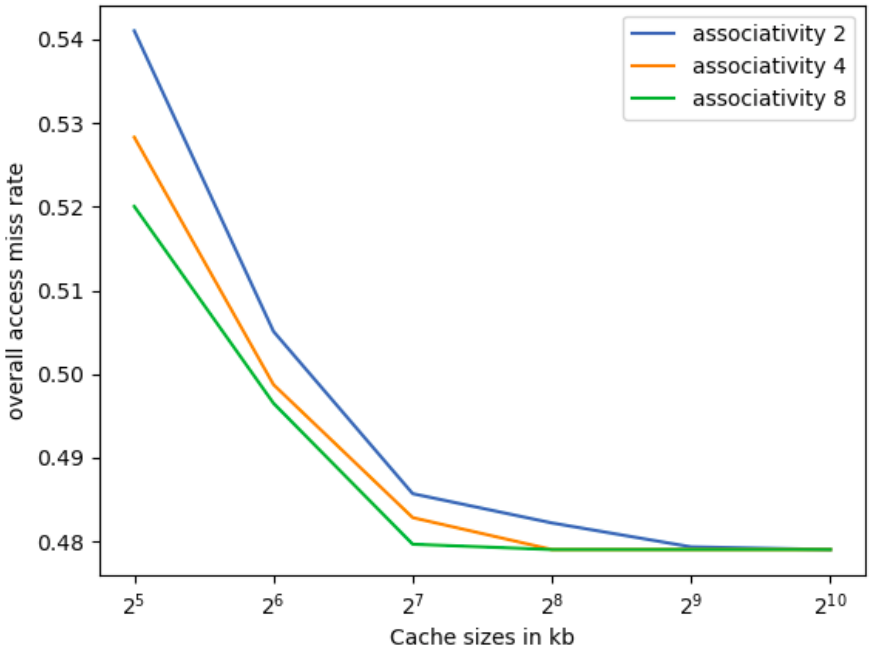
Data Miss Rate



Instruction Miss rate



Overall access miss rate



2

b.By increasing the cache size we can reduce miss rate but also by increasing the associativity we can reduce the miss rate for same cache sizes..It is also evident from the graphs that after increasing the cache size(at larger sizes) there is no change in the miss rate.