Linear Discriminant Analysis

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Introduction

Definition : Linear Discriminant Analysis (LDA) is most commonly used as dimensionality reduction technique in the pre-processing step for pattern-classification and machine learning applications.

Objective : The objective of the LDA is to project the original data matrix onto lower dimensional space.
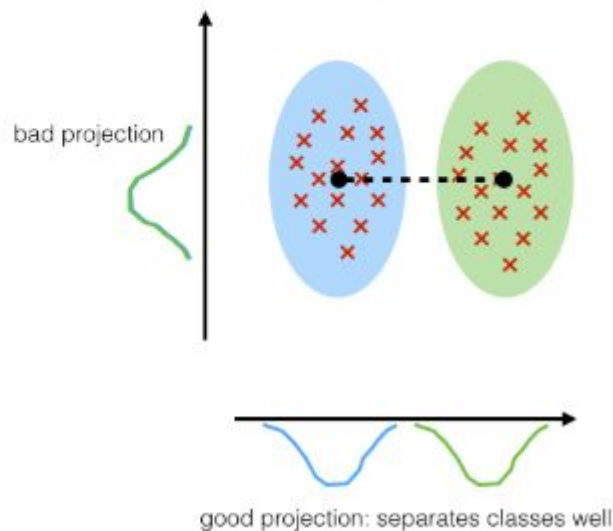
Introduction
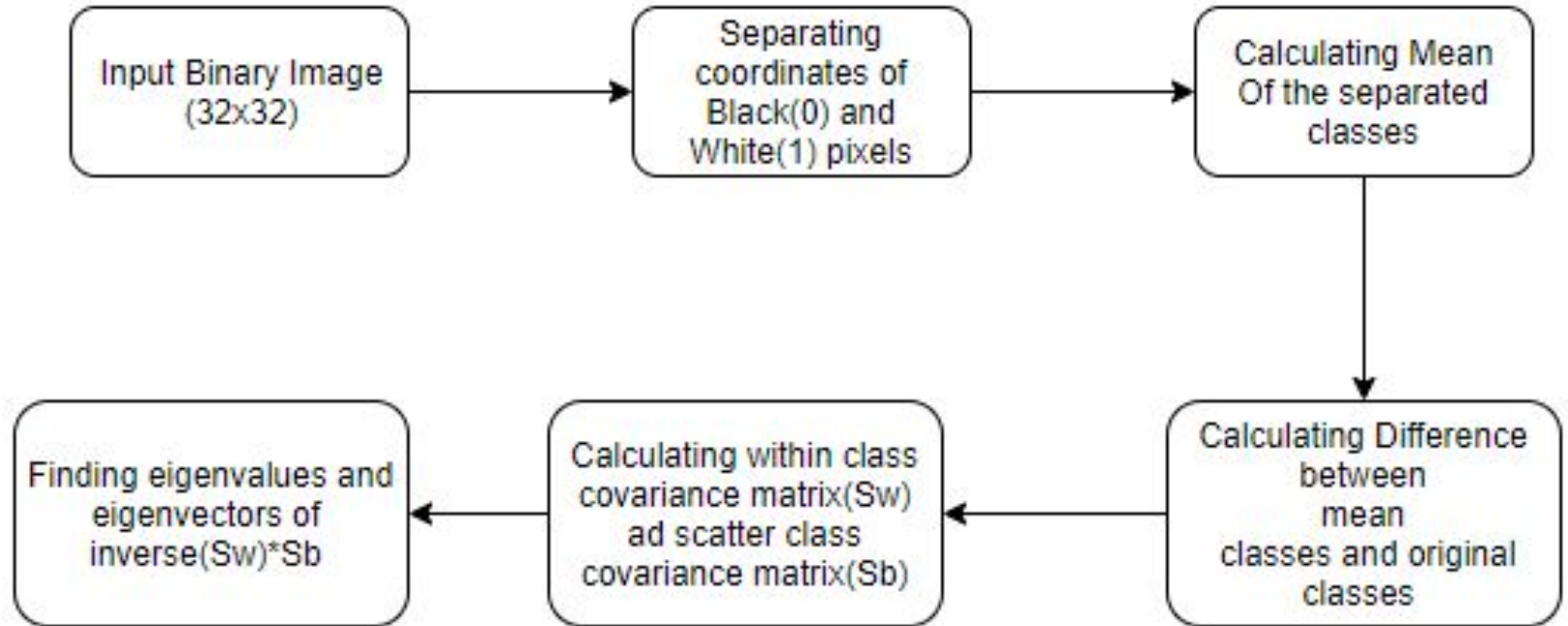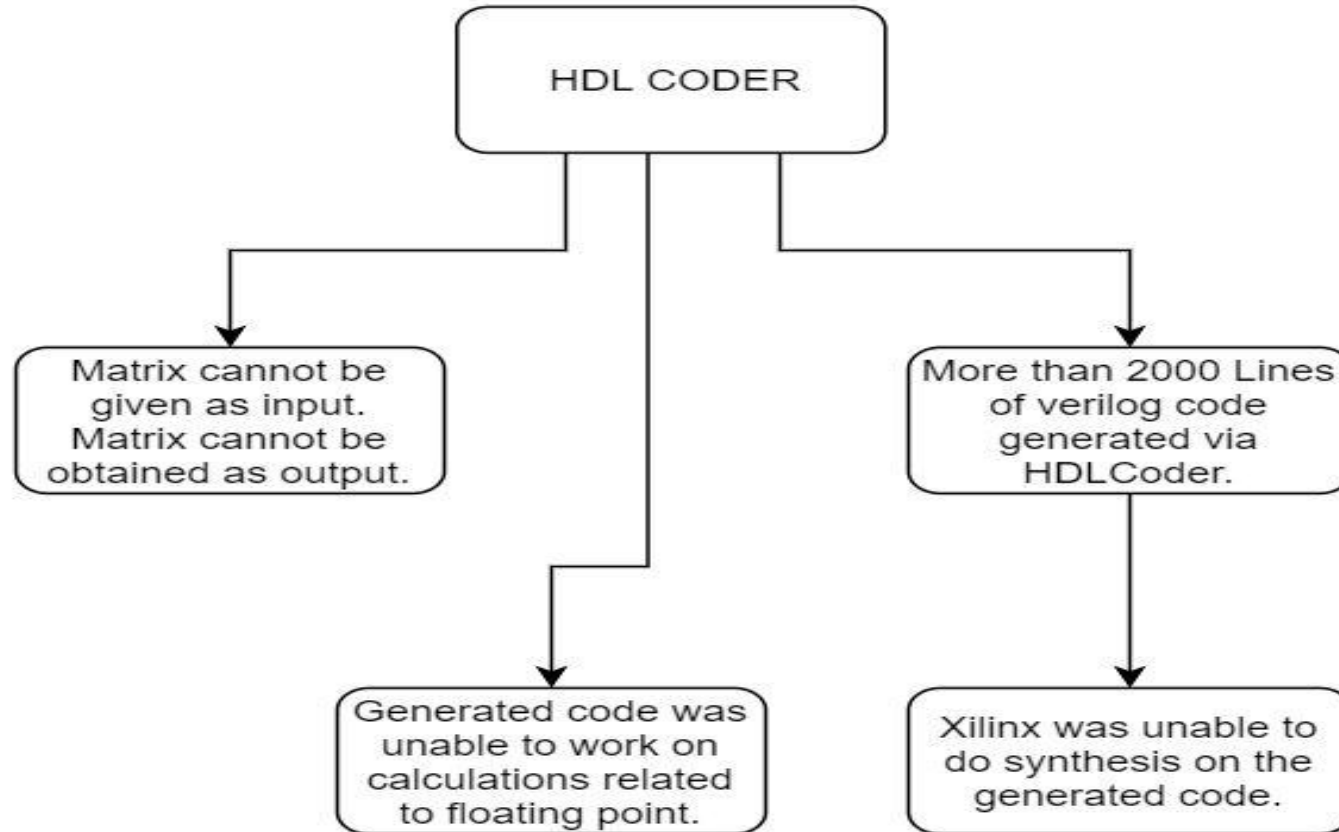

PCA: component axes that maximize the variance
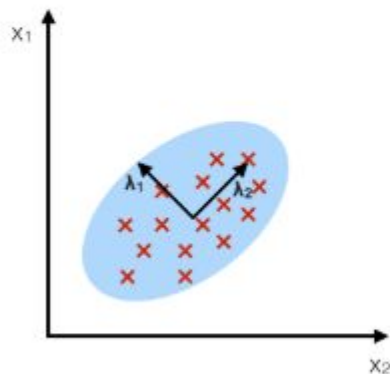
LDA: maximizing the component axes for class-separation

Existing Approaches(Matlab Scripting):

Difficulties Faced Using HDL Coder:


```
                        HDL CODER


    Matrix cannot be                      More than 2000 Lines
    given as input.                          of verilog code
    Matrix cannot be                         generated via
    obtained as output.                       HDLCoder.


            Generated code was          Xilinx was unable to
            unable to work on           do synthesis on the
            calculations related        generated code.
            to floating point.
```

Different Algorithms Researched:

Algorithm For Square Root:
1)Restoring Algorithm
2)Non-Restoring Algorithm

Algorithm For Division:
1)Non-Restoring Algorithm For Division

Reason Not To Use These Algorithms:
These algorithms were mainly used for fixed point number or integers and so, floating point calculations were difficult to be solved.

For Floating Point Calculations:

- We use online available FPU(Floating Point Unit).
- Features Of FPU:
  1)Input can be given as standard IEEE-754 floating point format.
  2)Output generated is also in the standard IEEE-754 floating point format.
- FPU Used For:
  1)Addition
  2)Subtraction
  3)Multiplication
- Advantages Of using FPU:
  1)Any of the above operations can be performed in 1 clock cycle.

Using IP CORE:

- The use of IP core in our project is for calculating **division** and **square root** of floating point inputs.
- Input: 32 Bit Floating Point(IEEE 754 Floating Point Representation, Single Precision).
- Output: 32 Bit Floating Point(IEEE 754 Floating Point Representation, Single Precision).
- Limitations Of using IP CORE:
  1)IP core takes 40 clock cycles for calculation of division and square root of floating point inputs.