MADHAV INSTITUTE OF TECHNOLOGY & SCIENCE, GWALIOR (M.P.), INDIA

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DEPARTMENT OF ELECTRONICS ENGINEERING

2024

A SKILL BASED MINI PROJECT

REPORT ON

"Design and Verify the 180 nm CMOS based EXNOR gate on LT Spice."

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS ENGINEERING

SUBMITTED BY:

RATNESH ASATI

EC 5TH SEM

(0901EC221087)

SUBMITTED TO:

DR. VARUN MISHRA

ASSISTANT PROFESSOR

DEPT. OF ELECTRONICS

CERTIFICATE

This is to certify that the mini project report entitled **"Design and Verify the 180 nm CMOS based EXNOR gate on LT Spice."** submitted by Ratnesh Asati has been carried out under the guidance of **Dr. Varun Mishra**, Electronics Engineering, Madhav Institute of Technology & Science, Gwalior. The project report is approved for submission requirement for Mini Project in 5th semester in Electronics Engineering, from Madhav Institute of Technology & Science, Gwalior (M.P).

SUBMITTED TO:

DR. VARUN MISHRA

(Department Of Electronics Engineering)

SUBMITTED BY:
RATNESH ASATI
(0901EC221087)

DECLARATION

I hereby declare that the project work entitled **"Design and Verify the 180 nm CMOS based EXNOR gate on LT Spice."** submitted to the Madhav Institute of Technology & Science Gwalior, is a record of an original work done by me under the guidance of **Dr. Varun Mishra**, Department of Electronics Engineering.

The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Ratnesh Asati

(0901EC221087)

Date: 19/11/2024

Place: MITS, GWALIOR

ACKNOWLEDGEMENT

We would like to express our gratitude towards **Dr. Varun Mishra**, for his support in accomplishment of our project on **"Design and Verify the 180 nm CMOS based EXNOR gate on LT Spice."**.

I would like to extend my deep appreciation to all my group members, without their support and coordination we would not have been able to complete this project.

Finally, as one of the team members, I would like to appreciate all my group members for their support and coordination, I hope we will achieve more in our future endeavours.

Ratnesh

Ratnesh Asati

(0901EC221087)

Date: 19/11/2024

Place: MITS, GWALIOR

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Design and Verify the 180 nm CMOS based EXNOR gate on LTSpice.

INTRODUCTION:

CMOS stands for **C**omplementary **M**etal **O**xide **S**emiconductor. And CMOS based logic gates uses complementary pair of NMOS and PMOS transistors. When MOS transistors are used as logic gate then they are used as a switch. By controlling the gate to source voltage, PMOS and NMOS transistor can be used as a switch. And they can be used to design a logic gate.
CMOS logic uses both NMOS and PMOS transistors. The PMOS transistors are used as pull-up network and NMOS transistors are used as pull-down network. And because of that, the **static power consumption of the CMOS based logic gates and logic circuit is very low compared to the logic gates which is designed using only either NMOS or PMOS transistors.** Moreover, **CMOS based logic gates has higher noise margin compared to NMOS and PMOS based logic gates.**

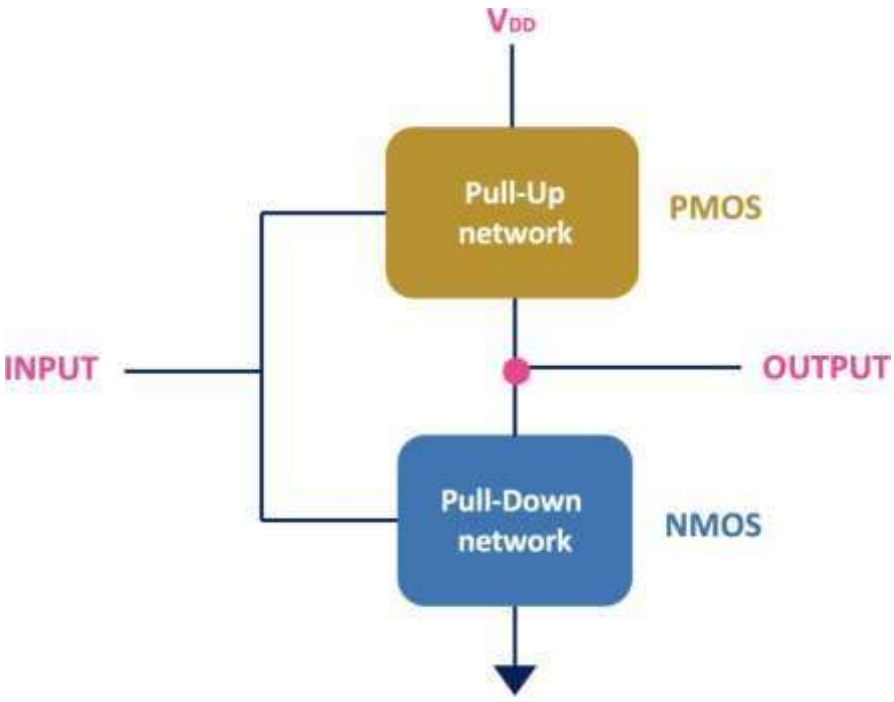


Figure 1

PMOS transistor is used as a pull-up transistor, so its source is connected to supply voltage and drain is connected to the output node.

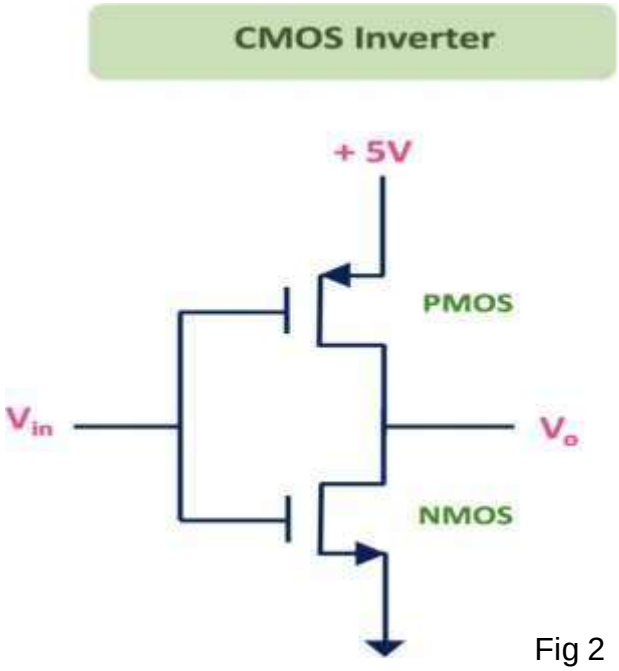
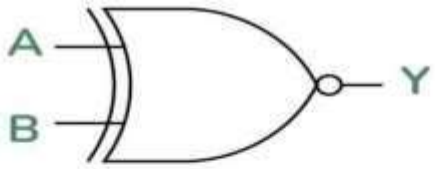


Fig 2

Similarly, the NMOS transistor is used as a pull-down transistor. That means its source terminal is connected to ground terminal and drain is connected to output node. And the gate terminals of both PMOS and NMOS transistor is connected to the input.

The XNOR (Exclusive NOR) gate is useful in digital electronics, producing a true output only when its two binary inputs are identical. This makes it valuable for applications like equality detectors and arithmetic operations. The Boolean expression for the XNOR gate is $Y=AB+\bar{}AB$
Meaning the output (Y) is true when both inputs (A) and (B) are either true or false.



Truth Table

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Fig 3

The truth table shows that the XNOR gate outputs 1 when both inputs are the same and 0 when the inputs differ. This verification is required for ensuring the XNOR gate's practical circuits align with theoretical expectations.

CMOS Implementation of XNOR Gate

Implementing an XNOR gate using CMOS technology involves constructing pull-up and pull-down networks with PMOS and NMOS transistors, respectively. CMOS is favoured for its low power consumption and high noise immunity. The circuit design is based on the Boolean expression ($Y=AB+\bar{}AB$).

Pull-up network (PMOS transistors): This will implement the logic where output Y is high (1).
Pull-down network (NMOS transistors): This will implement the logic where output Y is low (0).

The circuit consists of multiple PMOS and NMOS transistors, connected to implement the XNOR logic function.

Schematic of the CMOS XNOR Gate

PMOS Transistors: Two PMOS transistors will be in parallel for the pull-up network, representing the logic where the output is high when the inputs are equal.

NMOS Transistors: Two NMOS transistors will be in series for the pull-down network, representing the logic where the output is low when the inputs are different.

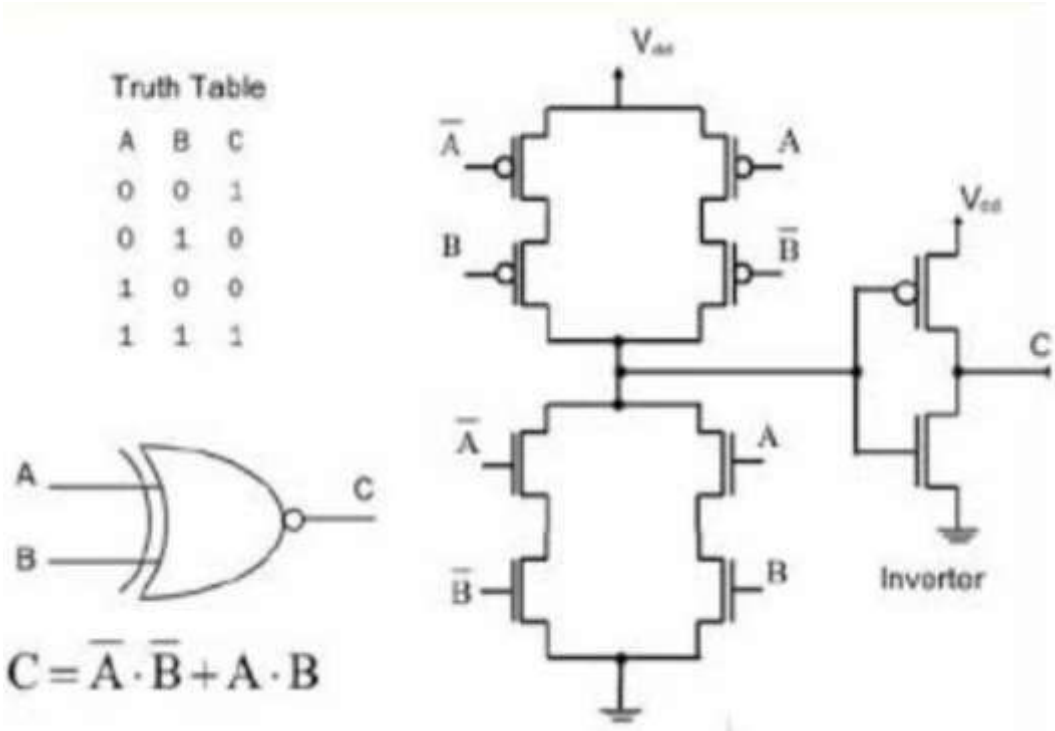


Figure 4

Circuit:

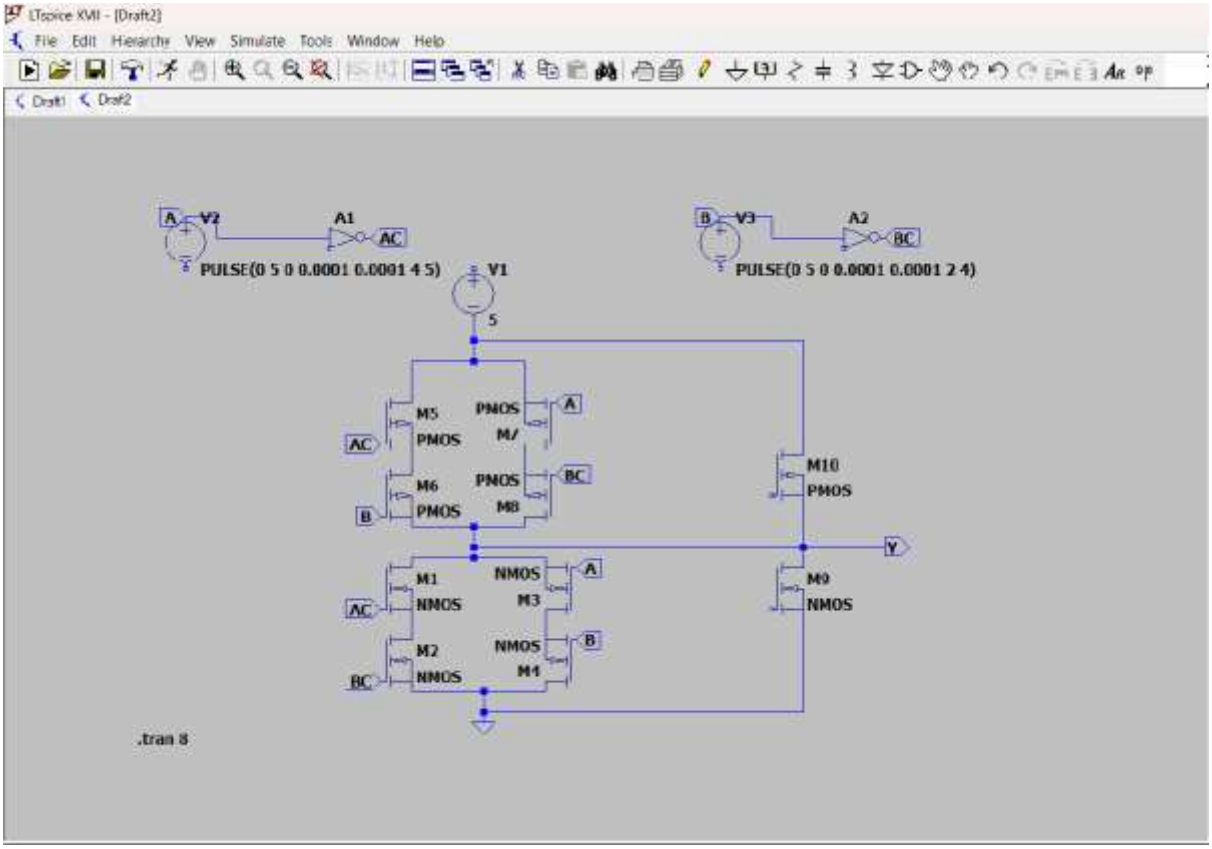


Figure 5:Circuit Simultation

Result:

Figure 6:Output waveform

CONCLUSION

The XNOR, designed using CMOS technology, are valuable in digital electronics, the XNOR gate, needed for equality comparisons, demonstrate CMOS technology's efficiency in creating reliable, low-power circuits. The Transmission Gate exemplifies CMOS adaptability in signal management and switching. Understanding these gates' designs and applications enhances knowledge of digital logic design and highlights CMOS technology's importance in modern electronics.

The CMOS-based XNOR gate function correctly, and you can verify its performance through LTSpice simulations. By carefully simulating the gate, you can ensure that it operates as expected at a 180 nm process node