CSE 231 Course Outline

Digital Logic (North South University)

NORTH SOUTH UNIVERSITY

Centre of Excellence in Higher Education

DEPARTMENT OF Electrical and Computer Engineering

School of Engineering and Physical Sciences

Course Schedule/Timing: Lecture – 3 Hours/week, Lab – 3 Hours/week

1. **Course Number and Title:** **CSE231 Digital Logic Design**
   CSE231L Digital Logic Design Laboratory

   Instructor: Tanzilur Rahman (Tnr)

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   Office Hours: Check My Routine

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   Course Web: https://sites.google.com/site/neuro11school/

   Lecture Time: ST 9:40 – 11:10

   Lab Room: Digital Microprocessor Laboratory, 5th Floor of SAC Building

2. **Course Summary:**

   This course provides an introduction to logic design and basic tools for the design of digital logic systems. A basic idea of number systems will be provided, followed by a discussion on combinational logic: logic gates, Boolean algebra, minimization techniques, arithmetic circuits (adders, subtractors), basic digital circuits (decoders, encoders, multiplexers, shift registers), programmable logic devices (PROM, PAL, PLA). The course will then cover sequential circuits: flip-flops, state transition tables and diagrams, state minimization, state machines, design of synchronous/asynchronous counters, RAM/ROM design. An introduction to programmable logic will also be provided. Hands-on experience will be provided through project on design of a sequential logic system. This course has separate mandatory laboratory session every week as CSE 231L.

3. **Course Objective:**

The objectives of this course are

a. to introduce Boolean logic operation and Boolean Algebra
b. to teach students how to use Boolean Algebra and K-maps to realize two-level minimal/optimal combinational circuits
c. to exposed students in the introductory design process of combinational and sequential circuits
d. to teach the operation of latches, flip-flops, counters and registers.
e. to explain how to analyze and design sequential circuits built with various flip-flops.
f. to introduce using simulation tool for digital system design.

4. Course Outcomes (COs):

Upon successful completion of this course, students will be able to

Sl.	CO Description	Weightage (%)
CO1	apply principles of Boolean algebra to logic functions.	10%
CO2	use K-maps to realize two-level minimal/optimal combinational circuits with up to 4-5 variables	10%
CO3	construct gate-level implementation of a combinational logic function using fundamental logic gates (AND/OR/NOT), Multiplexers, Decoders and Programmable logic gates (ROMs, PLAs and PALs)	30%
CO4	analyze and Design sequential circuits built with various flip-flops, registers, counters	30%
CO5	use simulation tool (e.g. Logisim) to construct Digital Logic Circuit in schematic level	5%
CO6	operate laboratory equipment build, and troubleshoot simple combinational and sequential circuits	20%

5. Mapping of CO-PO

Sl.	CO Description	POs	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	**Apply** principles of Boolean algebra to logic functions.	**a**	Cognitive/ Apply	Lectures, notes	Quiz, Exam
CO2	**Use** K-maps to realize two-level minimal/optimal combinational circuits with up to 4-5 variables.	**c**	Cognitive/ Apply	Lectures, notes	Quiz, Exam

CO3	**Construct** gate-level implementation of a combinational logic function using fundamental logic gates (AND/OR/NOT), Multiplexers, Decoders and Programmable logic gates (ROMs, PLAs and PALs)	**c**	Cognitive/ Create	Lectures, notes	Exam, Design Project
CO4	**Analyze** and **Design** sequential circuits built with various flip-flops, registers, counters	**c**	Cognitive/ Create	Lectures, notes	Exam, Design Project
CO5	**Use** simulation tool (e.g. Logisim) to construct Digital Logic Circuit in schematic level	**e**	Cognitive/ Apply, Psychomotor/ Manipulation	Lab class	Lab work, Design Project
CO6	**Operate** laboratory equipment **build**, and **troubleshoot** simple combinational and sequential circuits	**e**	Cognitive/ Remember, Psychomotor/ Precision	Lab class	Lab work, Design Project

6. Resources

Text books:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	M Morris Mano & M D Ciletti	2012	Digital Design	5th ed.	Pearson Education	ISBN-13: 978-0-13-277420-8

Reference books:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	J F Wakerly	2005	Digital Design: Principles and Practices	4th ed.	Prentice Hall	ISBN-13: 978-0131863897

7. Weightage Distribution among Assessment Tools

Assessment Tools	Theory Weightage (%)
Class Performance	**5**
Assignment	**5**
Quizzes	**10**
Midterm Exam	**25**
Final Exam	**25**
Term Project	**10**
Lab work	**20**

8. Grading policy: As per NSU grading policy .

Numerical Scores	Letter Grade	Grade Points
93 & above	A	4.0
90 - 92	A-	3.7
87 – 89	B+	3.3
83 – 86	B	3.0
80 – 82	B-	2.7
77 – 79	C+	2.3
73- 76	C	2.0
70 – 72	C-	1.7
67 - 69	D+	1.3
60 - 66	D	1.0

http://www.northsouth.edu/academic/grading-policy.html

Make-up Policy:
No make-up testes for the missed Term Examinations and Quizzes.

Course Topics	Min. Coverage
Numerical representation of numbers Binary, octal, decimal, hexadecimal, complements, signed/unsigned numbers, binary codes, error detecting/correcting codes	4.5 hours
Boolean algebra Logic gates, Boolean algebra, Boolean functions, canonical and standard forms	3 hours
Combinational logic design Minimization techniques (Boolean algebra, Karnaugh map), don't care conditions, universal gate implementation	4.5 hours

Combinational circuits Analysis, design procedure, binary adder/subtractor, decoders, encoders, multiplexers, combinational logic implementation using decoders and multiplexers	6 hours
Synchronous sequential logic Sequential circuits, flip-flops, timing diagrams, state transition tables, state transition diagrams (Mealy and Moore models), state minimization and assignment, design implementation	6 hours
Sequential circuits: Registers and counters Synchronous/Asynchronous counters, registers, shift registers	3 hours
Memory design (RAM, ROM) Programmable logic: Implementation of logic functions using programmable logic devices ROM, PLA, PAL	6 hours

Class Structure:

1. Lectures : Attendance and participation of all of them is strongly encouraged.

2. Laboratory : You must pass in your lab to attain a passable grade in theory. 20% marks from your lab will be directly added to your theory

3. Assignments : You will be given some design assignments. You will use pen and papers and tools to solve those problems.

4. Projects : You will have to submit a hardware design project at the end of the semester. You will work on the project as a group.

5. Exams: There will be one midterm, one final exam and no make-ups.