EEE111 Course outline & Syllabus

Anagolg Electronics (North South University)

Course Objective, Outcome, & Outline
Department of Electrical and Computer Engineering
School of Engineering and Physical Sciences
North South University, Bashundhara, Dhaka-1229, Bangladesh

1. **Course Number and Title:** EEE 111/ ETE 111 Analog Electronics-I
    EEE 111L/ ETE 111L Analog Electronics-I Lab

2. **Number of Credits:**   3+1=4 credits

3. **Type:**   Core, Engineering, Lecture + Lab

4. **Prerequisites:**   EEE 141/ETE 141 Electrical Circuits-I

5. **Contact Hours:**   Lecture-3 Hours/week, Lab- 3 Hours/week

6. **Instructor:**   **Tanjila Farah (TnF)**

7. **Course Summary:**
    In this course, a variety of electronic devices used in the design of analog electronics are studied. Basic understanding of semiconductor devices is covered. Emphasis is placed on diodes, BJT, and FET. Small and large signal characteristics and models of electronic devices, analysis and design of elementary electronic circuits are also included. This course has separate mandatory laboratory sessions every week as EEE 111L.

8. **Course Objectives:**

    The objectives of this course are

    a. to possess a solid understanding of semiconductor devices used in the design of analog electronics
    b. to learn the required skill to use the electronic devices in designing practical circuits to solve practical problems.
    c. to gain the ability of conduct, analyze, and interpret experiments, and apply experimental results to improve processes or circuit systems.

9. **Course Outcomes (COs):**

Upon Successful completion of this course, students will be able to:

Sl.	CO Description	Weightage (%)
CO1	**explain** the characteristics of diode, BJT and FET	30
CO2	**analyze** simple electronic circuits using diodes and transistors.	30
CO3	**apply** simple models of BJT and FET for analysing the small signal behaviour of BJT and FET.	15
CO4	**conduct** experiments, as well as to **analyze** and **interpret** data	25

10. Mapping of CO-PO:

Sl.	CO Description	POs	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	**Explain** the characteristics of diode, BJT and FET	a	Cognitive/ Understand	Lecture	Quizzes, Exam
CO2	**Analyze** simple electronic circuits using diodes and transistors.	a	Cognitive/Analyze	Lecture	Quizzes, Exam
CO3	**Apply** simple models of BJT and FET for analyzing the small signal behavior of BJT and FET.	a	Cognitive/Apply	Lecture	Quizzes, Exam
CO4	**Conduct** experiments, as well as to **analyze** and **interpret** data	d	Psychomotor/ Precision	Lab experiments	Lab Report

11. Resources

Text books:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	Robert Boylestad, Louis Nashelsky	2016	Electronic Devices and Circuit Theory	11th	Pearson	ISBN978-93-325-4260-0

Reference books:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	Adel S. Sedra and Kenneth C. Smith	2013	Microelectronic Circuits	6th	Oxford University Press.	ISBN 13: 978-0-19-808913-1
2	Albert Malvino and David J. Bates	2016	Electronic Principles	8th	McGraw Hill	ISBN 978-0-07-337388-1

12. Weightage Distribution among Assessment Tools:

Assessment Tools	Weightage (%)
Attendance	**5%**
Quiz	**15%**
Midterm Exam (1)	**25%**
Final Exam	**35%**
Lab	**20%**
Assignment	**Non Credit**

13. Grading Policy: As per NSU grading policy available in
http://www.northsouth.edu/academic/grading-policy.html

14. Office Room & Hours:
Room: SAC 929
Office hours: to be announced

15. Contact email: tanjila.farah@northsouth.edu

16. Syllabus (Tentative):

Topics	Weeks
1. Semiconductor Diodes I. Semiconductor Materials II. Intrinsic and Extrinsic Materials III. PN Junction IV. Diode under bias V. Resistance levels and Diode equivalent circuit	**1, 2, 3, 4, & 5**
2. Diode applications I. Load line analysis II. Series and Parallel Configuration III. AND/OR gates IV. Half-wave and full-wave rectification, clippers and clampers	
3. BJT I. Transistor Construction and Operation II. Transistor amplifying action III. Configuration: CB, CE and CC	
Midterm	
4. DC Biasing of BJT I. Operating point II. Fixed Bias Circuit (Ckt) III. Emitter Bias IV. Voltage Divider Bias V. DC Bias with Voltage Feedback	**6**
5. BJT AC analysis I. BJT Modeling II. r_e modeling	**7 & 8**

III. Hybrid Equivalent Model IV. CE Fixed Bias configuration V. Voltage Divider Bias VI. CE Emitter Bias Configuration VII. Emitter Follower Configuration VIII. CB And Collector Feedback Configuration	

6. FETs
    I. Construction and Characteristics of JFET
    II. Transfer Characteristics
    III. Depletion Type MOSFET
    IV. Enhancement Type MOSFET
    V. CMOS
	9

7. FET Biasing
    I. Fixed Bias Configuration
    II. Self Bias Configuration
    III. Voltage Divider Biasing
    IV. Depletion Type MOSFETs
    V. Enhancement Type MOSFETs
	10

8. FET Amplifications
    I. Enhancement Type MOSFETs
    II. E-MOSFET Drain Feedback Configuration
    III. E-MOSFET Voltage Divider Configuration
	11 & 12

Final Exam	