NSU/Spring 2025
Department of Electrical Engineering and Computer Science
CSE 332 Computer Organization and Architecture (Sections: 7 & 8)

Instructor: Professor Dr. Md. Shafiul Alam (Sfm)
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Office Hours: Thursday & Saturday: 11:20am –1:30pm, Office: SAC-946

Course Objectives: *Introduction to Computer Organization and Architecture, Software, levels of Programming & Instruction, CPU, Primary Memory, Control Unit & Bus System, Memory Organization and Architecture, CPU Architecture Evaluation: von Neumann, Harvard Architecture, CISC & RISC, Instruction and Fetch Cycle, Performance Evaluation & Amdahl's Law, Great ideas in Computer Architecture, RISC Processor, Instruction Set & Addressing Modes, Micro-architecture & Datapath Design, Pipeline Architecture and Hazards, Superscalar Architecture and Multi-core Processors, Cache Memory and Mapping, ALU, Floating Point Numbers and Floating Point ALU Design, CISC processor & Microprogrammed Control Unit*

Textbooks:

1. Computer Organization and Architecture by William Stallings, Pearson Publisher: 10 edition, January 22, 2015.
2. Computer Organization and Design MIPS Edition, Fifth Edition: The Hardware/Software Interface, by David A. Patterson and John L. Hennessy, Publisher: Morgan Kaufmann; 5 edition

Outline of the course

Lecture #1	Introduction to Computer Organization and Architecture, levels of Programming & Instruction	
Lecture #2	CPU Architecture: von Neumann, Harvard Architecture,	
Lecture #3	Primary Memory, Control Unit & Bus System, Memory Organization and Architecture	Quiz-1
Lecture #4	Fetch and Execution Cycle	
Lecture #5	Instruction Set Architecture, CISC & RISC	
Lecture #6	Performance Evaluation	Quiz-2
Lecture #7	Amdahl's Law	
Lecture #8	Great ideas in Computer Architecture	
Mid Term Test #1		
Lecture #9	RISC Processor Architecture and CISC Processor	
Lecture #10	Instruction Set & Addressing Modes of RISC Processors	
Lecture #11	Micro-architecture & Datapath Design	Quiz-3
Lecture #12	Micro-architecture & Datapath Design	
Lecture #13	Pipeline Architecture	
Lecture #14	Pipeline Hazards	
Lecture #15	Superscalar Architecture and Multi-core Processors	Quiz-4
Lecture #16	DRAM Organization, Advanced DRAM Organization, Error Correction, Problem solving	
	Mid Term Test #2	
Lecture #17	Memory Hierarchy	
Lecture #18	Cache Memory and Multi-level Cache	Quiz-5
Lecture #19	Cache Mapping Techniques	
Lecture #20	ALU Design: Fast Adders, Multipliers and Divisors	
Lecture #21	Floating Point Numbers and Floating Point ALU Design	Quiz-6
Lecture #22	CISC processor & Microprogrammed Control Unit	
Lecture #23	Microprogrammed Control Unit	
Lecture #24	Review	
Term Final		

Tests and Evaluation:

Attendance: 5%	MT-2: 15%
Assignment: 10% (average)	Lab : 10%
Quiz: 15% (Best 3 counted out of 6)	Term Final: 30%
MT-1: 15%	

Grading: NSU Standard