FIB UPC
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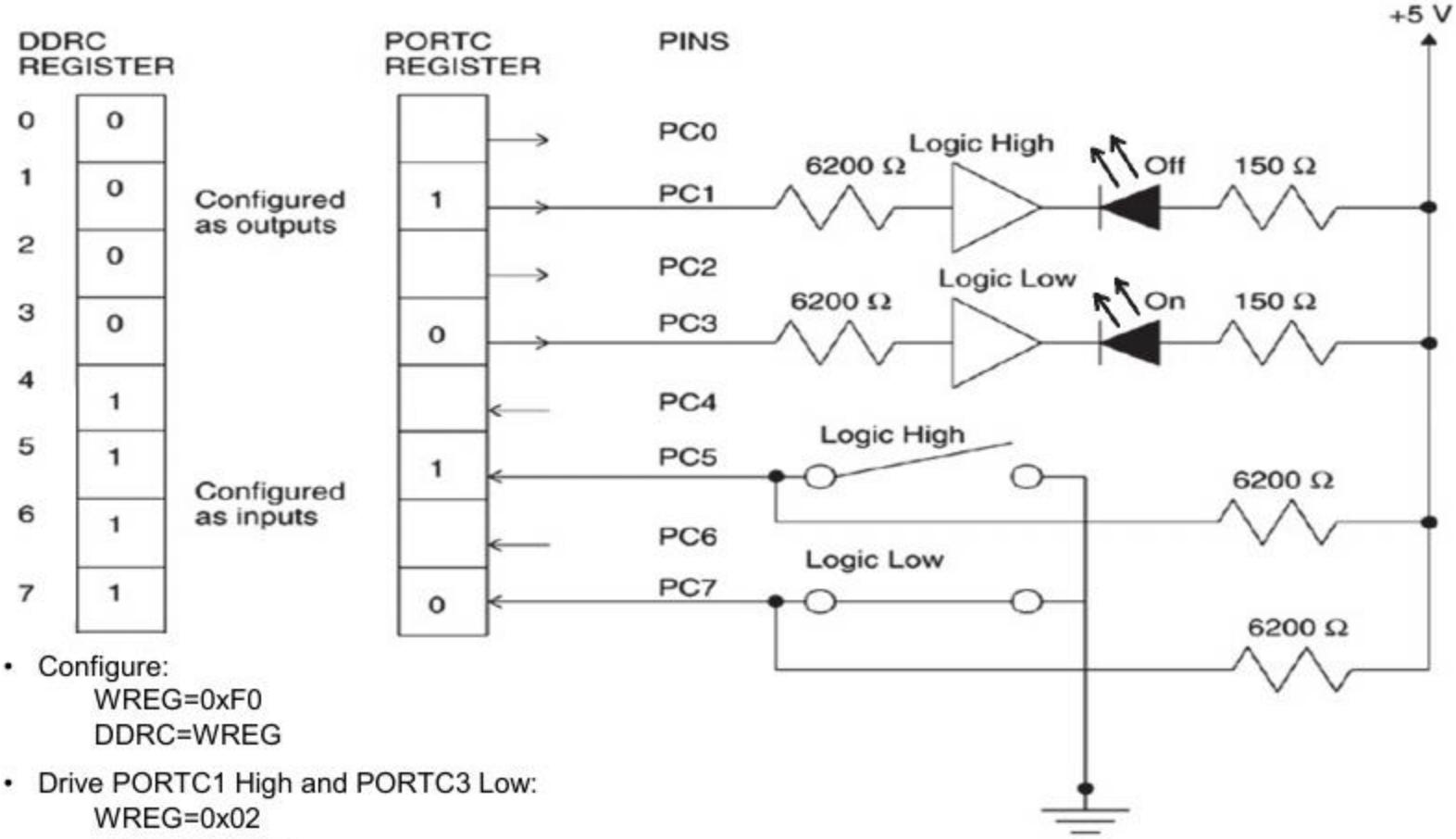
I/O Ports

Dpt. Enginyeria de Sistemes, Automàtica i Informàtica Industrial

Need of I/O ports

- Several applications require interfacing an MCU with Light Emitting Diodes, Switches, Liquid Crystal Display, Seven Segment Displays.
- I/O ports therefore have to be programmed to handle input/output signals.

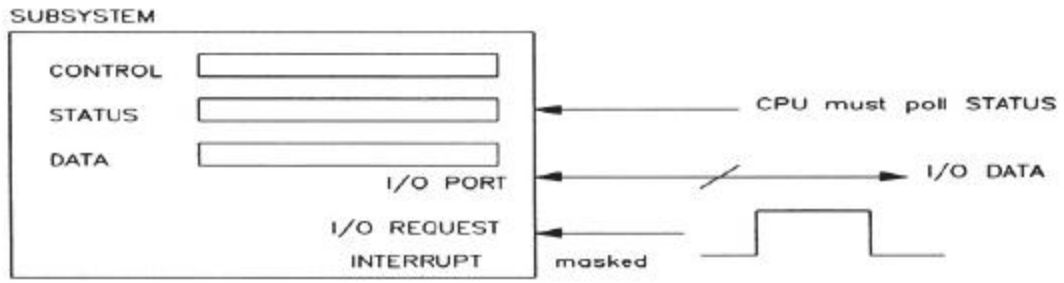


- Configure:
  WREG=0xF0
  DDRC=WREG
- Drive PORTC1 High and PORTC3 Low:
  WREG=0x02
  PORTC=WREG
- Read Inputs (use High Nibble only)
  WREG=PORTC

I/O Port Structure

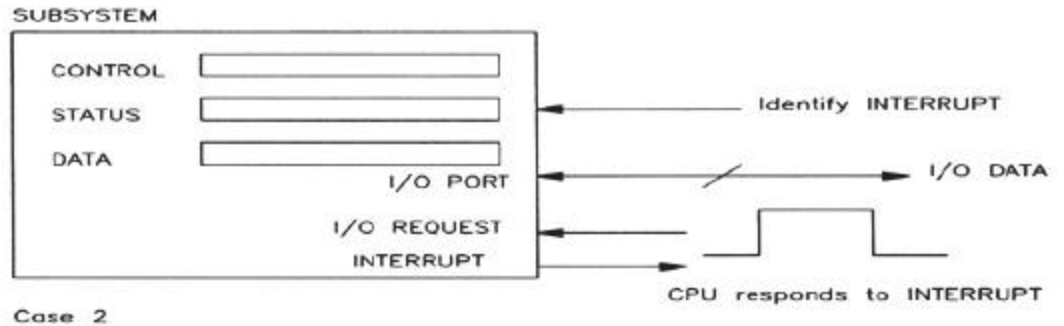
1. Data Register: for data in transit
2. Control Register: Hold commands from processor to port
3. Status Register: Used to monitor I/O activity

Principal functionality is to serve as way station for data in transit between the computer and external world.



Case 1
Polled I/O, no interrupt
CPU must check a status bit to determine whether an I/O request occurred.

Polling

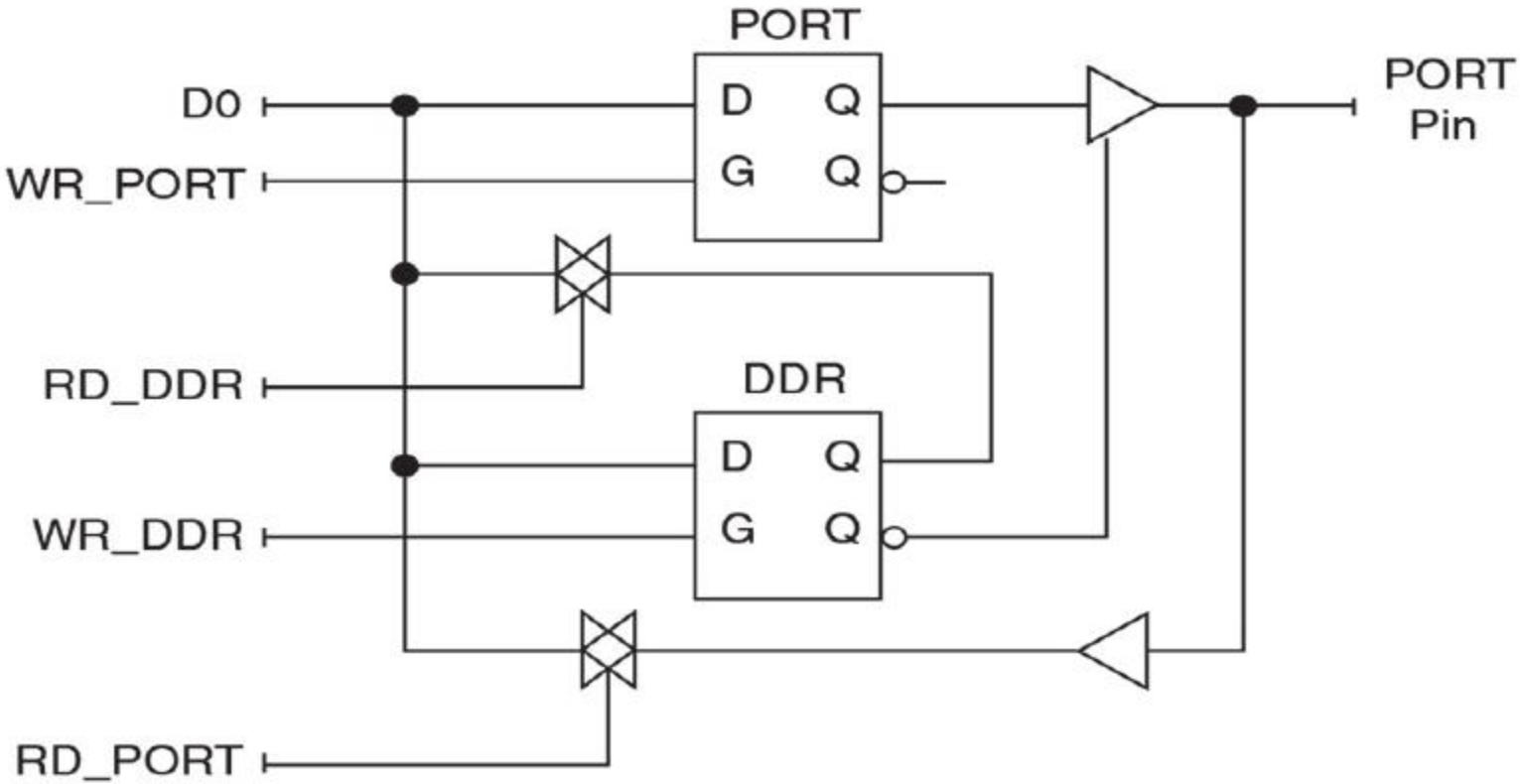


Case 2
Interrupt-driven I/O
I/O request causes interrupt and CPU responds to interrupt.

Interrupt Driven

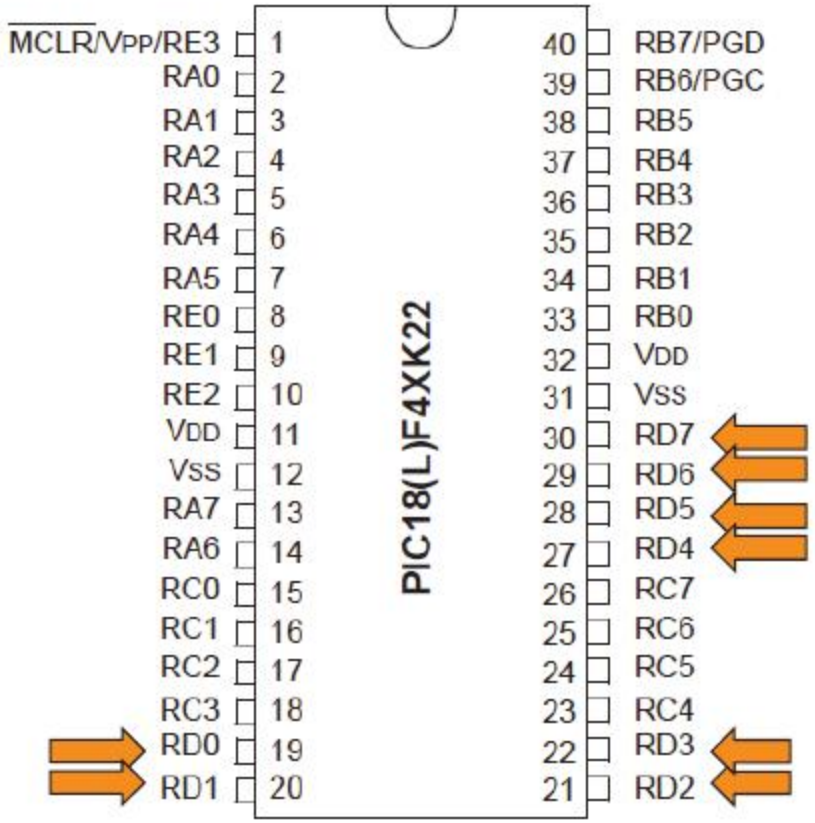
General Purpose I/O: Bidirectional

- Most GPIO pins on the MCU can be programmed for use in either direction.
- Two registers: the data register PORT and data direction register DDR.
  - The DDR determines the direction of the port pin.
    - if the DDR = 0 then the port is an output and
    - if the DDR = 1 the data register output is disabled and the port pin is placed in high impedance state.



Overview of the PIC18 Parallel I/O Ports

- I/O pins are often grouped into **ports**.
- A port consists of up to 8 pins, a data direction register (**TRISx**), a latch register (**LATx**) , and a data register (**PORTx**); where x=A,B,C,D,…etc.
- Data to be output is written into the latch, which in turn drives the output pins.
- An I/O port is often **multiplexed** with one or more peripheral functions.
- When a peripheral function is enabled, the I/O pins cannot be used for general purpose I/O.
- A PIC18 may have as many as 10 I/O ports.



Example: PORTD pins D{0..7}

Overview of the PIC18 Parallel I/O Ports

Table 3 (reference manual, page 7) fully describes the functionality of all device pins.

TABLE 3: PIC18(L)F4XK22 PIN SUMMARY

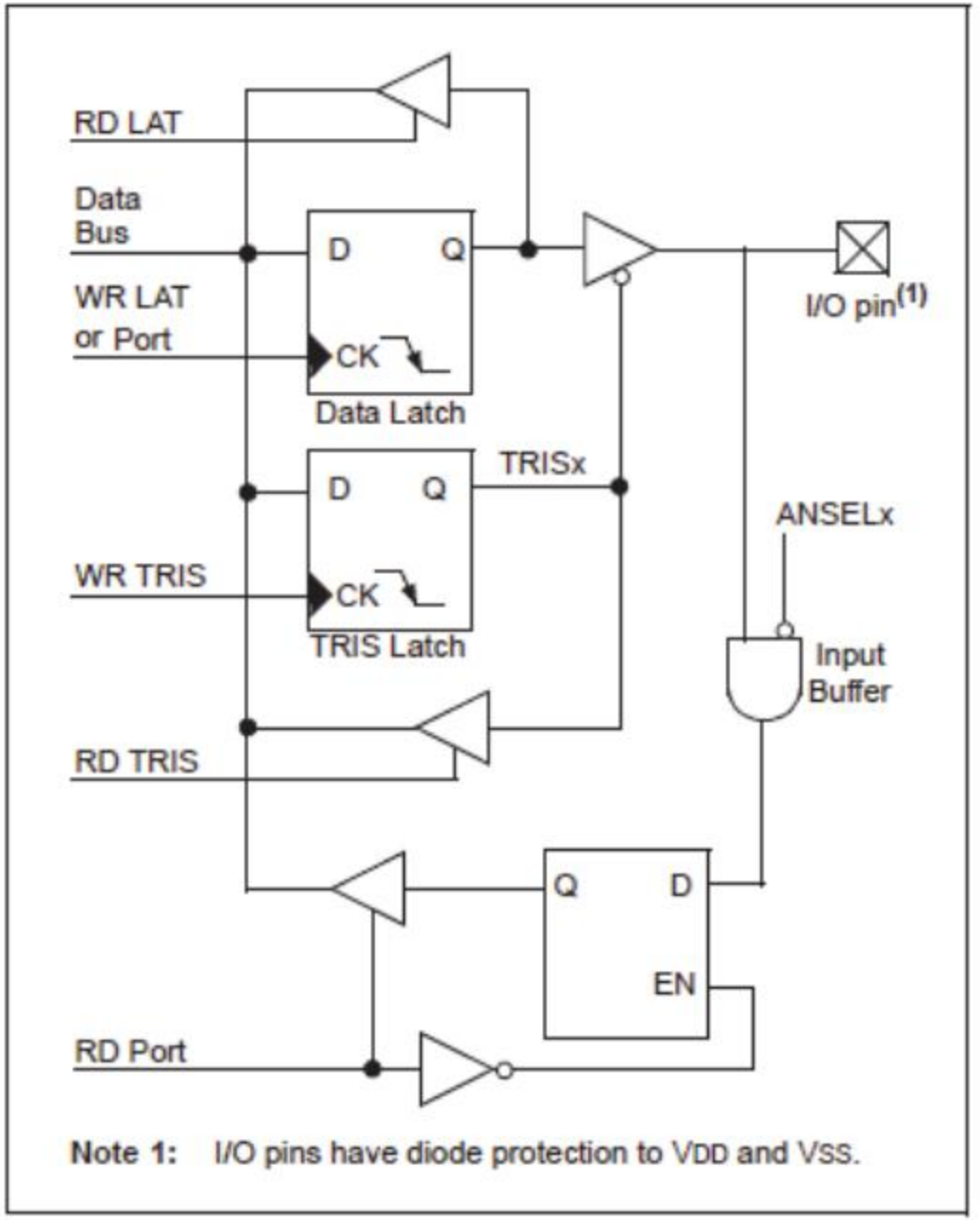
40-PDIP	40-UQFN	44-TQFP	44-QFN	I/O	Analog	Comparator	CTMU	SR Latch	Reference	(E)CCP	EUSART	MSSP	Timers	Interrupts	Pull-up	Basic
2	17	19	19	RA0	AN0	C12IN0-										
3	18	20	20	RA1	AN1	C12IN1-										
4	19	21	21	RA2	AN2	C2IN+			VREF- DACOUT							
5	20	22	22	RA3	AN3	C1IN+			VREF+							
6	21	23	23	RA4		C1OUT		SRQ					T0CKI			
7	22	24	24	RA5	AN4	C2OUT		SRNQ	HLVDIN			$\overline{SS}$1				
14	29	31	33	RA6												OSC2 CLKO
13	28	30	32	RA7												OSC1 CLKI
33	8	8	9	RB0	AN12			SRI		FLT0				INT0	Y	
34	9	9	10	RB1	AN10	C12IN3-								INT1	Y	
35	10	10	11	RB2	AN8		CTED1							INT2	Y	
36	11	11	12	RB3	AN9	C12IN2-	CTED2			CCP2 P2A(1)					Y	
37	12	14	14	RB4	AN11								T5G	IOC	Y	
38	13	15	15	RB5	AN13					CCP3 P3A(3)			T1G T3CKI(2)	IOC	Y	
39	14	16	16	RB6										IOC	Y	PGC
40	15	17	17	RB7										IOC	Y	PGD
15	30	32	34	RC0						P2B(4)			SOSCO T1CKI T3CKI(2) T3G			
16	31	35	35	RC1						CCP2(1) P2A			SOSCI			

. . . . . .

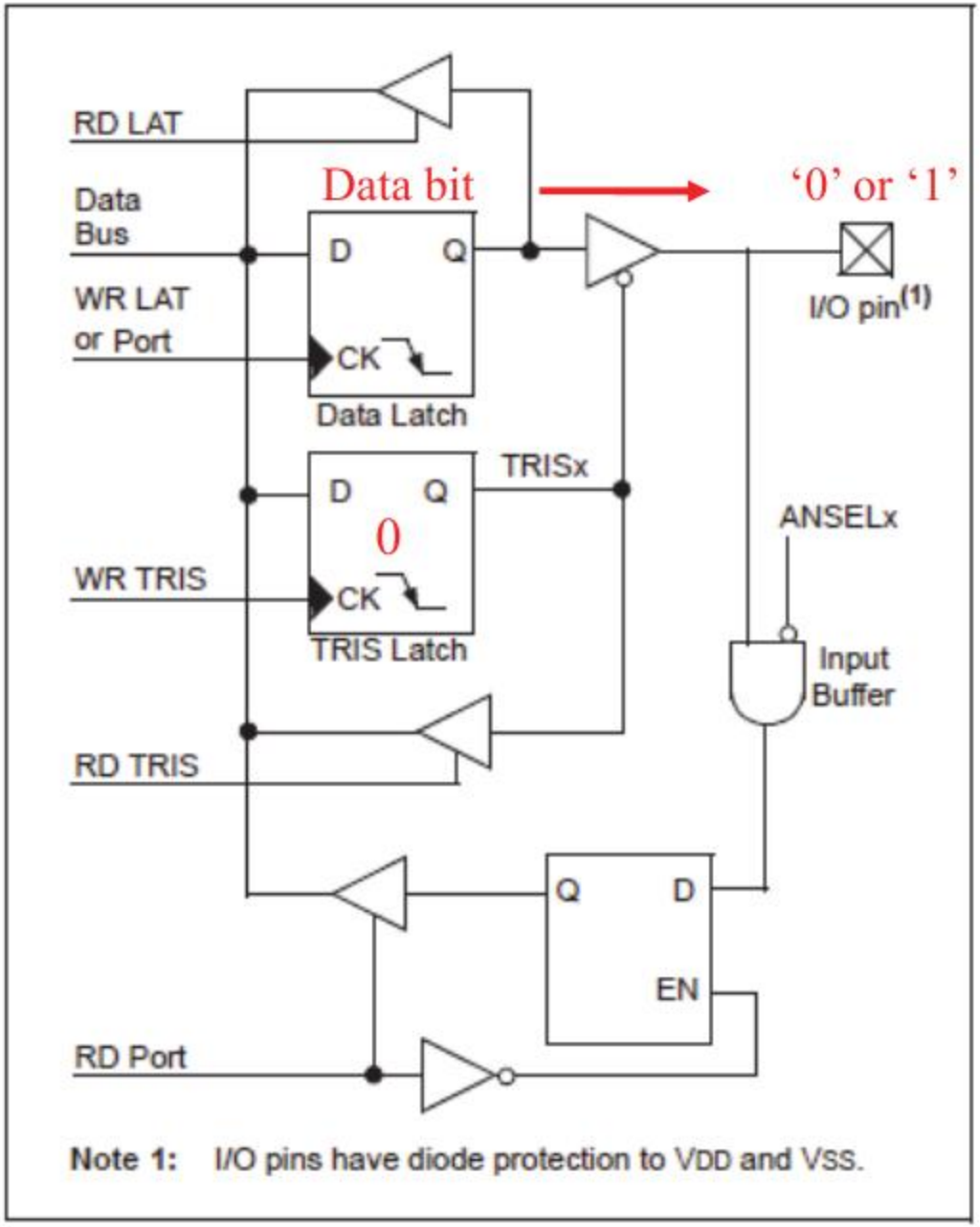
PIC18 I/O port operation

- **TRISx register (data direction register. 1 Input, 0 Output)**
- **PORTx register (reads the levels on the pins of the device)**
- **LATx register (output latch)**
- **ANSELx register (analog input control.** 0 Digital / 1 Analog**)**

x = {A, B, C, D, E}

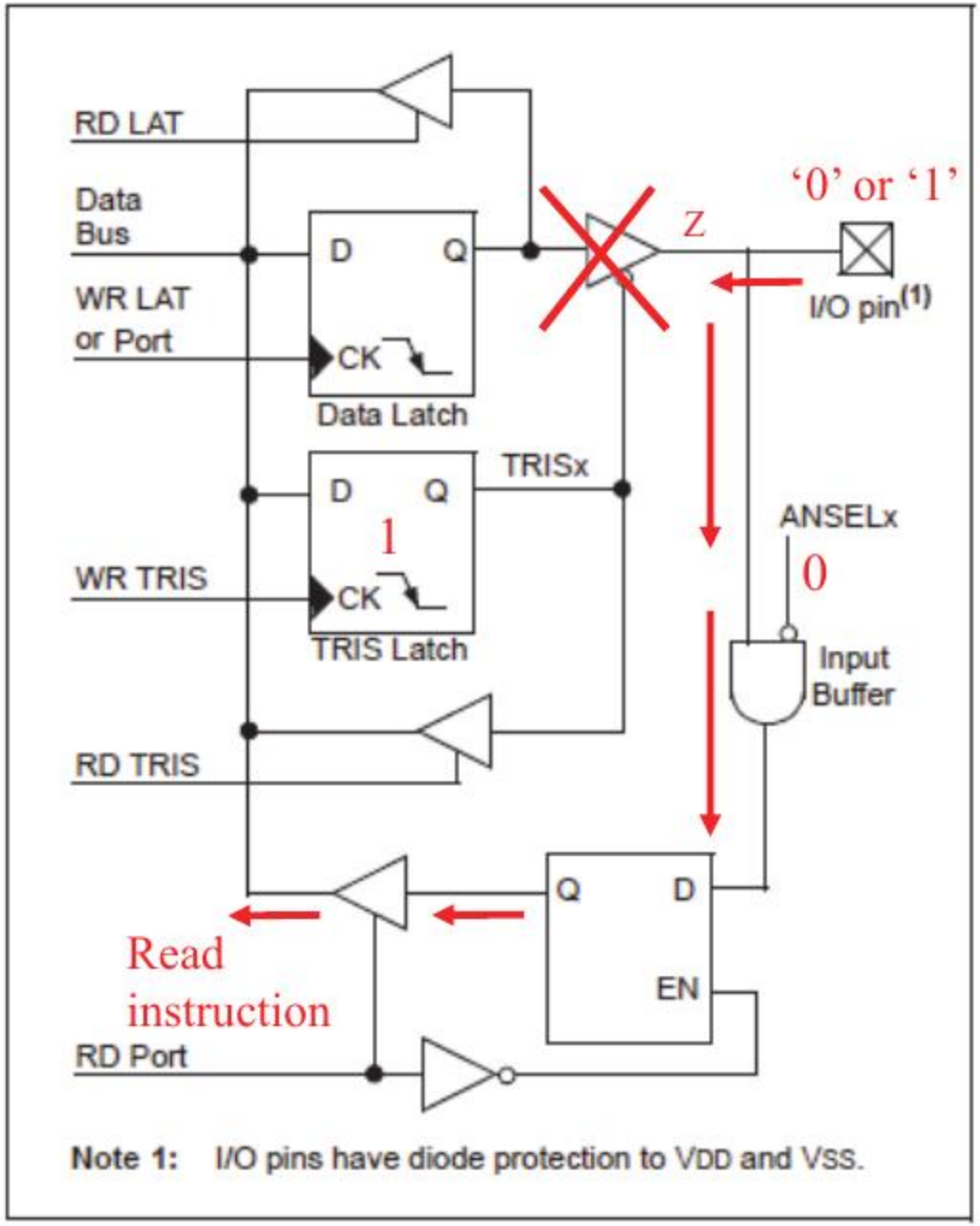


PIC18 I/O port operation



Output

PIC18 I/O port operation



Input

PORTA

- **PORTA is an 8-bit wide, bidirectional port.**
- **Pins RA6 and RA7 are multiplexed with the main oscillator pins.**
- **The operation of pins RA<3:0> and RA5 as analog is selected by setting the ANSELA<5, 3:0> bits in the ANSELA register which is the default setting after a Power-on Reset.**

Note: **On a Power-on Reset, RA5 and RA<3:0> are configured as analog inputs and read as '0'. RA4 is configured as a digital input.**

PORTA

There is a table (e.g. PORTA pag. 128) showing all the possible functions and the required configuration settings for every pin.

TABLE 10-1: PORTA I/O SUMMARY

Pin Name	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RA0/C12IN0-/AN0	RA0	0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	0	I	TTL	PORTA<0> data input; disabled when analog input enabled.
	C12IN0-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN0	1	1	I	AN	Analog input 0.
RA1/C12IN1-/AN1	RA1	0	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	0	I	TTL	PORTA<1> data input; disabled when analog input enabled.
	C12IN1-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN1	1	1	I	AN	Analog input 1.
RA2/C2IN+/AN2/ DACOUT/VREF-	RA2	0	0	O	DIG	LATA<2> data output; not affected by analog input; disabled when DACOUT enabled.
		1	0	I	TTL	PORTA<2> data input; disabled when analog input enabled; disabled when DACOUT enabled.
	C2IN+	1	1	I	AN	Comparator C2 non-inverting input.
	AN2	1	1	I	AN	Analog output 2.
	DACOUT	x	1	O	AN	DAC Reference output.
	VREF-	1	1	I	AN	A/D reference voltage (low) input.
RA3/C1IN+/AN3/ VREF+	RA3	0		O	DIG	LATA<3> data output; not affected by analog input.
		1	0	I	TTL	PORTA<3> data input; disabled when analog input enabled.
	C1IN+	1	1	I	AN	Comparator C1 non-inverting input.
	AN3	1	1	I	AN	Analog input 3.
	VREF+	1	1	I	AN	A/D reference voltage (high) input.

PORTA

There is a table (e.g. PORTA pag. 128) showing all the possible functions and the required configuration settings for every pin.

RA4/CCP5/C1OUT/ SRQ/T0CKI	RA4	0	—	O	DIG	LATA<4> data output.
		1	—	I	ST	PORTA<4> data input; default configuration on POR.
	CCP5	0	—	O	DIG	CCP5 Compare output/PWM output, takes priority over RA4 output.
		1	—	I	ST	Capture 5 input/Compare 5 output/ PWM 5 output.
	C1OUT	0	—	O	DIG	Comparator C1 output.
	SRQ	0	—	O	DIG	SR latch Q output; take priority over CCP 5 output.
	T0CKI	1	—	I	ST	Timer0 external clock input.
RA5/C2OUT/SRNQ/ $\overline{SS1}$/ HLVDIN/AN4	RA5	0	0	O	DIG	LATA<5> data output; not affected by analog input.
		1	0	I	TTL	PORTA<5> data input; disabled when analog input enabled.
	C2OUT	0	0	O	DIG	Comparator C2 output.
	SRNQ	0	0	O	DIG	SR latch $\overline{Q}$ output.
	$\overline{SS1}$	1	0	I	TTL	SPI slave select input (MSSP1).
	HLVDIN	1	1	I	AN	High/Low-Voltage Detect input.
	AN4	1	1	I	AN	A/D input 4.
RA6/CLKO/OSC2	RA6	0	—	O	DIG	LATA<6> data output; enabled in INTOSC modes when CLKO is not enabled.
		1	—	I	TTL	PORTA<6> data input; enabled in INTOSC modes when CLKO is not enabled.
	CLKO	x	—	O	DIG	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
	OSC2	x	—	O	XTAL	Oscillator crystal output; connects to crystal or resonator in Crystal Oscillator mode.
RA7/CLKI/OSC1	RA7	0	—	O	DIG	LATA<7> data output; disabled in external oscillator modes.
		1	—	I	TTL	PORTA<7> data input; disabled in external oscillator modes.
	CLKI	x	—	I	AN	External clock source input; always associated with pin function OSC1.
	OSC1	x	—	I	XTAL	Oscillator crystal input or external clock source input ST buffer when configured in RC mode; CMOS otherwise.

TABLE 10-2: REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0	149
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH<1:0>		308
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH<1:0>		308
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	152
VREFCON1	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	335
VREFCON2	—	—	—	DACR<4:0>					336
HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL<3:0>				337
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	148
SLRCON	—	—	—	SLRE	SLRD	SLRC	SLRB	SLRA	153
SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	329
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				253
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS<2:0>			154
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	151

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTA.

TABLE 10-3: CONFIGURATION REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG1H	IESO	FCMEN	PRICLKEN	PLLCFG	FOSC<3:0>				345

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTA.

Example: Initializing PORTA

```
MOVLB 0xF           ; Set BSR for banked SFRs
CLRF PORTA,1        ; Initialize PORTA by
                    ; clearing output
                    ; data latches
CLRF LATA,1         ; Alternate method
                    ; to clear output
                    ; data latches
MOVLW C0h           ; Configure I/O
MOVWF ANSELA,1      ; for digital inputs
MOVLW 0CFh          ; Value used to
                    ; initialize data
                    ; direction
MOVWF TRISA,1       ; Set RA<3:0> as inputs
                    ; RA<5:4> as outputs. A6 and A7 are OSC!!
```

Example: C programming

```
#include <p18f45k22.h>
#include "config.h"

void main()
{
    ANSELA = 0xC0;     //A5-A0:DIGITAL, Pin A6 and A7? OSC or IO
    ANSELB = 0x00;     // B DIGITAL
    TRISA = 0xFF;      // PORTA INPUT
    TRISB = 0x00;      // PORTB OUTPUT
    PORTB = 0x00;

    while (1) {
        PORTB = PORTA;
    };
}
```

PORTB

- **PORTB is an 8-bit wide, bidirectional port.**
- **All pins may be used as Digital or Analog Pins**
- **The pins RB<2:0> may be used for external interrupts (Int0, Int1 and Int2).**
- **Four of the PORTB pins (RB<7:4>) are individually configurable as interrupt-on-change pins**

Note: **On a Power-on Reset, RB<5:0> are configured as analog inputs by default and read as '0'; RB<7:6> are configured as digital inputs.**

When the PBADEN Configuration bit is set to '0', RB<5:0> will alternatively be configured as digital inputs on POR.

PORTC

- **PORTC is an 8-bit wide, bidirectional port.**
- **RC2..RC7 may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**

PORTD

- **PORTD is an 8-bit wide, bidirectional port.**
- **All the pins may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**

PORTE

- **PORTE is a 4-bit wide, bidirectional port.**
- **RE0..RE2 may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**
- **RE3 = MASTER CLEAR. On a Power-on Reset, RE3 is enabled as a digital input only if Master Clear functionality is disabled.**

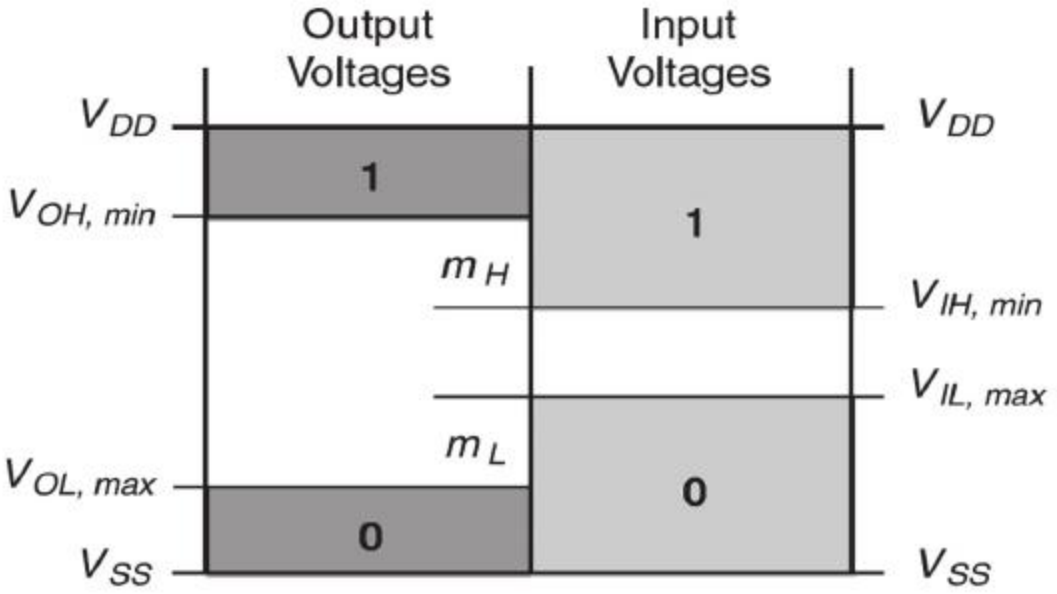
Interfacing: Voltage Parameters

- **Like any digital device, before we can connect something to an input or output, we need to know the specification for the interface parameter.**
- **The first parameter to consider are the input and output voltage levels and corresponding noise margins.**

VDD and VSS are supply voltages. The output voltage parameters are V_{OL} and V_{OH}.

The input voltage parameters are V_{IL} and V_{IH}.

For a digital system to work correctly, the output high voltage always must be between $V_{IH,min}$ and VDD.



Noise Margin?

Interfacing: Current Parameters

- **The interface current parameters are the output currents, I_{OH} and I_{OL}, and the input leakage current I_{IN}.**
  1. **I_{OH} is the current *flowing out* of a *high output* (sourced)**
  2. **I_{OL} is the current *flowing in* to a *low output* (sunk)**
  3. **I_{IN} is the leakage current that flows into or out of an input pin.**

- **These currents are used to determine the *static fanout of a device*, that is, the number of inputs that can be connected to one output while preserving the required voltage margins.**
  1. **Static fanout for a low output is: $n_L = | I_{OL,max} | / | I_{In} |$**
  2. **Static fanout for a high output is: $n_H = | I_{OH,max} | / | I_{In} |$**
  3. **$n = \min [n_H, n_L]$**

Absolute maximum ratings

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD}, and $\overline{MCLR}$)	-0.3V to (V_{DD} + 0.3V)
Total power dissipation **(Note 1)**	1.0W
Maximum current out of V_{SS} pin (-40°C to +85°C)	300 mA
Maximum current out of V_{SS} pin (+85°C to +125°C)	125 mA
Maximum current into V_{DD} pin (-40°C to +85°C)	200 mA
Maximum current into V_{DD} pin (+85°C to +125°C)	85 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports (-40°C to +85°C)	200 mA
Maximum current sunk by all ports (+85°C to +125°C)	110 mA
Maximum current sourced by all ports (-40°C to +85°C)	185 mA
Maximum current sourced by all ports (+85°C to +125°C)	70 mA

Maximum I_{OH} or **I_{OL}** for the PIC18F45K22 is +/- 25mA.

This Maximum ratings give the value that if exceeded may destroy the part.

DC Characteristics. Supply Voltage

27.1 DC Characteristics: Supply Voltage, PIC18(L)F2X/4XK22

PIC18(L)F2X/4XK22				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	PIC18LF2X/4XK22	1.8	—	3.6	V	
			PIC18F2X/4XK22	2.3	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage**(1)		1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal		—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal		0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	**Brown-out Reset Voltage**						
		BORV<1:0> = 11(2)		1.75	1.9	2.05	V	
		BORV<1:0> = 10		2.05	2.2	2.35	V	
		BORV<1:0> = 01		2.35	2.5	2.65	V	
		BORV<1:0> = 00(3)		2.65	2.85	3.05	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: On PIC18(L)F2X/4XK22 devices with BOR enabled, operation is supported until a BOR occurs. This is valid although VDD may be below the minimum rated supply voltage.

3: With BOR enabled, full-speed operation (FOSC = 64 MHz or 48 MHz) is supported until a BOR occurs. This is valid although VDD may be below the minimum voltage for this frequency.

Input characteristics

27.8 DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	VIL	**Input Low Voltage**					
		I/O PORT:					
D140		with TTL buffer	—	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D140A			—	—	0.15 VDD	V	1.8V ≤ VDD ≤ 4.5V
D141		with Schmitt Trigger buffer	—	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		with I²C levels	—	—	0.3 VDD	V	
		with SMBus levels	—	—	0.8	V	2.7V ≤ VDD ≤ 5.5V
D142		MCLR, OSC1 (RC mode)(1)	—	—	0.2 VDD	V	
D142A		OSC1 (HS mode)	—	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—	—		
D147		with TTL buffer	2.0	—	—	V	4.5V ≤ VDD ≤ 5.5V
D147A			0.25 VDD + 0.8	—	—	V	1.8V ≤ VDD ≤ 4.5V
D148		with Schmitt Trigger buffer	0.8 VDD	—	—	V	2.0V ≤ VDD ≤ 5.5V
		with I²C levels	0.7 VDD	—	—	V	
		with SMBus levels	2.1	—	—	V	2.7V ≤ VDD ≤ 5.5V
D149		MCLR	0.8 VDD	—	—	V	
D150A		OSC1 (HS mode)	0.7 VDD	—	—	V	
D150B		OSC1 (RC mode)(1)	0.9 VDD	—	—	V	
	IIL	**Input Leakage I/O and MCLR**(2),(3)					VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D155		I/O ports and MCLR	— — — —	0.1 0.7 4 35	50 100 200 1000	nA nA nA nA	≤ +25°C(4) +60°C +85°C +125°C

Interpretation:
if the power supply (VDD) is between 4,5V and 5,5V then $V_{IL\,MAX} = 0{,}8V$

$V_{IL\,MAX} = 0{,}8V$ (voltage input low maximum) means that any voltage under 0,8V put on an input pin will always be read as a logical '0'

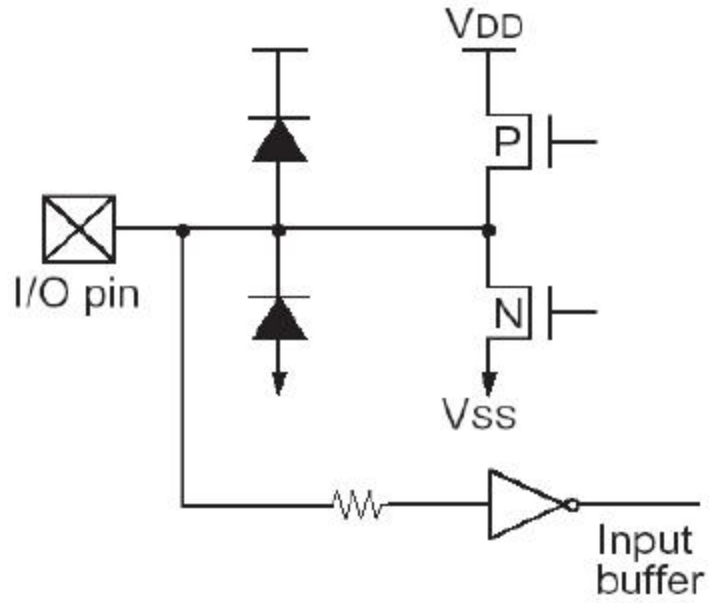
Output characteristics

27.8 DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22 (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D159	VOL	**Output Low Voltage** I/O ports	—	—	0.6	V	IOL = 8 mA, VDD = 5V IOL = 6 mA, VDD = 3.3V IOL = 1.8 mA, VDD = 1.8V
D161	VOH	**Output High Voltage**(3) I/O ports	VDD - 0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V

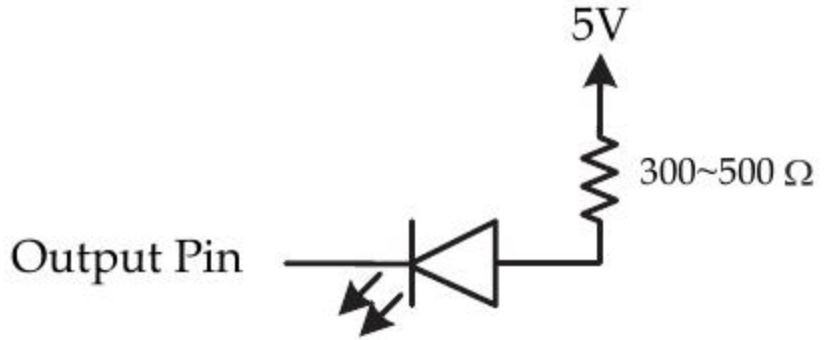
$V_{OL\,MAX}$ = 0,6V (voltage output low maximum) means that even in the worst conditions, a logical '0' will always be output as a voltage less than 0,6V

Protection diodes

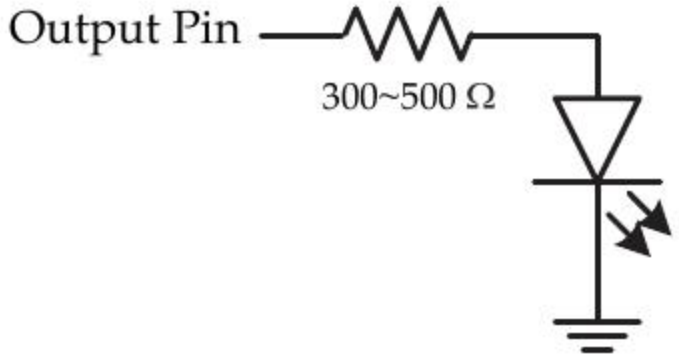


Simplified structure of an I/O pin.

Interfacing with LEDs



(a) low voltage on output pin lights LED



(b) high voltage on output pin lights LED

A LED emits light when current flows through it in the positive direction i.e. when the voltage on the anode side is made higher than the voltage on the cathode side.

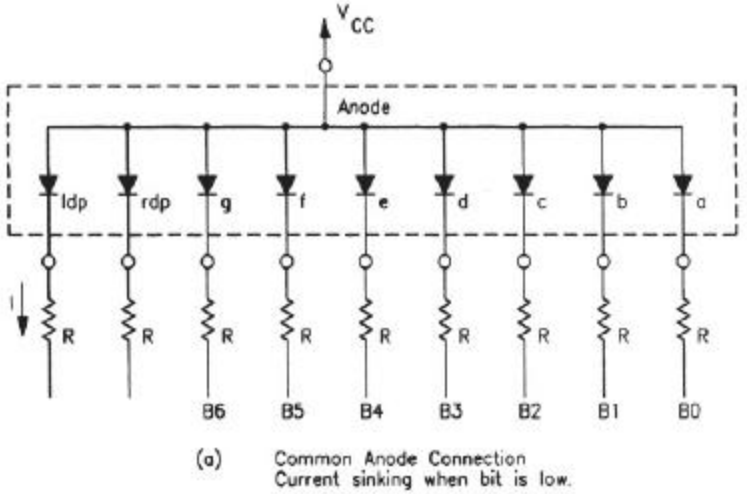
The forward voltage across the LED is typically about 1.5 to 2 Volts.
We need to add a resistor to limit the current.

Connecting a LED to an Output Port

- Using a 5-volt supply and assuming that the LED has a 2.0 V drop across it, what resistor value will limit the current to 10mA?
- Answer:
  - $5V = 2.0V + I_{Rx} \times Rx$
  - Setting I_{Rx} to 10mA the resistor Rx is solved to be 300 Ohm.

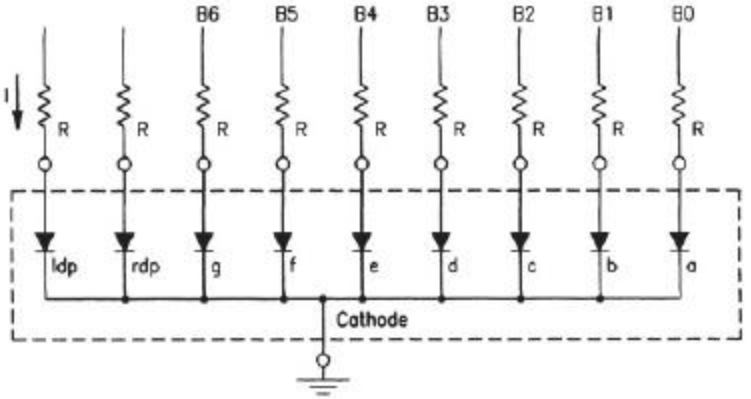
Seven Segment Displays

- Common Anode:
  1. All anodes are tied in common.
  2. Segment will be lit whenever a low voltage is applied.

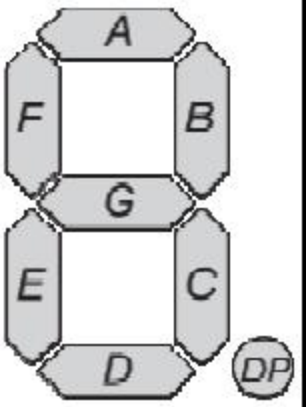


(a) Common Anode Connection
Current sinking when bit is low.

- Common Cathode:
  1. all cathodes are tied in common.
  2. Segment will be lit whenever a high voltage is applied.



(b) Common Cathode Connection
Current sourcing when bit is high.



- Current limiting resistors must be included or else you might damage display.

Seven Segment Displays: Examples

- **Depending on the type of display used a different hex code is generated by the MCU.**

1.Common Anode: sending a "0" will illuminate the segment.

B7	B6	B5	B4	B3	B2	B1	B0
x	0	0	1	1	0	0	1
	g	f	e	d	c	b	a

0 = segment illuminated
1 = segment off

Hex Code = $19

(a) Common Anode Example

2.Common Cathode: sending a "1" will illuminate the segment.

B7	B6	B5	B4	B3	B2	B1	B0
x	1	0	0	1	1	1	1
	g	f	e	d	c	b	a

1 = segment illuminated
0 = segment off

Hex Code = $4F

(b) Common Cathode Example

Interfacing with DIP Switches

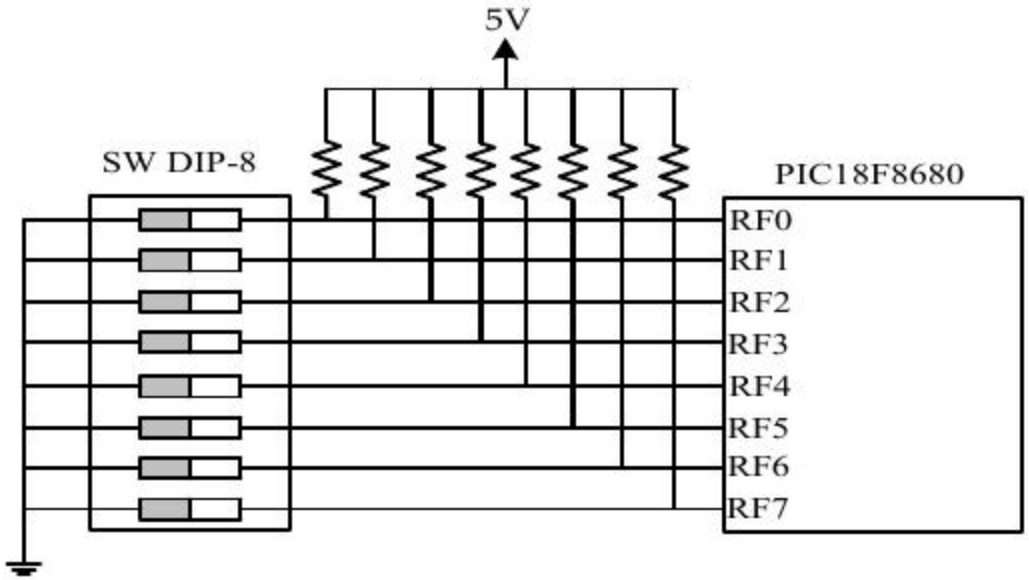


Figure 7.24b Connecting a set of eight DIP switches to port F of the PIC18F8680

Reading a byte from the DIP switches to WREG

```
movlw   0xFF     ; configure port F for input
movwf   TRISF    ;          "
movf    PORTF,W          ; read portF
```

Interfacing with Keypad

Types of Key Switches

1. Membrane: A plastic or rubber membrane presses one conductor onto another.
2. Capacitive: Two parallel plates. Pressing the plates changes the distance between the plates and changes the capacitance.
3. Hall effect: The motion of the magnetic flux lines of a permanent magnet perpendicular to a crystal is detected as voltage appearing between the two faces of the crystal.
4. Mechanical: Two metal contacts are brought together to complete an electrical circuit.

Mechanical Keypads and Keyboard

- **Low cost and strength of construction**
- **Most popular**
- **Pressing the key switch generates a series of pulses instead of a single clean output**
- **Human being cannot press and release the key switch 20 ms**
- **A debouncing process is required for correct operation**

Keypad Input Program

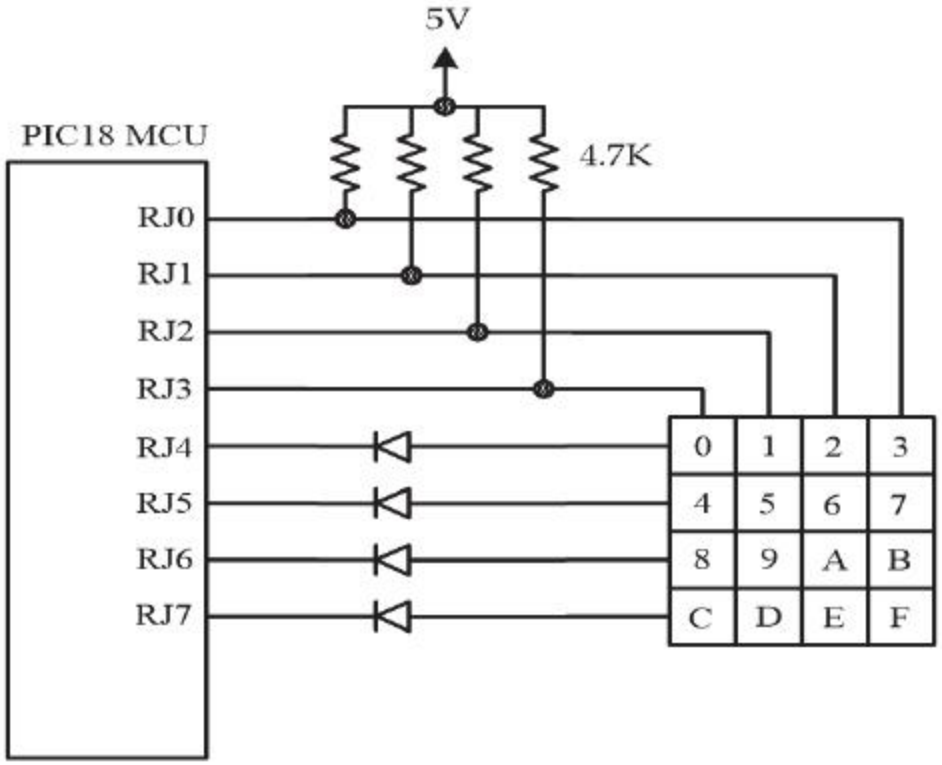


Figure 7.26b Sixteen-key keypad connected to PIC18 (used in all SSE demo boards)

Keypad Input Program **Consists of Three Parts**

1. **Keypad scanning**
2. **Key switch debouncing**
3. **Table lookup**

Keypad Scanning

- **Performed to detect which key is being pressed**
- **Performed row by row or column by column**
- **The rows and columns of a keypad are simply conductors**

Example of "row-by-row" scan:

- **The row to be scanned is pulled to low. Other rows are pulled high.**
- **When a key is pressed, the corresponding row and column are shorted together and is detected low.**
- **The diodes in Figure 7.26b provide protection of accidental simultaneous press of multiple keys.**

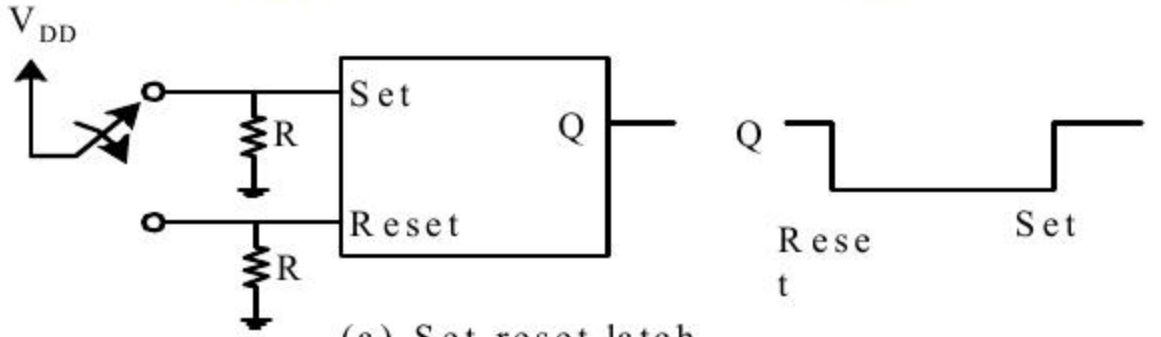
Keypad Debouncing

- **When a key is pressed, the voltage of the key switch falls and rises a few times within a period of about 5 ms as a contact bounces.**
- **A debouncer will recognize that the switch is closed after the voltage is low for about 10 ms and will recognize that the switch is open after the voltage is high for about 10 ms.**
- **Both hardware and software debouncing solutions are available.**
- **The simplest and most popular software solution is** wait-and-see. **The program simply waits for 10 ms after detecting a key switch is closed and re-examines the same key.**
- **Three hardware debouncing techniques are shown in Figure 7.27.**

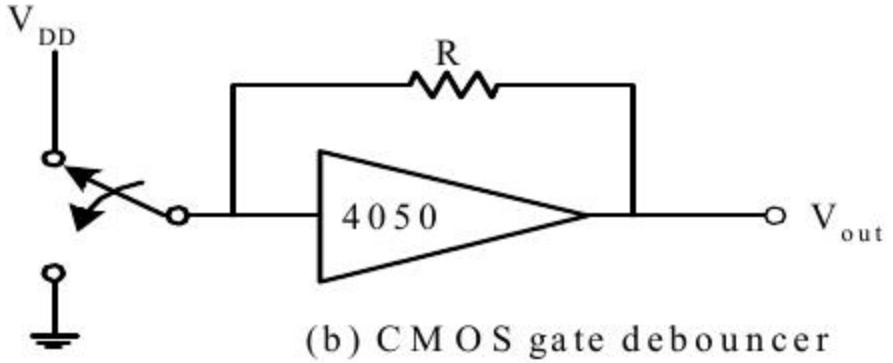
ASCII Code Lookup

- **The keypad input subroutine returns the ASCII code to the caller.**
- **This step can be embedded in the debouncing procedure.**

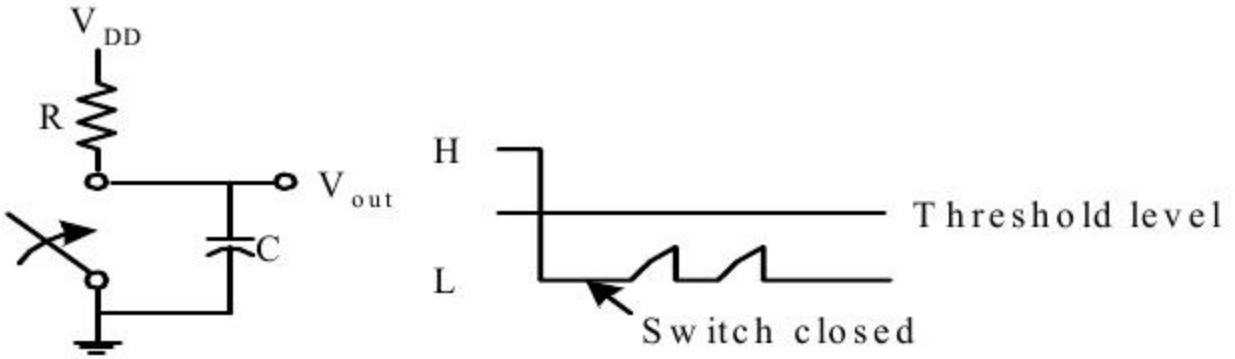
Keypad Debouncing



(a) Set-reset latch



(b) CMOS gate debouncer



(c) Integrating RC circuit debouncer

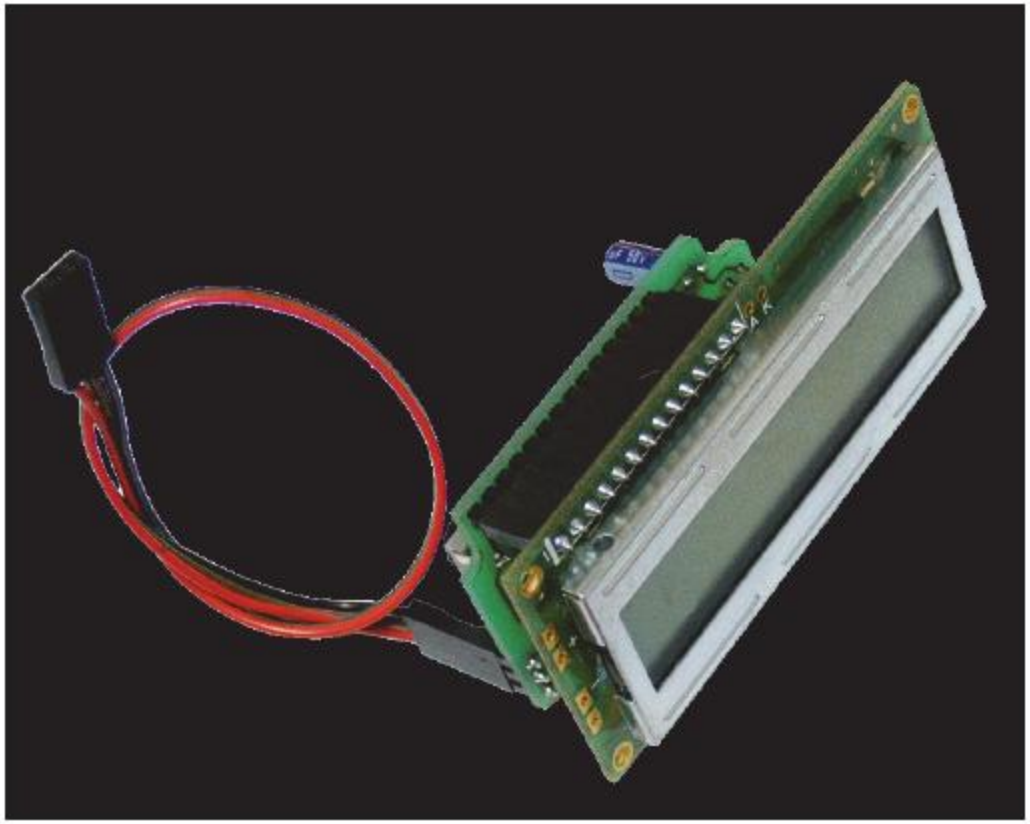
Figure 7.27 Hardware debouncing techniques

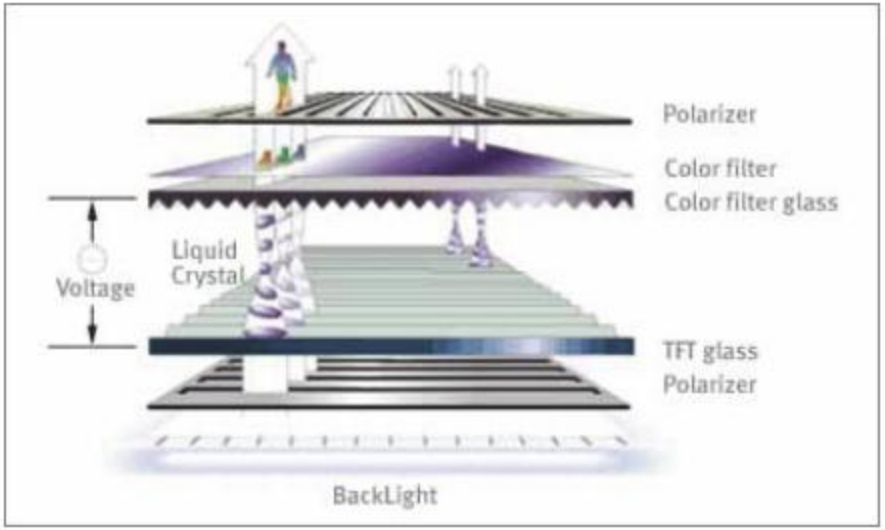
Keypad debouncing

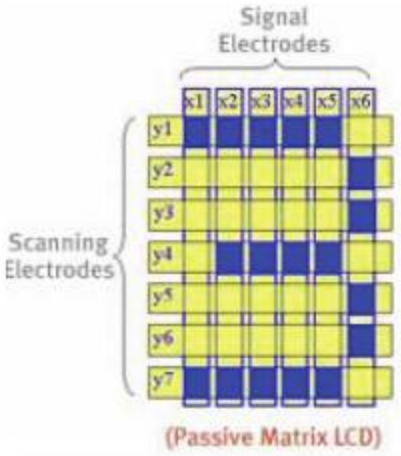
"row-by-row" scanning

```
#include     <p18F8680.h>
#define  keypad_dir  TRISJ
#define  keypad      PORTJ
void wait_10ms(void);
…
unsigned char get_key (void)
{
 keypad_dir = 0x0F;        /* configure RJ7..RJ4 for output, RJ3..RJ0 for input */
 keypad |= 0xF0;           /* start with no row being scanned (row pins to 1) */
 while (1) {
     keypad &= 0xEF;                /* set RJ4 to low to scan the first row */
     if (!(keypadbits.RJ3)) {       /* read the first column */
          wait_10ms( );
          if (!(keypadbits.RJ3))
               return 0x30;  /* return the ASCII code of 0 */
     }
     if (!(keypadbits.RJ2)) {       /* read the second column */
          wait_10ms( );
          if (!(keypadbits.RJ2))
               return 0x31;          /* return the ASCII code of 1 */
…
}
```

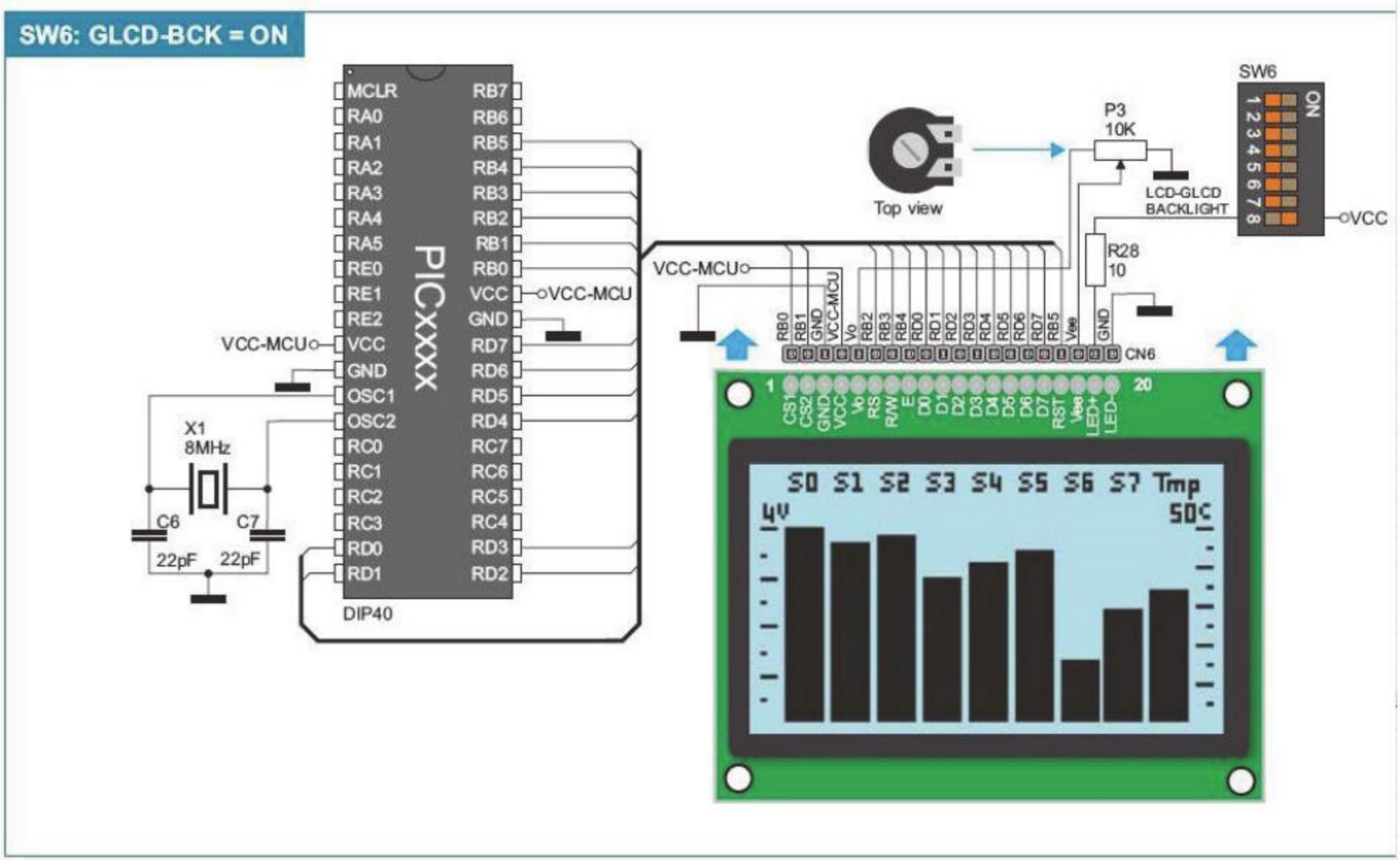
LCD



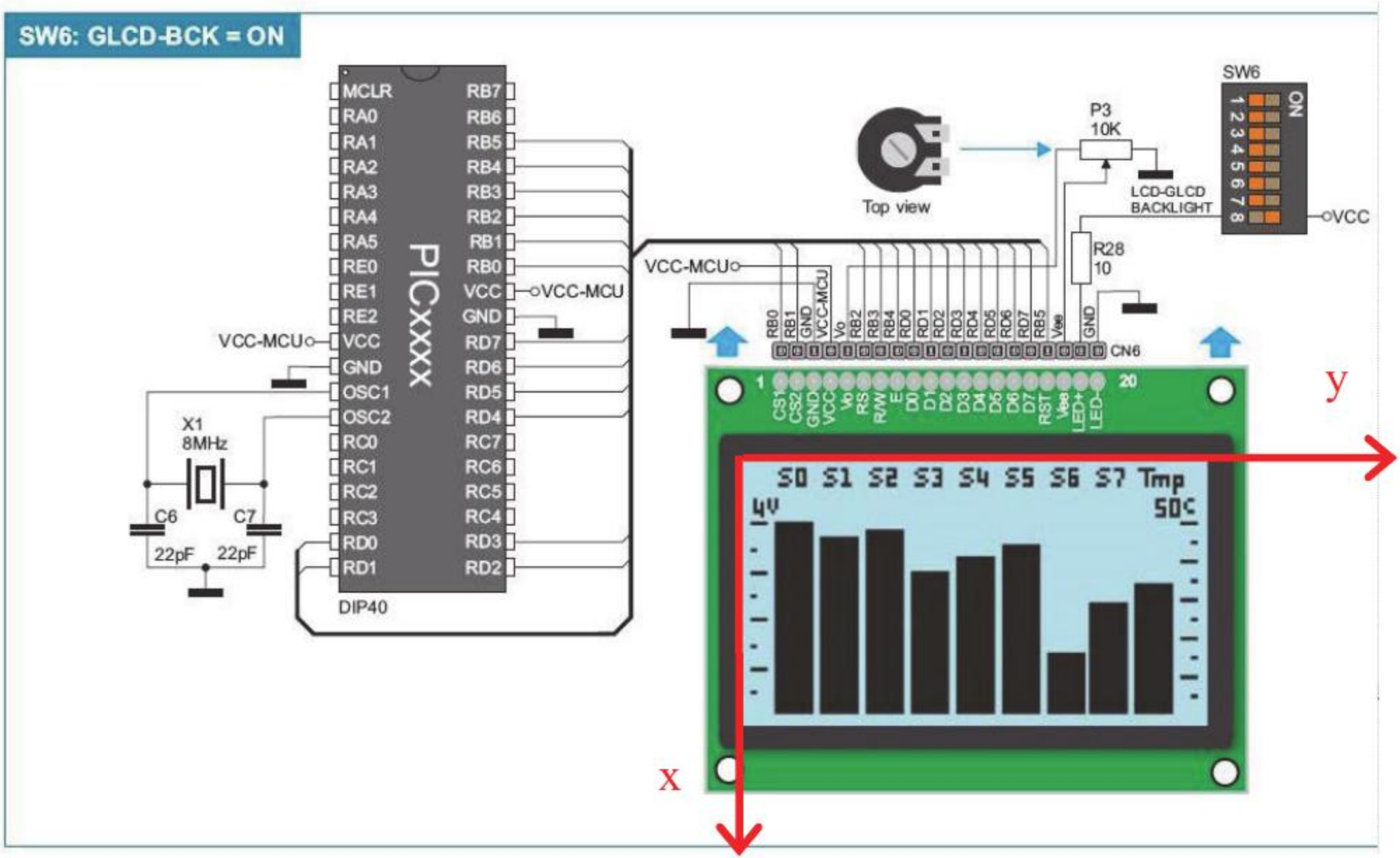

Polarizer
Color filter
Color filter glass
Liquid Crystal
Voltage
TFT glass
Polarizer
BackLight


Signal Electrodes
x1
x2
x3
x4
x5
x6
y1
y2
y3
y4
y5
y6
y7
Scanning Electrodes
(Passive Matrix LCD)

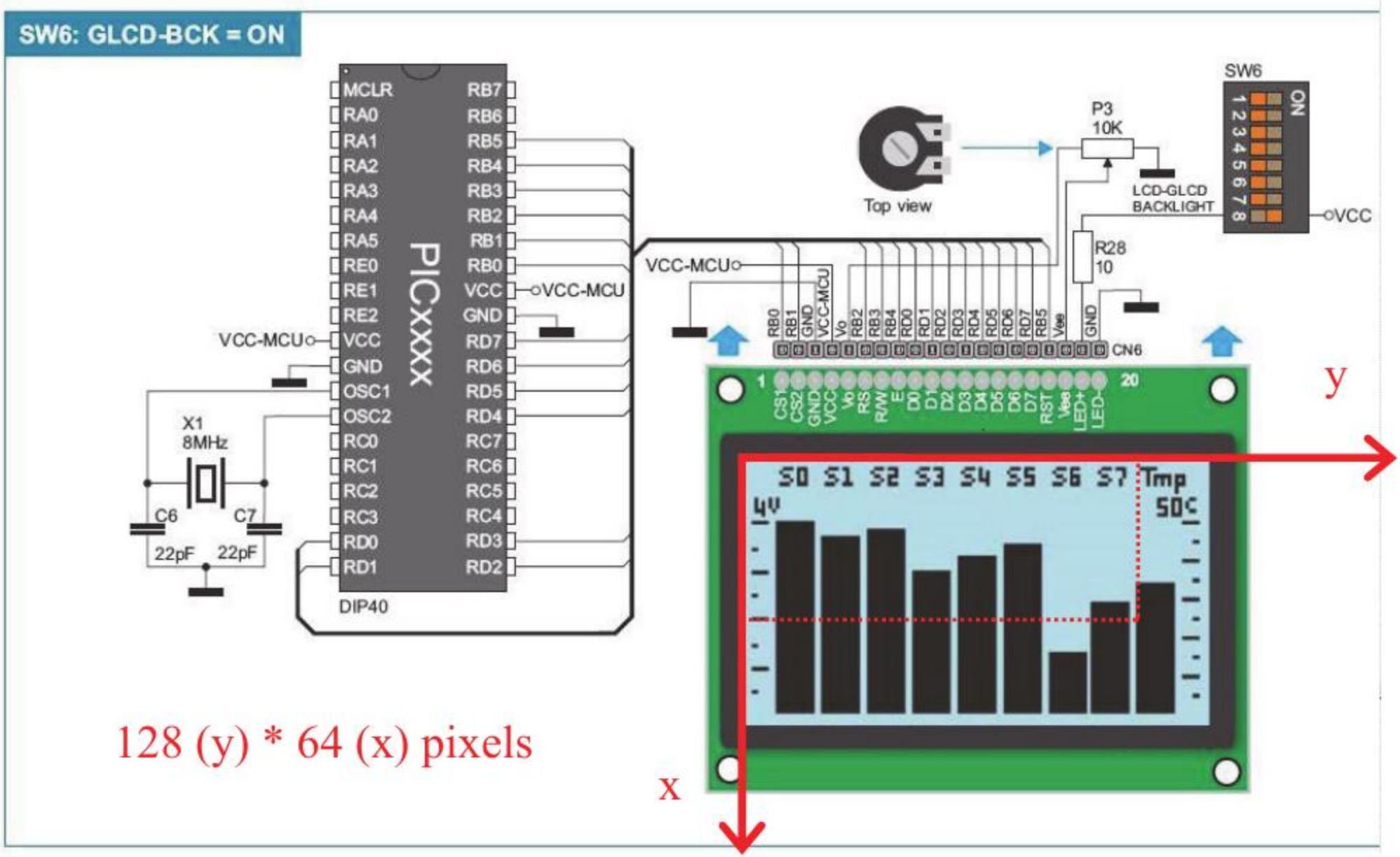
GLCD


SW6: GLCD-BCK = ON
PICxxxx
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VCC
GND
OSC1
OSC2
RC0
RC1
RC2
RC3
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VCC
GND
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
DIP40
VCC-MCU
VCC-MCU
X1
8MHz
C6
C7
22pF
22pF
Top view
P3
10K
LCD-GLCD
BACKLIGHT
SW6
ON
1 2 3 4 5 6 7 8
VCC
R28
10
RB0
RB1
GND
VCC-MCU
Vo
RB2
RB3
RB4
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RB5
Vee
GND
CN6
1
20
CS1
CS2
GND
VCC
Vo
RS
R/W
E
D0
D1
D2
D3
D4
D5
D6
D7
RST
Vee
LED+
LED-
S0 S1 S2 S3 S4 S5 S6 S7 Tmp
4V
50C

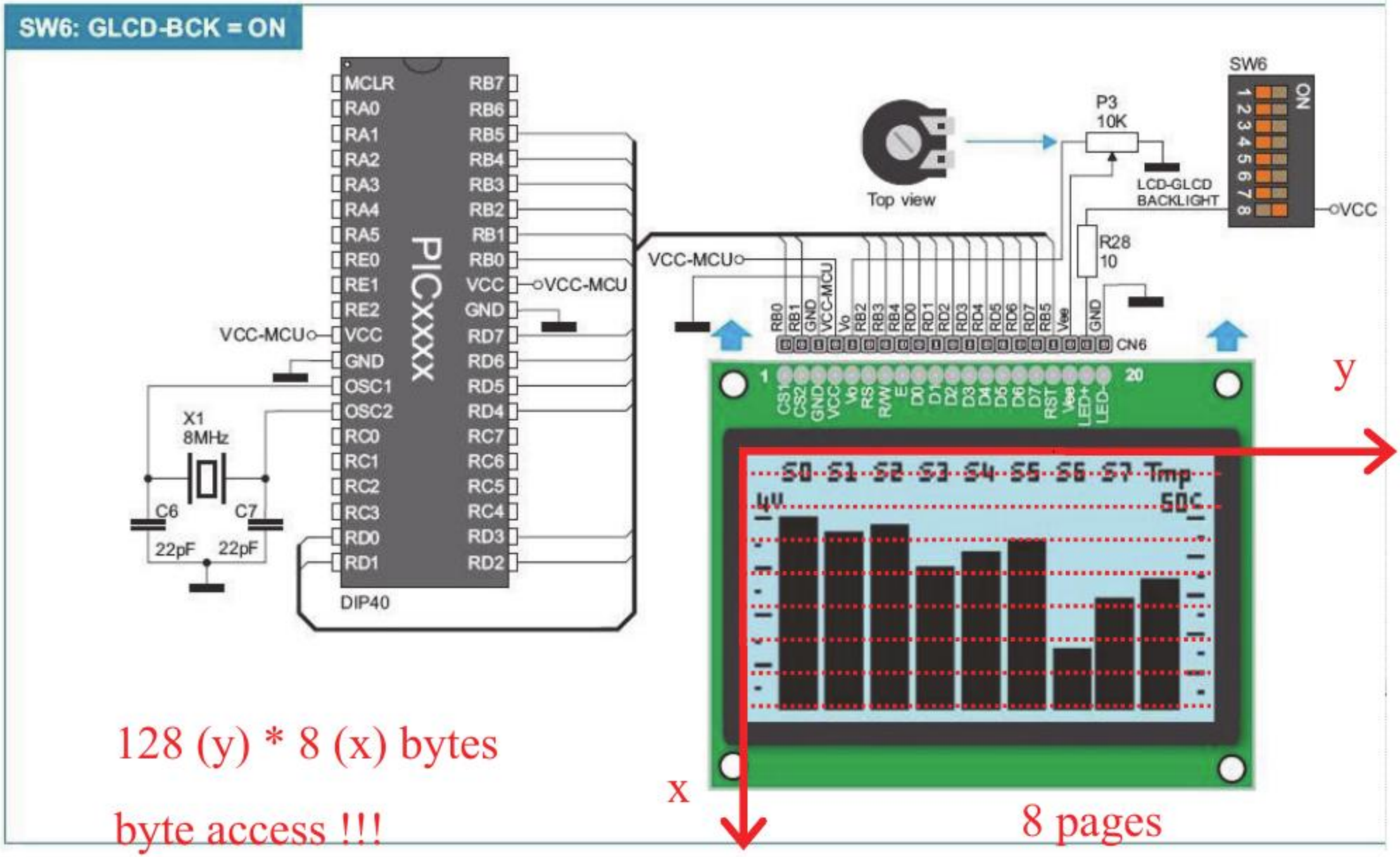
GLCD


SW6: GLCD-BCK = ON
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VCC
GND
OSC1
OSC2
RC0
RC1
RC2
RC3
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VCC
GND
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
PICxxxx
DIP40
VCC-MCU
VCC-MCU
VCC-MCU
X1
8MHz
C6
C7
22pF
22pF
Top view
P3
10K
LCD-GLCD
BACKLIGHT
SW6
ON
1 2 3 4 5 6 7 8
VCC
R28
10
RB0 RB1 GND VCC-MCU Vo RB2 RB3 RB4 RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RB5 Vee GND
CN6
1
20
CS1 CS2 GND VCC Vo RS R/W E D0 D1 D2 D3 D4 D5 D6 D7 RST Vee LED+ LED-
S0 S1 S2 S3 S4 S5 S6 S7 Tmp
4V
50C
y
x

GLCD


SW6: GLCD-BCK = ON
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VCC
GND
OSC1
OSC2
RC0
RC1
RC2
RC3
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VCC
GND
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
PICxxxx
DIP40
VCC-MCU
VCC-MCU
VCC-MCU
X1
8MHz
C6
C7
22pF
22pF
Top view
P3
10K
LCD-GLCD
BACKLIGHT
SW6
ON
1 2 3 4 5 6 7 8
VCC
R28
10
RB0 RB1 GND VCC-MCU Vo RB2 RB3 RB4 RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RB5 Vee GND
CN6
1
20
CS1 CS2 GND VCC Vo RS R/W E D0 D1 D2 D3 D4 D5 D6 D7 RST Vee LED+ LED-
S0 S1 S2 S3 S4 S5 S6 S7 Tmp
4V
50C
y
x
128 (y) * 64 (x) pixels

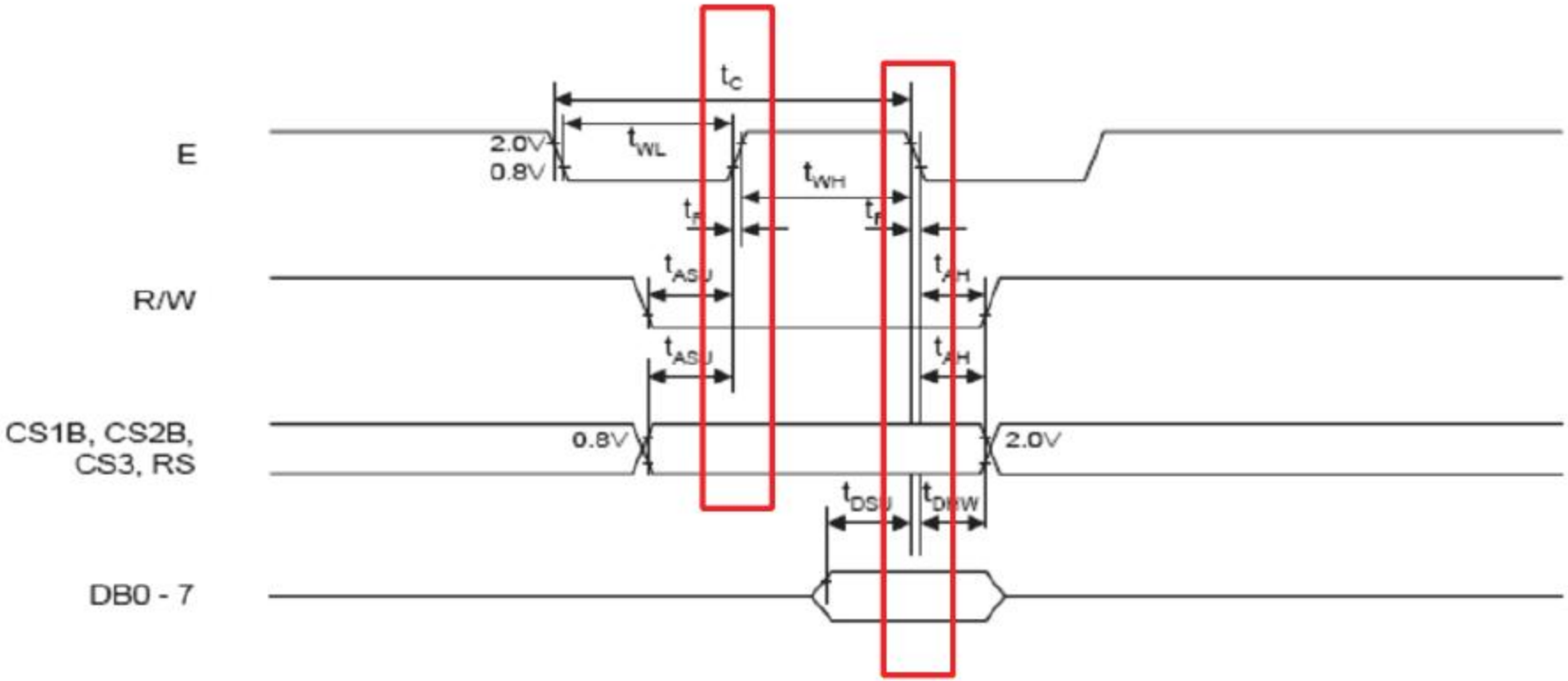
GLCD


SW6: GLCD-BCK = ON
PICxxxx
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VCC
GND
OSC1
OSC2
RC0
RC1
RC2
RC3
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VCC
GND
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
VCC-MCU
VCC-MCU
DIP40
X1
8MHz
C6
22pF
C7
22pF
Top view
P3
10K
SW6
ON
1 2 3 4 5 6 7 8
LCD-GLCD
BACKLIGHT
VCC
R28
10
VCC-MCU
RB0 RB1 GND VCC-MCU Vo RB2 RB3 RB4 RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RB5 Vee GND
CN6
1
CS1 CS2 GND VCC Vo RS R/W E D0 D1 D2 D3 D4 D5 D6 D7 RST Vee LED+ LED-
20
S0 S1 S2 S3 S4 S5 S6 S7 Tmp
uV
50C
y
x
128 (y) * 8 (x) bytes
byte access !!!
8 pages

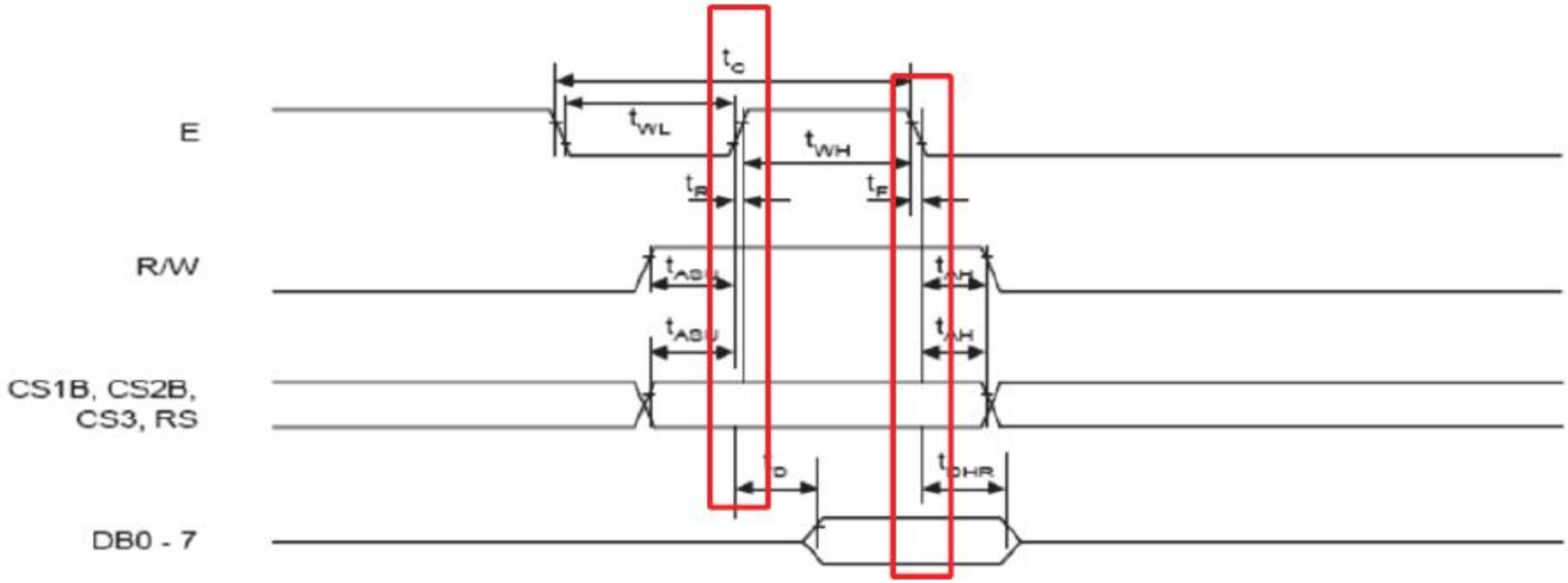
GLCD. Instruction set

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L: OFF, H: ON
Set address (Y address)	L	L	L	H	Y address (0 - 63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0 - 7)			Sets the X address at the X address register.
Display start line (Z address)	L	L	H	H	Display start line (0 - 63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On / Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0:7) from display data RAM to the data bus.

GLCD. Write timing



GLCD. Read timing



Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	t_C	1000	-	-	ns
E high level width	t_{WH}	450	-	-	ns
E low level width	t_{WL}	450	-	-	ns
E rise time	t_R	-	-	25	ns
E fall time	t_F	-	-	25	ns
Address set-up time	t_{ASU}	140	-	-	ns
Address hold time	t_{AH}	10	-	-	ns
Data set-up time	t_{DSU}	200	-	-	ns
Data delay time	t_D	-	-	320	ns
Data hold time (write)	t_{DHW}	10	-	-	ns
Data hold time (read)	t_{DHR}	20	-	-	ns