Raul Pegan

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EXPERIENCE

TALKE LAB | Esophageal Deflection Device
June 2017 – Present | University of California, San Diego

- Developed an embedded system for a medical device that deflects the esophagus away from the heart during cardiac ablation surgeries performed on atrial fibrillation patients. Publication pending submission.
- Designed the analog circuit, MCU firmware, data processing, and automation.

THE ART OF PRODUCT ENGINEERING | Staff Research Associate & Teaching Assistant
June 2016 – Present | University of California, San Diego

- Led the creation of a new upper division course for the Electrical & Computer Engineering department focusing on the creation of a full stack IoT application development.
- Developed the IoT ecosystem, from hardware stack composed of embedded Linux ARM devices attached to a custom REST API and web framework.

BROADCOM | Bluetooth SVT, Intern
Jun 2015 – September 2015 | Rancho Bernardo, CA

- Developed testing frameworks for the software and firmware of the Broadcom Bluetooth stack.
- Created a new automated regression testing environment using Perl and C to replace older systems.

ACTIVCIRK | Software Design Engineer, Intern
February 2015 – June 2015 | San Diego, CA

- Created a tool that geometrically analyzes the floorplan of MMIC GDS files and checks for design rule violations.
- Customized the DRC tool for the unique analog circuit process the company relies on.

PROJECTS

CUSTOM SCHEDULER FOR LINUX | C, ARM Assembly, Linux Kernel

- Developed custom kernel modules for a Raspberry Pi in order to access PMU readings and write a scheduler.
- Characterized the different provided workloads in order to best implement the LIST scheduler.

MIPS PIPELINE OPTIMIZATION | Verilog

- Optimized a MIPS r2000 pipeline to include state of the art improvements.
- Included features such as a victim cache, an L-TAGE predictor, and perceptron predictor.

SHA1 COPROCESSOR | Verilog

- Created a hardware encryption co-processor that uses the SHA1 encryption algorithm.
- Optimized the design to minimize critical paths and are using techniques such as loop unrolling.

EDUCATION

UNIVERSITY OF CALIFORNIA, SAN DIEGO | MS in Computer Engineering
Expected June 2019 | La Jolla, CA • Cum. GPA: 3.67

UNIVERSITY OF CALIFORNIA, SAN DIEGO | BS in Computer Engineering
June 2016 | La Jolla, CA

LANGUAGES

PROGRAMMING & TOOLS
C • Python • Perl • Verilog • Cadence VLSI tools • git
SQL • Perl • Javascript
LaTeX • C++ • CSS • PHP • Assembly

Arch Linux + i3 + Vim enthusiast

SPOKEN & WRITTEN
Native fluency:
English, Spanish
Professional working proficiency:
Italian