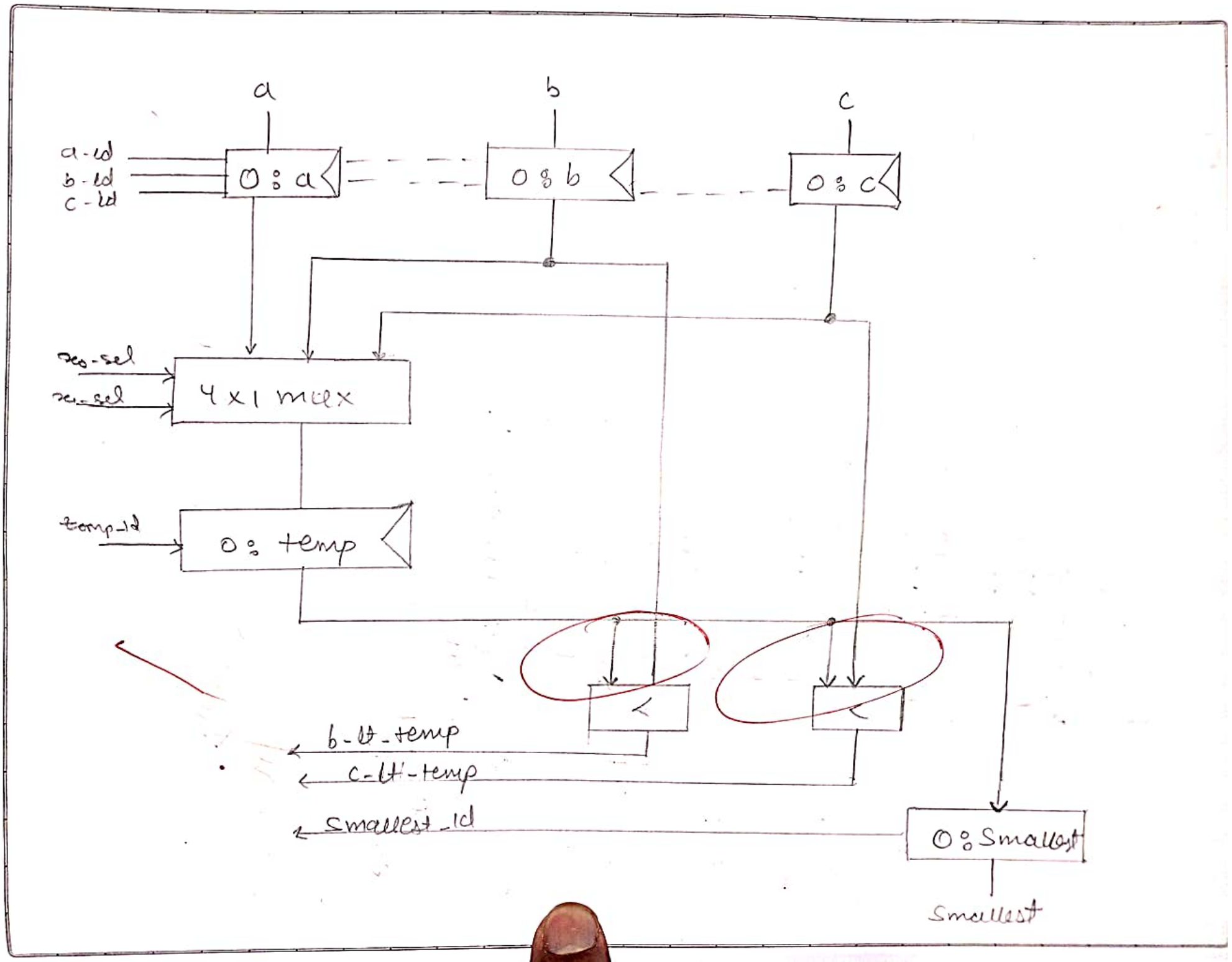
a
b
c
a-ld
b-ld
c-ld
0 : a
0 : b
0 : c
sel-sel
sel-sel
4 x 1 mux
temp-ld
0 : temp
<
<
b-lt-temp
c-lt-temp
smallest-ld
0 : Smallest
Smallest

Assignment - 3.

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Page No. 5.2

Smallest of Three Input Numbers.

Objective:

To design a VHDL logic that determines the smallest of three 4-bit input numbers (a, b, c) and outputs the smallest value.

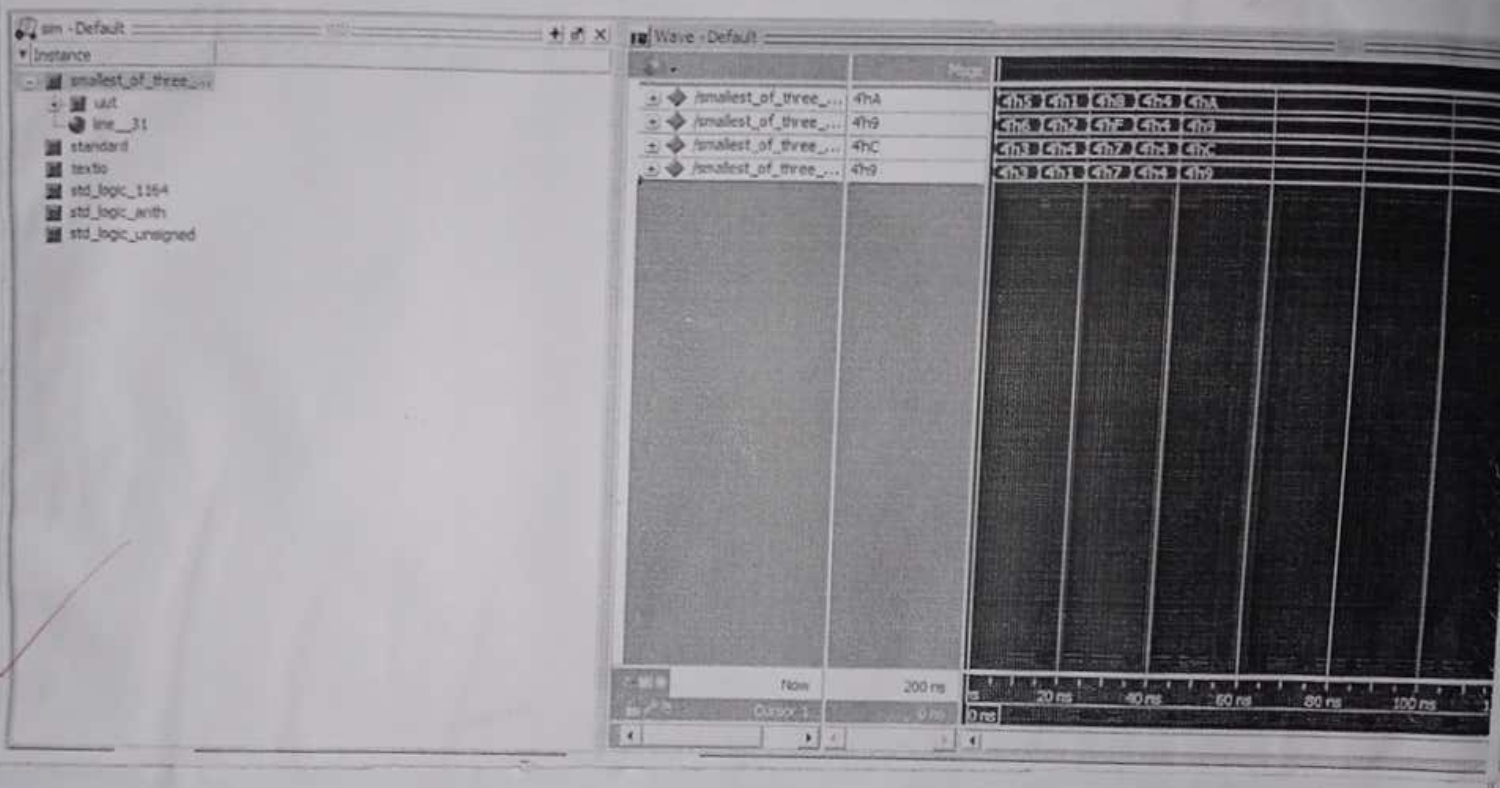
Description:

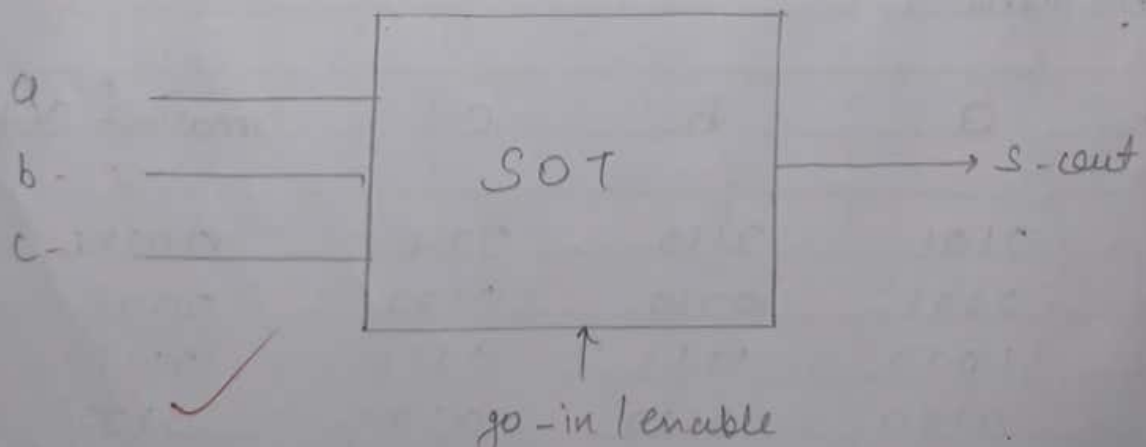
The Smallest_of_three entity compares the three 4-bit inputs (a, b, c) and assigns the smallest value to the smallest output using Conditional logic. The testbench simulates the design with various input combinations to verify the correct output is produced for each test case.

Truth Table:

Test	a	b	c	Smallest Output
1.	0101	0110	0011	0011
2.	0001	0010	0100	0001
3.	1000	1111	0111	0111
4.	0100	0100	0100	0100
5.	1010	1001	1100	1001

Teacher's Signature


sim - Default
Instance
smallest_of_three_...
uut
line__31
standard
textio
std_logic_1164
std_logic_arith
std_logic_unsigned
Wave - Default
/smallest_of_three_...
/smallest_of_three_...
/smallest_of_three_...
/smallest_of_three_...
4'hA
4'h9
4'hC
4'h9
Now
200 ns
Cursor 1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns


a
b
c
SOT
S - out
go - in / enable

Date

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- VHDL Code :-

```
library IEEE;
use IEEE.STD_Logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Smallest_of_three is
    Port (
        a : in Std_logic_vector (3 downto 0);
        b : in Std_logic_vector (3 downto 0);
        c : in Std_logic_vector (3 downto 0);
        Smallest : out Std_logic_vector (3 downto 0));

end Smallest_of_three;

architecture Behavioral of Smallest_of_three is
begin
    process (a, b, c)
    begin
        temp <= A
        if B < temp then
            temp <= B;
        end if
        if C < temp then
            temp <= C
        end if
        Smallest <= temp;
    end process;
end Behavioral;
```

Teacher's Signature

- Test Bench Code

```
library IEEE;
Use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;


entity smallest_of_three_tb is
end smallest_of_three_tb;

architecture Behavioral of smallest_of_three_tb is

    signal a : std_logic_vector (3 downto 0);
    signal b : std_logic_vector (3 downto 0);
    signal c : std_logic_vector (3 downto 0);
    signal smallest : std_logic_vector (3 downto 0);
```

```
begin
    uut : smallest_of_three
        port map (a=>a, b=>b, c=>c, smallest=>smallest
```

Date

Expt. No.

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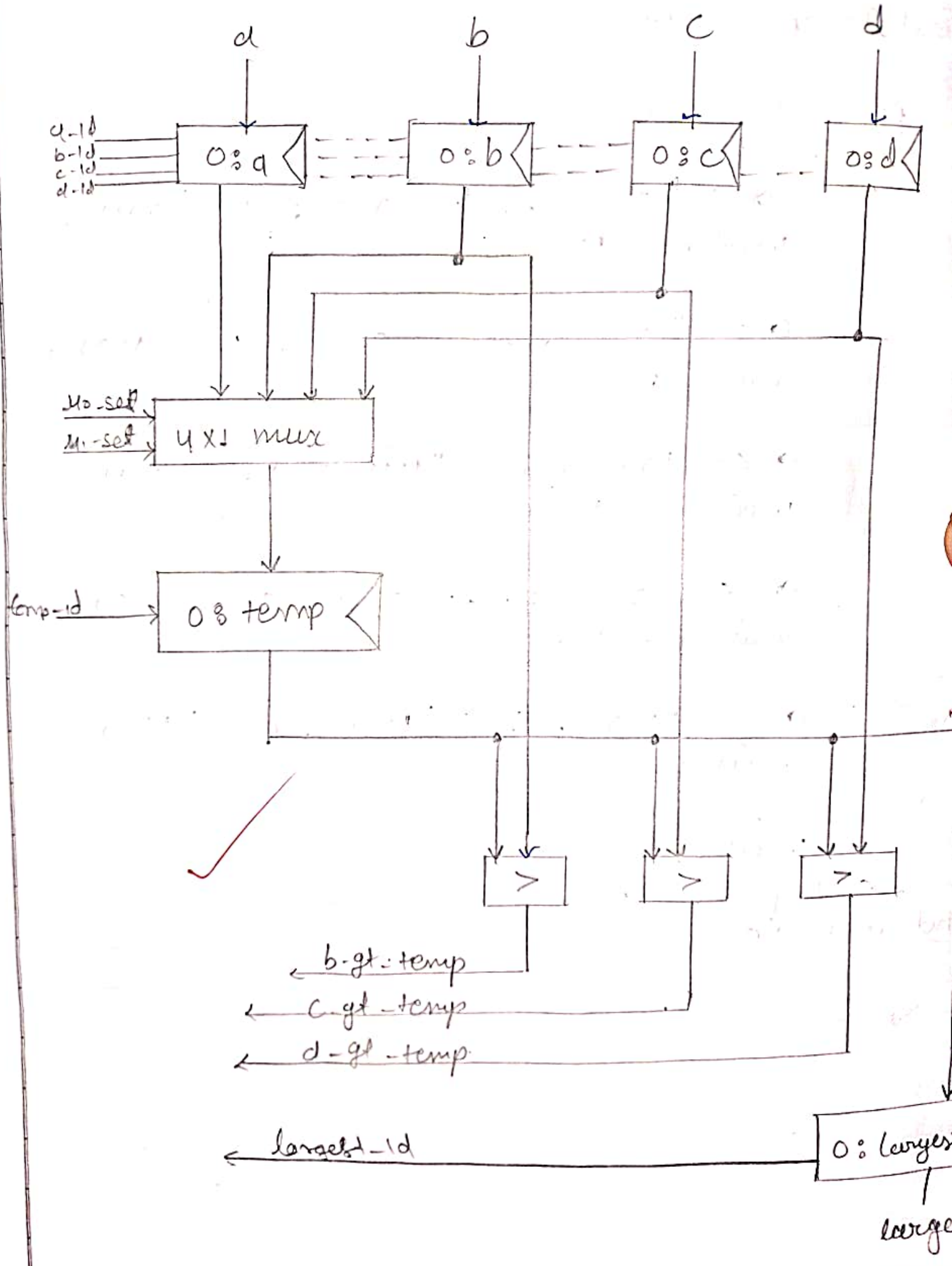
• Test Bench Code

```
process
begin
    a <= "0101" ; b <= "0110" ; c <= "0011" ;
    wait for 10 ns;

    a <= "0001" ; b <= "0010" ; c <= "0100" ;
    wait for 10 ns;

    a <= "1000" ; b <= "1111" ; c <= "0111" ;
    wait for 10 ns;

    a <= "0100" ; b <= "0100" ; c <= "0100" ;
    wait for 10 ns;

    a <= "1010" ; b <= "1001" ; c <= "1100" ;
    wait for 10 ns;

    wait ;
end process;
end Behavioral;
```

Teacher's Signature


a
b
c
d
a-ld
b-ld
c-ld
d-ld
O: a
O: b
O: c
O: d
M0-sel
M1-sel
4 X 1 mux
temp-ld
O: temp
>
>
>
b-gt-temp
c-gt-temp
d-gt-temp
largest-ld
O: larges
large

Expt. No. 2. Date

Page No. 5 9

Largest Among Four 4-bit input Numbers.

Objective :-

To design a VHDL logic that determines the largest of four 4-bit input numbers (a,b,c,d) and outputs the largest value.

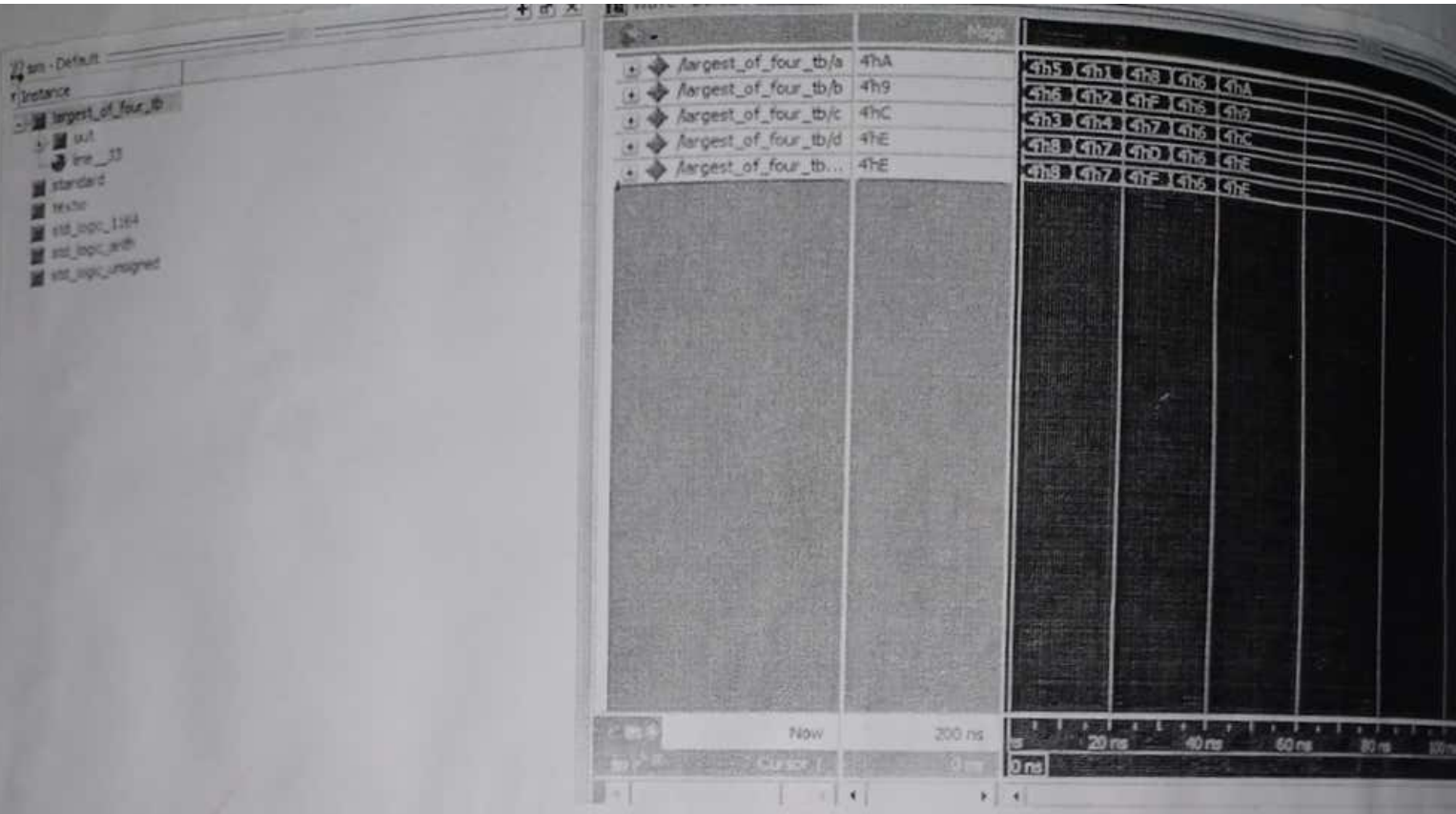
Description:

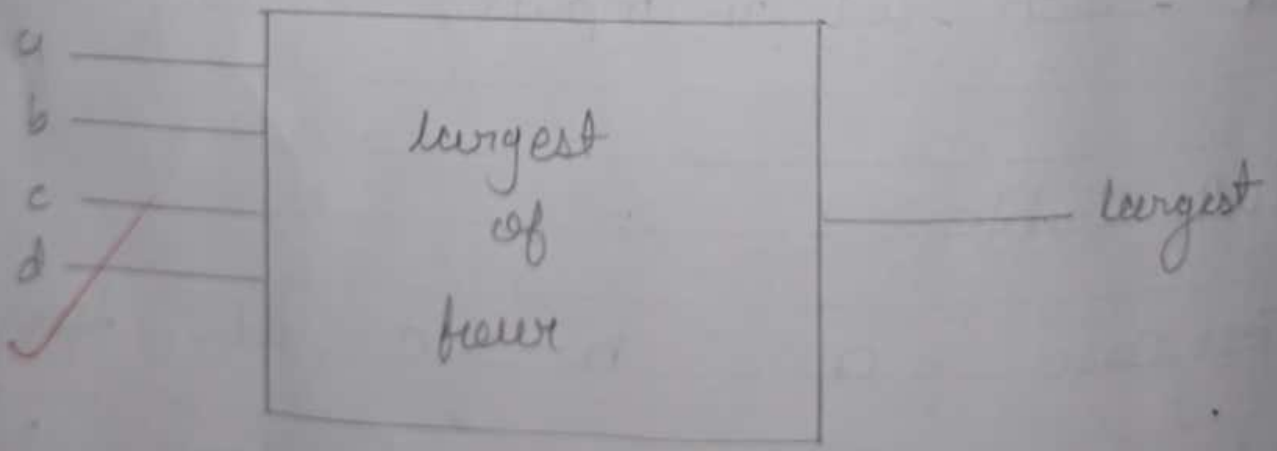
The largest_of_four entity compares the four 4-bit inputs (a,b,c,d) and assigns the largest value to the largest output using Conditional logic. The testbench simulates the design by applying various test cases with different input combinations to ensures that the largest value is correctly computed and output for each set of inputs.

Truth Table:

Test Case	a	b	c	d	largest
1	0101	0110	0011	1000	1000
2	0001	0010	0100	0111	0111
3	1000	1111	0111	1101	1111
4	0110	0110	0110	0110	0110
5	1010	1001	1100	1110	1110

Teacher's Signature


/largest_of_four_tb/a
/largest_of_four_tb/b
/largest_of_four_tb/c
/largest_of_four_tb/d
/largest_of_four_tb...
4'hA
4'h9
4'hC
4'hE
4'hE
Now
200 ns
20 ns
40 ns
60 ns


a
b
c
d
largest
of
four
largest

Expt. No. _____ Date _____

Page No. 5 8

- VHDL Code:

```
library IEEE;
use ieee.Std_logic_1164.all;
use ieee.Std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity Largest_of_four is
      port (
            a : in std_logic_vector (3 downto 0);
            b : in std_logic_vector (3 downto 0);
            c : in std_logic_vector (3 downto 0);
            d : in std_logic_vector (3 downto 0);
          Largest : out std_logic_vector (3 downto 0));
end Largest_of_four;

architecture Behavioral of Largest_of_four is
begin
    process (a,b,c,d)
    begin
        temp <= A
        if B > temp then
            temp <= B;
        endif;
        if C > temp then
            temp <= C;
        end if;
        if D > temp then
            temp <= D;
        end if
            Largest <= temp;
        end if;
    end process;
end Behavioral;
```

Teacher's Signature _____

· Test Bench Code :-

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity largest_of_four_tb is
end largest_of_four_tb;

architecture Behavioral of largest_of_four_tb is

    signal a : std_logic_vector (3 downto 0);
    signal b : std_logic_vector (3 downto 0);
    signal c : std_logic_vector (3 downto 0);
    signal d : std_logic_vector (3 downto 0);
    signal largest: std_logic_vector (3 downto 0);
```

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```
begin
    uut : largest_of_four
        Port map (a=>a, b=>b, c=>c, d=>d, largest=>
                  largest );

    process
    begin
        a <= "0101"; b <= "0110"; c <= "0011"; d <= "1000";
        wait for 10 ns;

        a <= "0001"; b <= "0010"; c <= "0100"; d <= "0111";
        wait for 10ns;

        a <= "1000"; b <= "1111"; c <= "0111"; d <= "1101";
        wait for 10 ns;

        a <= "0110"; b <= "0110"; c <= "0110"; d <= "0110";
        wait for 10ns;

        a <= "1010"; b <= "1001"; c <= "1100"; d <= "1110";
        wait for 10 ns;

        wait;

    end process;
end Behavioral;
```

15/2/2025

Teacher's Signature _____