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Department of Computer Science and Engineering

Topic: Basic and Universal Gates -iVerilog

Sub Code: 19CSE211 **Sub Title:** Computer Organization and Architecture

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Activity No:1 **Date:11-01-2021**

1.) OR GATE :

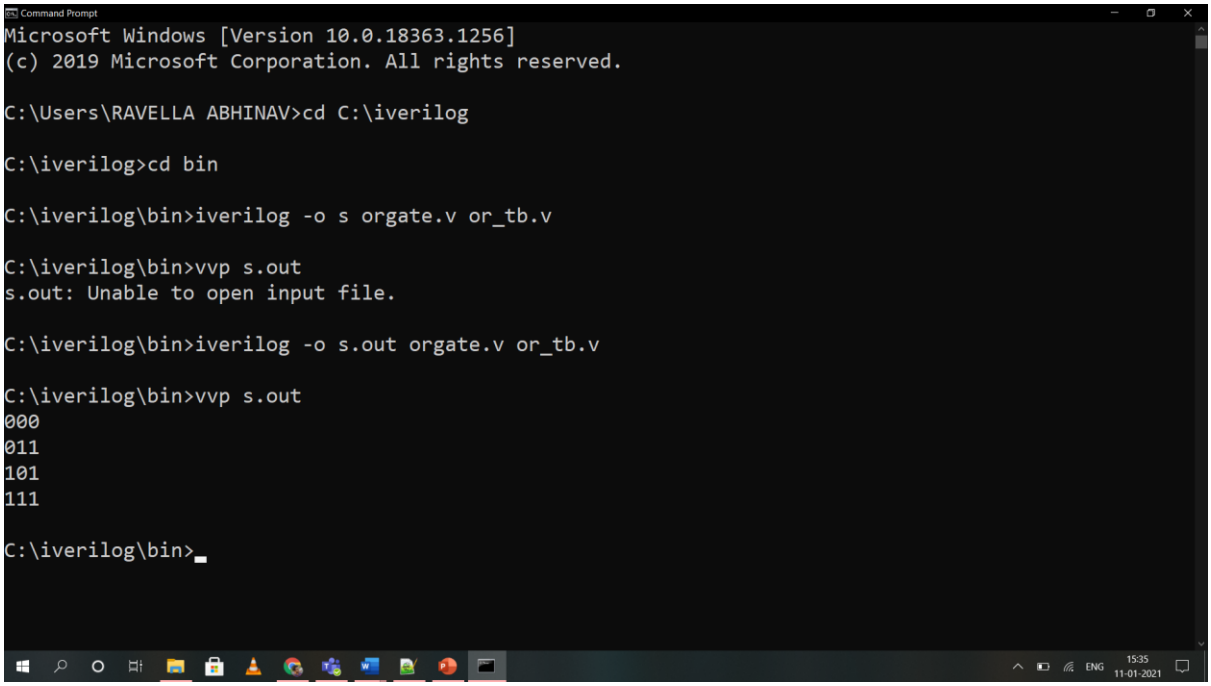
```
module orgate (a,b,y);
input a,b;
output y;
assign y= a| b;
endmodule
```

Test bench:

```
module orgate_tb;
wire t_y;
reg t_a, t_b;
orgate my_gate( .a(t_a), .b(t_b), .y(t_y) );
initial
begin
$monitor(t_a,t_b,t_y);
t_a  = 1'b0;
t_b = 1'b0;
#5
t_a  = 1'b0;
t_b = 1'b1;
#5
t_a  = 1'b1;
t_b = 1'b0;
#5
t_a  = 1'b1;
t_b = 1'b1;

end
endmodule
```

Output:


Command Prompt
Microsoft Windows [Version 10.0.18363.1256]
(c) 2019 Microsoft Corporation. All rights reserved.
C:\Users\RAVELLA ABHINAV>cd C:\iverilog
C:\iverilog>cd bin
C:\iverilog\bin>iverilog -o s orgate.v or_tb.v
C:\iverilog\bin>vvp s.out
s.out: Unable to open input file.
C:\iverilog\bin>iverilog -o s.out orgate.v or_tb.v
C:\iverilog\bin>vvp s.out
000
011
101
111
C:\iverilog\bin>
ENG
15:35
11-01-2021

2.)AND GATE:

```
module andgate (a, b, y);
input a, b;
output y;
assign y = a & b;
endmodule
```

Test bench:

```
module andgate_tb;
wire t_y;
reg t_a, t_b;

andgate my_gate( .a(t_a), .b(t_b), .y(t_y) );

initial
begin
$monitor(t_a, t_b, t_y);
t_a = 1'b0;
t_b = 1'b0;
#5
t_a = 1'b0;
t_b = 1'b1;
#5
t_a = 1'b1;
t_b = 1'b0;
#5
t_a = 1'b1;
t_b = 1'b1;

end
endmodule
```

Output:


Microsoft Windows [Version 10.0.18363.1256]
(c) 2019 Microsoft Corporation. All rights reserved.
C:\Users\RAVELLA ABHINAV>cd C:\iverilog\bin
C:\iverilog\bin>iverilog -o an.out and_gate.v tb_and_gate.v
C:\iverilog\bin>vvp an.out
000
010
100
111
C:\iverilog\bin>

3.)NOT GATE:

```
module notgate (a,y);
input a;
output y;
assign y = !a;
endmodule
```

Test bench:

```
module notgate_tb;
wire y;
reg a;

notgate my_gate( .a(a),.y(y) );

initial
begin
$monitor(a,y);

a=1'b0;

#10
a=1'b1;

end endmodule
```

Output:

```
Microsoft Windows [Version 10.0.18363.1256]
(c) 2019 Microsoft Corporation. All rights reserved.

C:\Users\RAVELLA ABHINAV>cd C;\iverilog\bin
The system cannot find the path specified.

C:\Users\RAVELLA ABHINAV>cd c:\iverilog\bin

c:\iverilog\bin>iverilog notgate.out notgate.v notgate_tb.v
notgate.out: No such file or directory
No top level modules, and no -s option.

c:\iverilog\bin>iverilog -o notgate.out notgate.v notgate_tb.v

c:\iverilog\bin>vvp notgate.out
01
10

c:\iverilog\bin>
```

4.)NAND GATE:

```
module nand_gate(c,a,b);
input a,b;
output c;
nand (c,a,b);
endmodule
```

Test Bench:

```
module nand_test;
reg a,b;
wire c;
nand_gate  nand_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
end
initial
begin
$monitor("a=%b,b=%b,c=%b",a,b,c);
end
endmodule
```

Output:


Microsoft Windows [Version 10.0.18363.1256]
(c) 2019 Microsoft Corporation. All rights reserved.
C:\Users\RAVELLA ABHINAV>cd C:\iverilog\bin
C:\iverilog\bin>iverilog -o nand.out nand_gate.v nand_test.v
C:\iverilog\bin>vvp nand.out
a=0,b=0,c=1
a=0,b=1,c=1
a=1,b=0,c=1
a=1,b=1,c=0
C:\iverilog\bin>