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Topic: Basic ALU Implementation using iVerilog

Sub Code: 19CS211	**Sub Title: COA**
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Lab Evaluation No: 3	**Date: 01-03-2021**

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1. Design of 1 bit ALU with the following operations

iVerilog Code:

```
module ALU(A,B,Operation,out);
input [3:0]A, B;
input [2:0] Operation;
output reg [3:0] out;
always@(*)
begin
    case(Operation)
      3'b000: out= A+B;
      3'b001: out= A-B;
      3'b010: out= A & B;
      3'b011: out= A | B;
      3'b100: out= ~A;
      3'b101: out= ~(A & B);
      3'b110: out= ~(A | B);
      3'b111: out= 0;
      default: out=0;
    endcase
end
endmodule
```

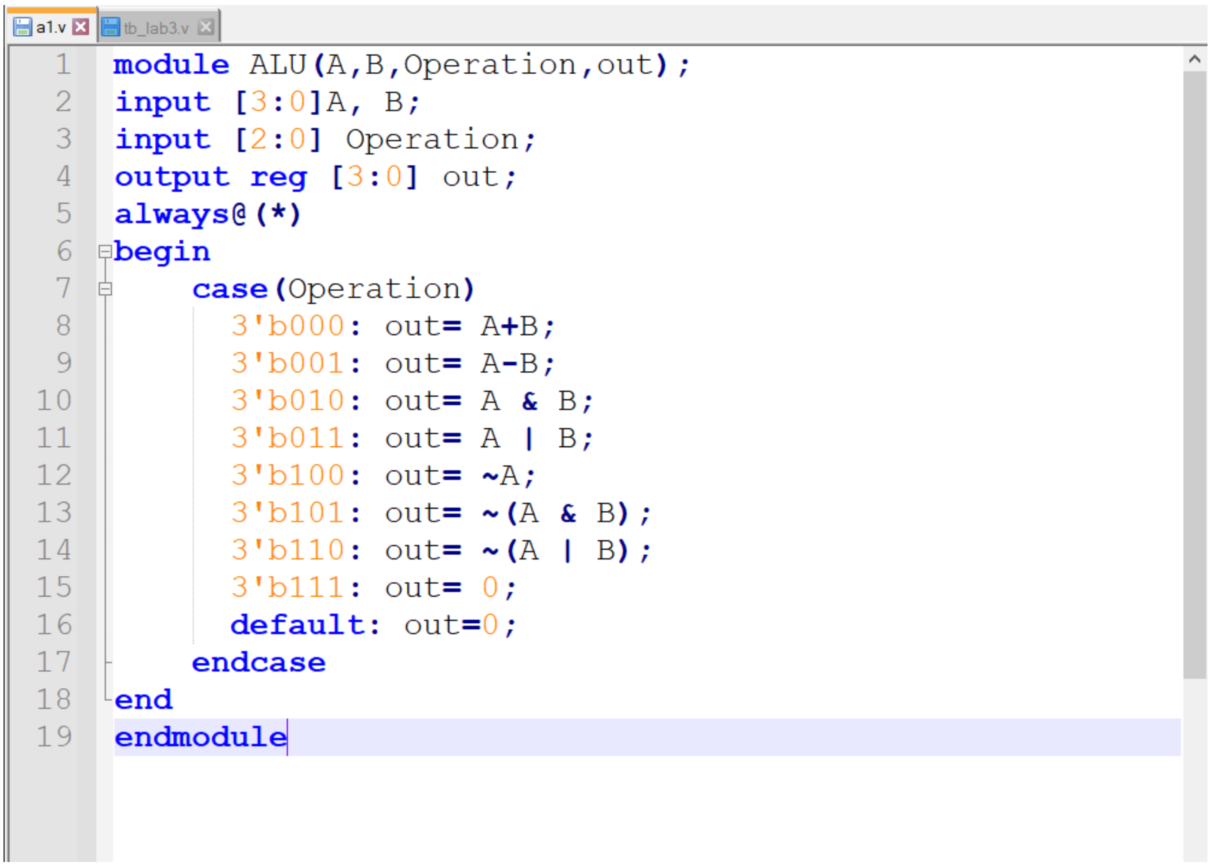
TestBench :

```
module ALU_tb;
wire t_out;
reg t_x, t_y, t_z, t_x, t_y;
ALU_m my_gate( .a(t_x), .b(t_y), .x(t_x), .y(t_y), .z(t_z), .out(t_out) );
```

```
initial
begin

	$monitor("X:%b Y:%b Z:%b | A:%b B:%b | Output:%b \n", t_x, t_y, t_z, t_x,
t_y, t_out );

	t_a = 1'b0;
	t_b = 1'b0;
	t_x = 1'b0;
	t_y = 1'b0;
	t_z = 1'b0;

	#5
	t_a = 1'b0;
	t_b = 1'b0;
	t_x = 1'b0;
	t_y = 1'b0;
	t_z = 1'b1;

	#5
	t_a = 1'b0;
	t_b = 1'b0;
	t_x = 1'b0;
	t_y = 1'b1;
	t_z = 1'b0;

	#5
	t_a = 1'b0;
```

```
t_b = 1'b0;
t_x = 1'b0;
t_y = 1'b1;
t_z = 1'b1;

#5
t_a = 1'b0;
t_b = 1'b0;
t_x = 1'b1;
t_y = 1'b0;
t_z = 1'b0;

#5
t_a = 1'b0;
t_b = 1'b0;
t_x = 1'b1;
t_y = 1'b0;
t_z = 1'b1;

#5
t_a = 1'b1;
t_b = 1'b1;
t_x = 1'b1;
t_y = 1'b1;
t_z = 1'b0;

#5
t_a = 1'b1;
t_b = 1'b1;
```

```
        t_x = 1'b1;
        t_y = 1'b1;
        t_z = 1'b1;

end
endmodule
```



```
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      3'b110: out= ~(A | B);
      3'b111: out= 0;
      default: out=0;
    endcase
end
endmodule
```