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19ECE204 Digital Electronics and Systems: Odd 2020-21 Lecture Plan

Key-words	Lecture No.	Topics	Sections and pages (in brackets)		
Introduction to logic circuits - Variables and functions, inversion - Truth tables - Logic gates and Networks - Boolean algebra - Synthesis using gates	1	Why Digital?		CO1, CO2	
	2	Variables, Functions, Properties and Identities and Minimization	2.1 to 2.5 (20-32)	CO1, CO2	
	3	Synthesis using AND, OR and NOT gates	2.6 (37-45)	CO1, CO2	
	4	PoS and SoP forms, Canonical forms, Minterms and Maxterms		CO1, CO2	
	5	NAND and NOR Logic Networks, XOR Gates	2.7, 2.8 3.9.1 (45-50, 139)	CO1, CO2	
	6	**QUIZ 1 (1-5)**		CO1, CO2	
Karnaugh map, SOP, POS, Tabulation method	7	Introduction to K-Maps	4.1,4.2.1 (167-178)		
	8	Minimization Procedure for SoP	4.2 (178-181)		
	9	Examples for K-Map Minimization of SoP Forms			
	10	K-Map Minimization of PoS Forms	4.3 (181-183)		
	11	Incompletely Specified Functions	4.4 (183-185)		
	12	**QUIZ 2 (7-11)**			
	13	Examples on Minimization of Incomplete Functions			
	14	Tabulation Method	4.9 (211-219)		
	15	Tabulation Method: Examples			
	16	**TUTORIAL TEST 1 (9-15)**			
Addition of unsigned numbers, Signed numbers	17	Review of Number Systems, Unsigned Addition and Adders	5.1, 5.2 (247-259)		
	18	Signed Number Representation	5.3.1 to 5.3.2 (259- 265)		
	19	Signed Addition, Subtraction and Radix Complementation	5.3.3 to 5.3.6 (265-272)		
	20	Examples in Signed and Unsigned Arithmetic			
	21	**QUIZ 3 (17-20)**			

Multiplexers, Decoders, Encoders, Code Converters, Comparators, Fast adders	22	Multiplexers, Synthesis of Logic Functions using MUXes	6.1 (322-335)		
	23	Examples of Logic Synthesis with MUXes			
	24	Decoders	6.2 (336-341)		
	25	Encoders and Code Converters	6.3-6.4 (341-345)		
	26	**TUTORIAL TEST 2 (22-25)**			
	27	Comparators	6.5, Example 5.10 (Excluding Verilog part) (344-345, 311-313)		
	28	Fast Adders	5.4 (272-279)		
	29	BCD Representation, BCD Adder	5.7.3 (Excluding Verilog Code) (302-305)		
	30	**QUIZ 4 (27-29)**			
31		**MID TERM TEST (1-30)**			
Latches, SR, JK, T, D, Flip Flops	32	Basic Latch	7.1-7.3 (384-390)		
	33	Gated D-Latch, Master-Slave and Edge-triggered D Flip-flops	7.4.1-7.4.2 (393-397)		
	34	Clear and Preset, Timing, T and JK Flip-flops	7.4.3-7.7 (397-403)		
	35	Conversion of Flip-flops	Handout		
	36	**QUIZ 5 (32-35) REMOVED**			
	36	Registers, Shift Registers and Ripple Counters	7.8-7.9.1 (404-409)		
	37	Synchronous Counters	7.9.2-7.9.3 (409-417)		
	38	BCD Counter, Ring Counter and Johnson Counter	7.10-7.11 (417-421)		
	40	**TUTORIAL TEST 3 (32-39) REMOVED**			
State Machine	39	Moore Finite State Machine - Basic Design Steps	8.1.1-8.1.5		

Design			(488-496)		
	40	Design Example	8.1.6 (496-499)		
	41	State Assignment and Encoding	8.2 (499-504)		
	44-45	Serial Adder and other Examples **REMOVED**	8.5.2 and additional examples		
	42	**QUIZ 5 (32-41) REMOVED**			
	47	State Minimization **REMOVED**	8.6.1 (529-537)		
	43-44	Counter Design Example	8.7 excluding 8.7.4 and 8.7.5 (538-542)		
	45	Arbiter FSM Example, Brief introduction to Mealy FSM Model	8.8 Introduction only, Exclude Verilog, Exclude 8.8.1 and 8.8.2, 8.8.3 (546-550)		
	46	Examples in FSM Design			
	47	**TUTORIAL TEST 3 (39-46)**			
Asynchronous Behavior, Analysis of Asynchronous circuits	48	Introduction to Asynchronous Circuits	9.1 (582-586)		
	54	Analysis of Asynchronous Circuits	9.2 (586-594)	**REMOVED**	
Introduction to CMOS	55	Transistor Switches, nMOS, CMOS	3.1-3.3 (78-91)		
	56	**QUIZ 7 (53-55)**			

TEXT BOOK: Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital logic with Verilog Design", Tata McGraw Hill Publishing Company Limited, Special Indian Edition, 2007.

REFERENCES:

1. Morris Mano, "Digital Design", Pearson Education, Third Edition,
2. Donald D Givone, "Digital Principles and Design", Tata McGraw Hill Publishing Company Limited, 2003.
3. Allen Dewey, "Analysis and Design of Digital Systems with VHDL", PWS Publishing Company, 1999.
4. John F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 3rd Ed, 2001.

EVALUATION PATTERN

Quizzes	– 25 marks
Tutorial Tests	- 15 marks
Home Assignments	– 15 marks
Mid Term Test	– 15 marks
End Semester Online Examination	– 15 marks
End Semester Viva	- 15 marks

NOTE:

1. The topics included in each evaluation component are given in brackets as lecture nos.
2. The quizzes will comprise MCQ and fill in the blank questions for 30 minutes duration. Each quiz will be for 10 marks and will comprise 5 Fill in the Blanks questions and 5 MCQ questions.
3. The tutorials will be 30 min and consist of word problems (3 problems). The total marks for each tutorial test will be 15 (5 marks for each question). The students have to write down the solutions with steps, scan the answer sheet and upload the PDF to AUMS/AMPLE
4. Home assignments will comprise 10-15 problems related to the topics that are indicated in the lecture plan. Each Assignment will have a maximum of 30 marks.
5. Mid Term Test and End Semester Online exam will have a mix of short-answer questions and descriptive problems