* 19ECE204 *

CB.EN.U4CSE19453

Digital Electronics and Systems

ASSIGNMENT - II

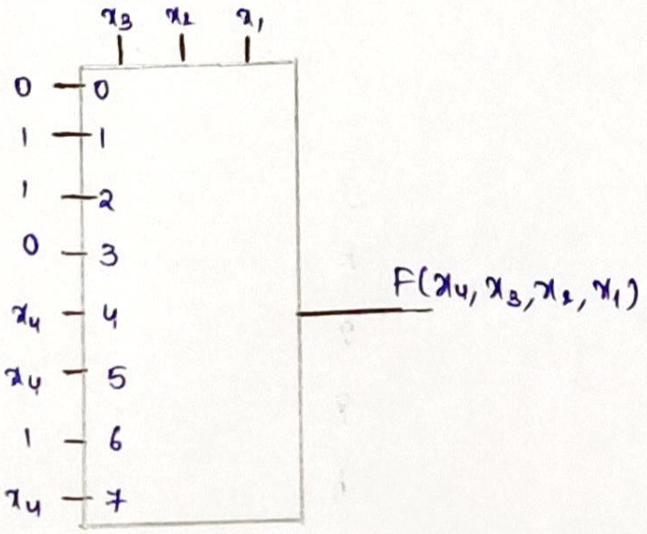
1.) $F(x_1, x_2, x_3, x_4) = \Sigma m(1,2,6,9,10,12,13,14,15)$

We can design the function F using 3:8 mux where each terminal can represent two inputs without use of basic gates (assuming negated literals are available universely)

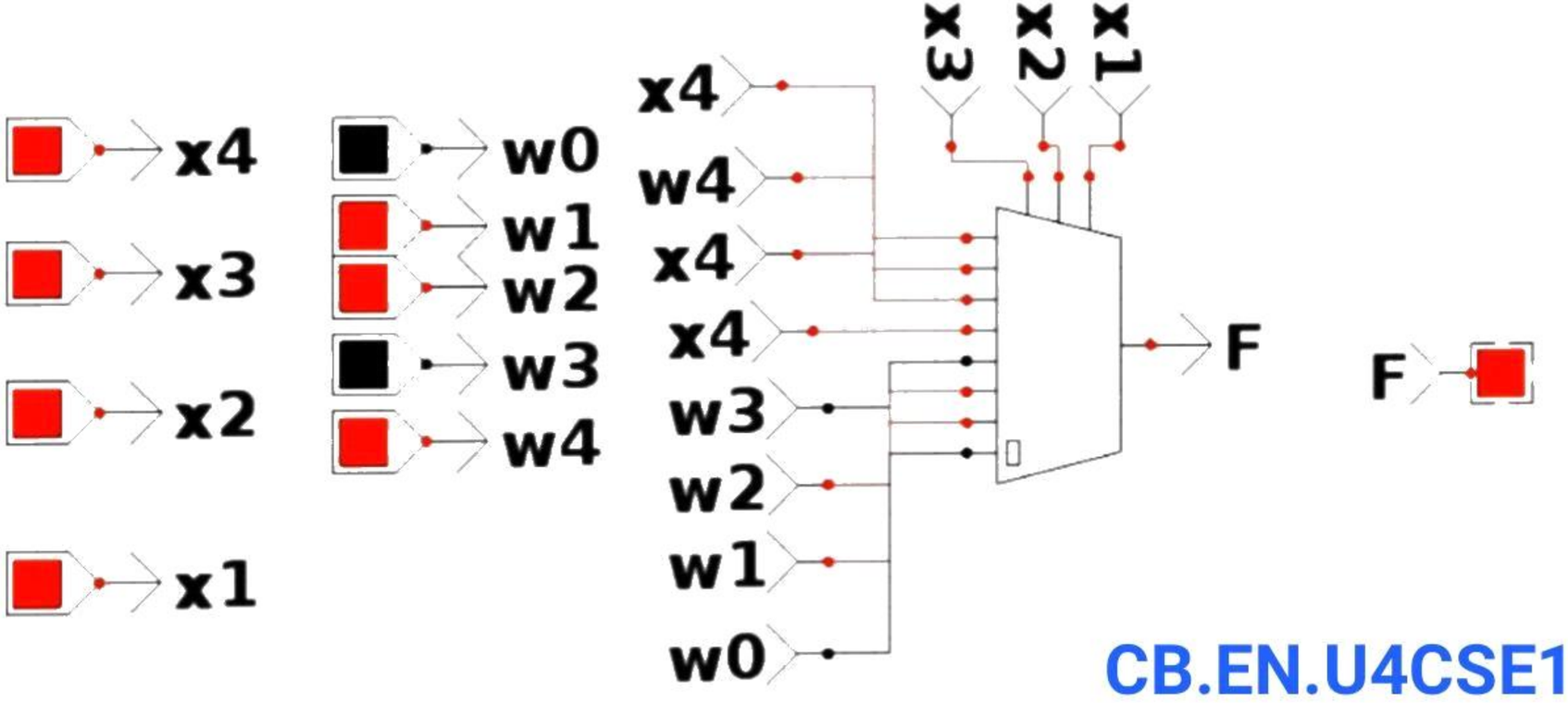
X	✓	✓	X	X	X	✓	X
0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
X	✓	✓	X	✓	✓	✓	✓

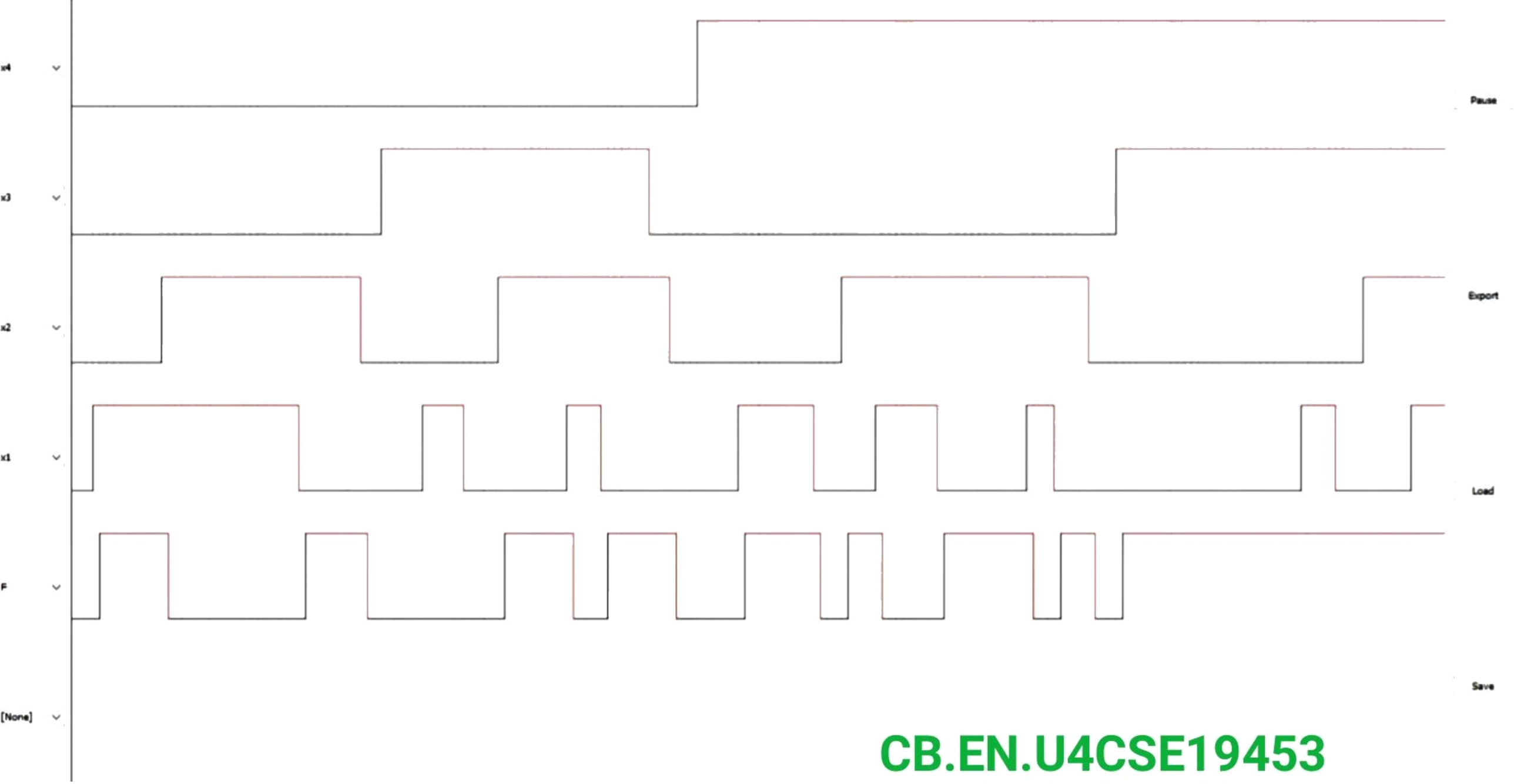
Curtailed Truth Table

The modelled MUX is shown below :-



F(X4,X3,X2,X1)=sigma m(1,2,6,9,10,12,13,14,15)





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2) $F(x_1, x_2, x_3) = \Sigma m(1, 2, 6, 7)$

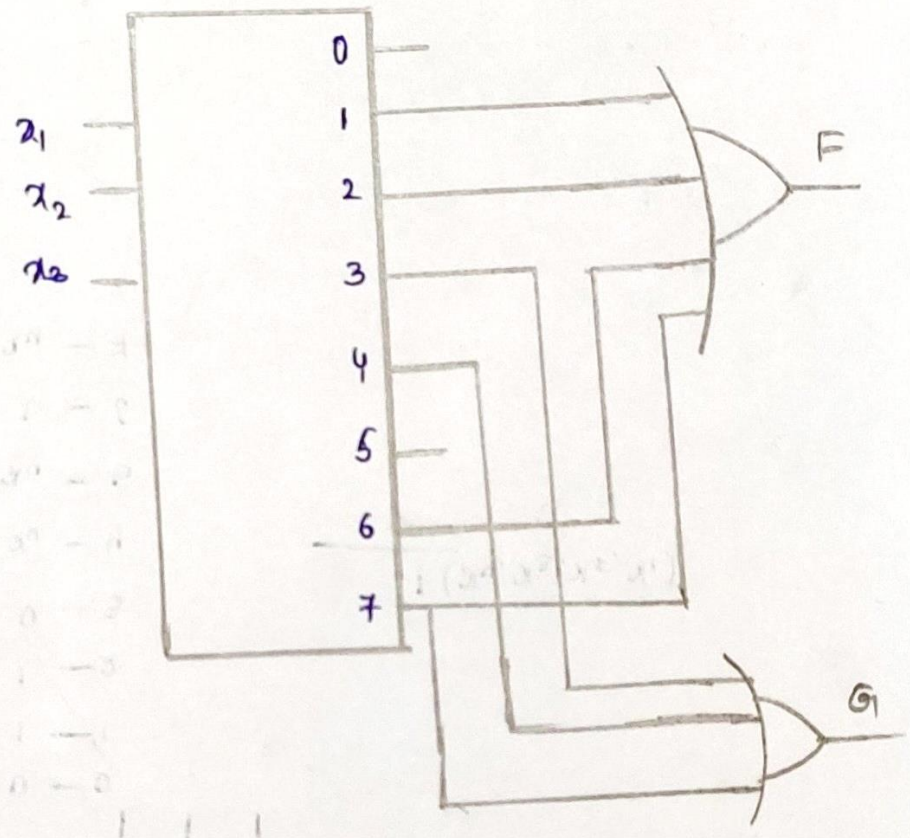
Using 'OR' the given minterm to realise F through a decoder.

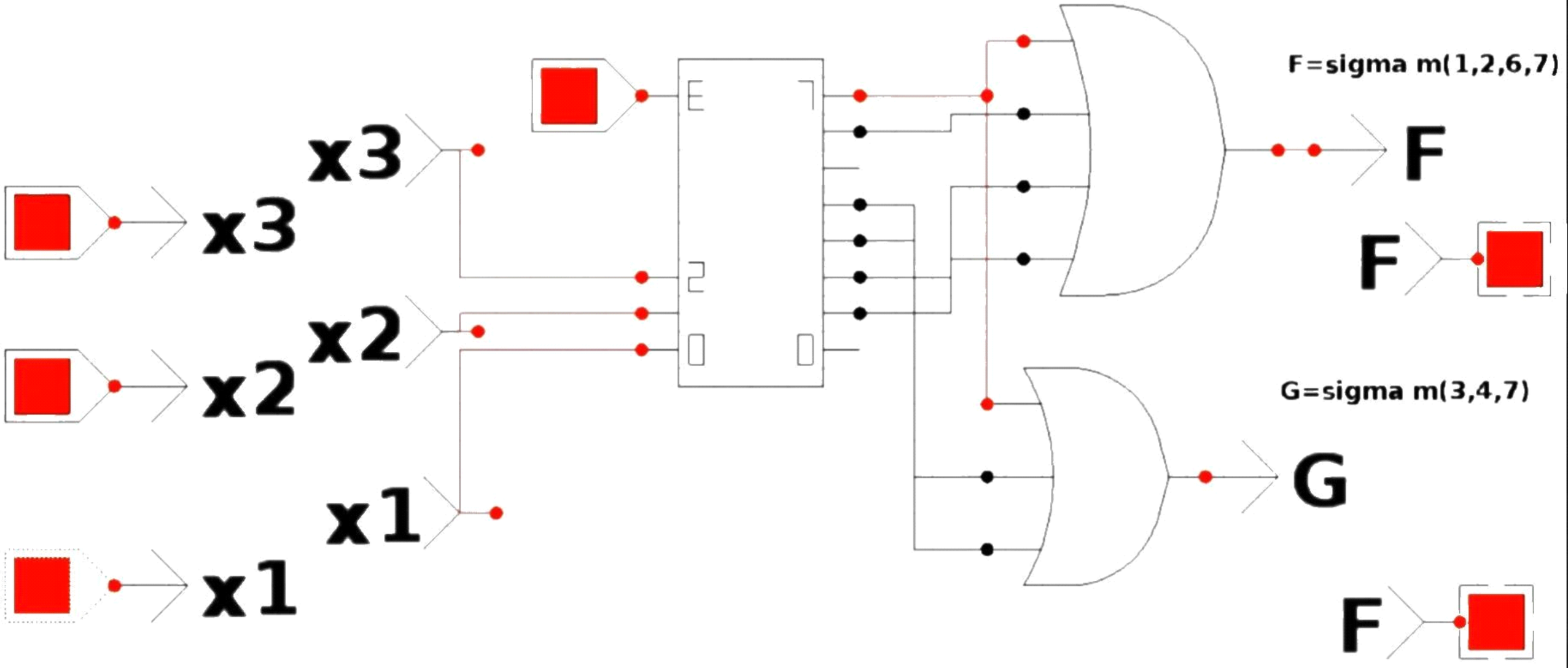
$G(x_1, x_2, x_3) = \Pi M(0, 1, 3, 5, 6)$

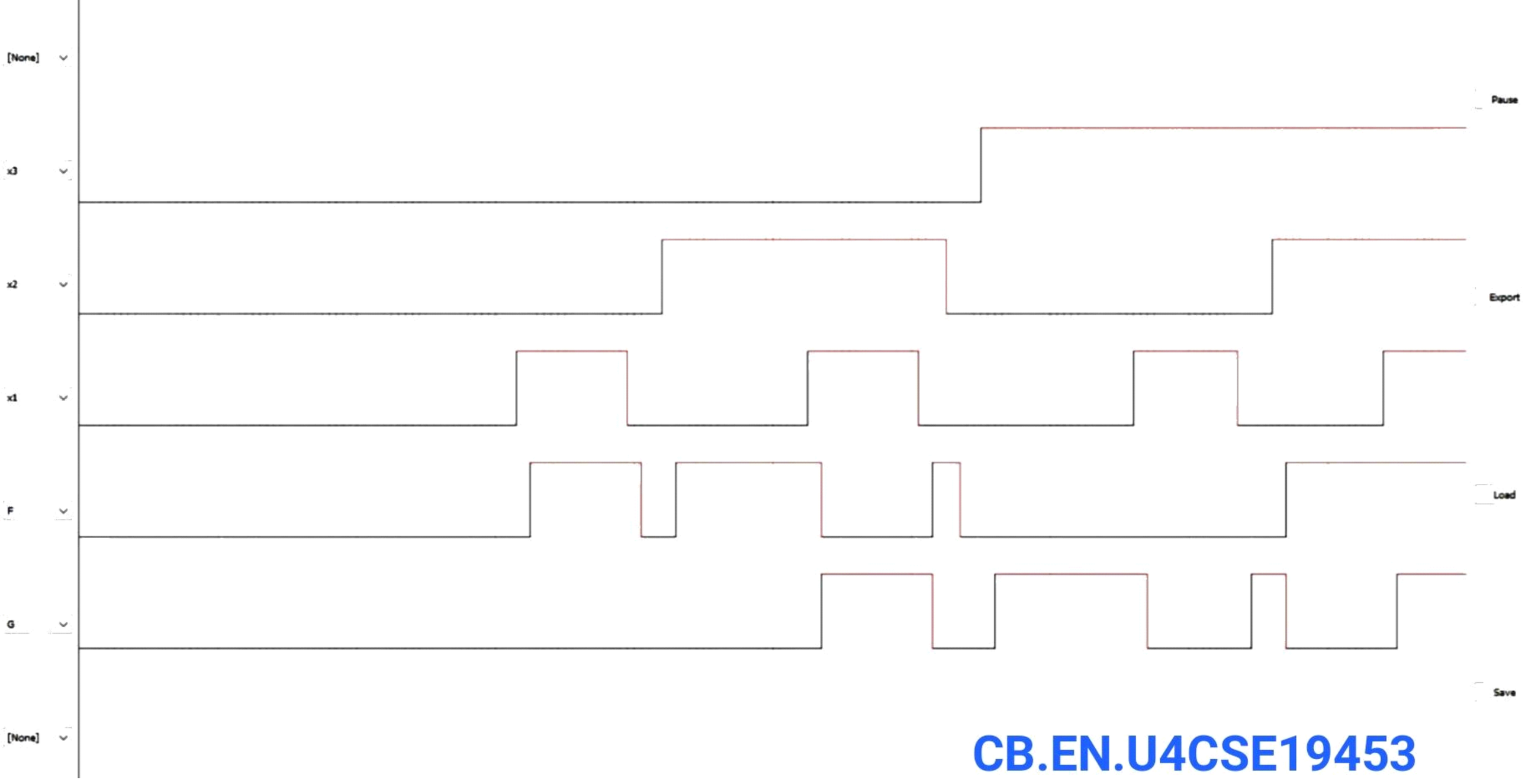
W.K.T.,

$G = \Sigma M(3, 4, 7)$

$\therefore$ SOP is complement of POS




x3
x3
x2
x2
x1
x1
F=sigma m(1,2,6,7)
F
F
G=sigma m(3,4,7)
G
F



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Characteristic Table :-

	y_1	y_0
Coffee	0	0
Tea	0	1
Milk	1	0
Coca-cola	1	1

a	b	c	d	e	f	g
1	0	0	1	1	1	0
0	0	0	0	1	1	1
0	0	0	1	1	1	0
1	1	1	0	1	1	1

Algebraic - equation for each output terminal :-

$$a = \bar{y}_1 y_0 + y_1 y_0 = y_1 \odot y_0$$

$$b = y_1 y_0$$

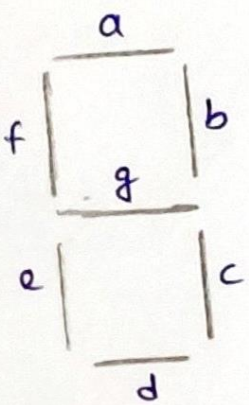
$$c = y_1 y_0$$

$$d = \bar{y}_1 \bar{y}_0 + y_1 \bar{y}_0 + \bar{y}_1 y_0 = \bar{y}_0 + \bar{y}_1$$

$$e = 1$$

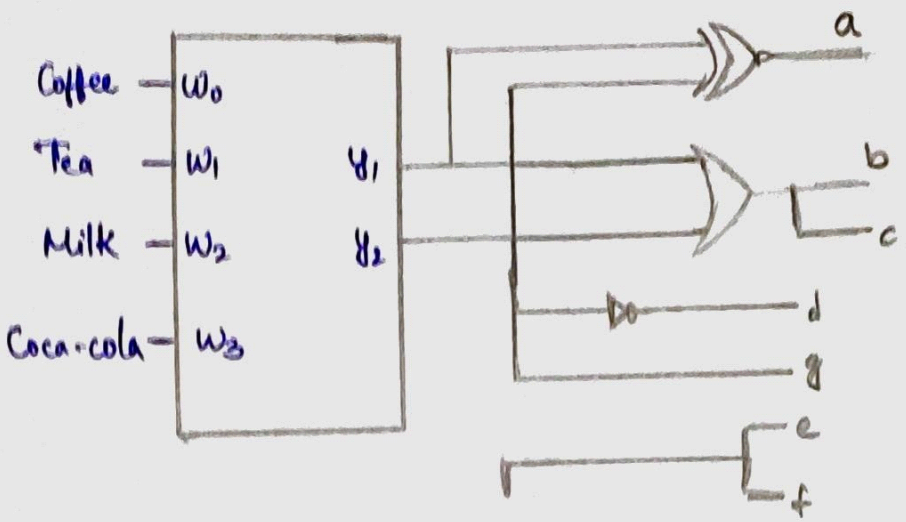
$$g = \bar{y}_1 y_0 + y_1 y_0 = y_0$$

$$f = 1$$



Circuit :

encoder 4 : 2

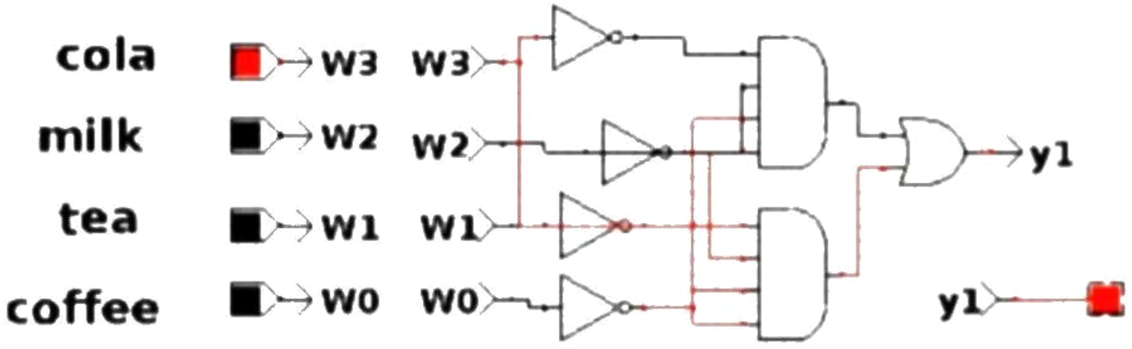


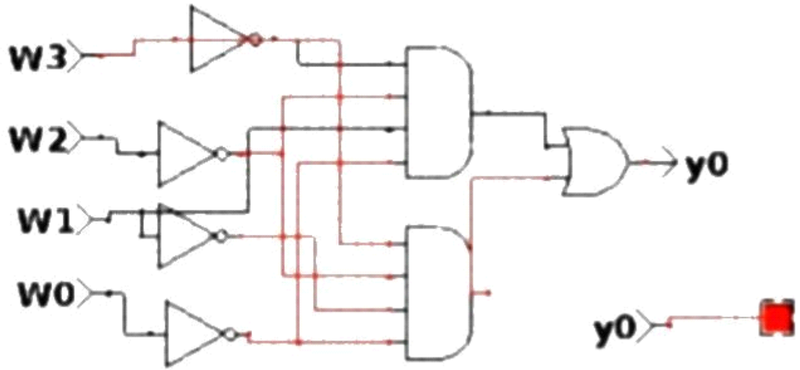
Building encoder :

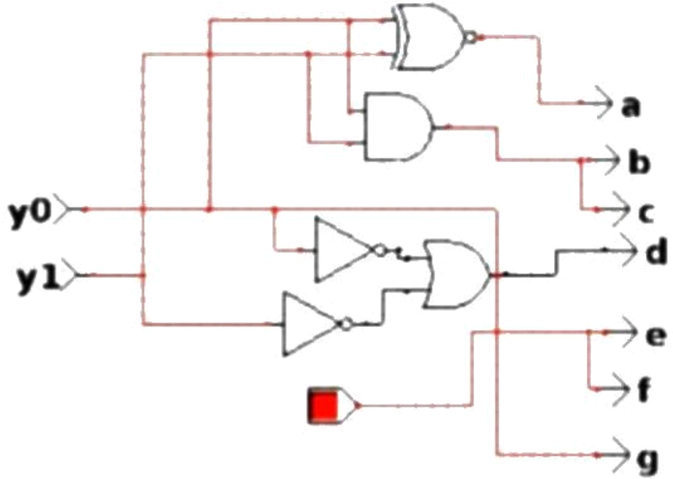
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

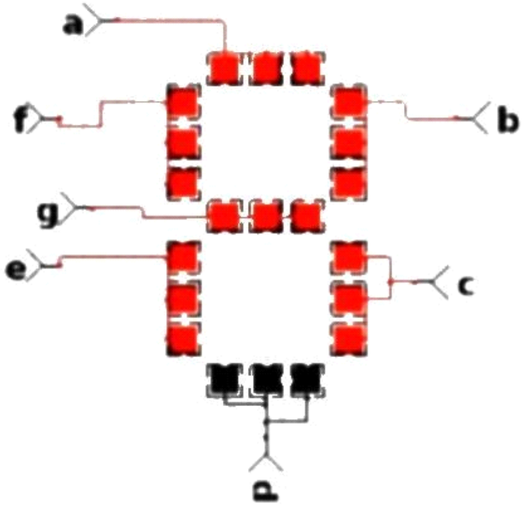
$$y_1 = \bar{w}_3 w_2 \bar{w}_1 \bar{w}_0 + w_3 \bar{w}_2 \bar{w}_1 \bar{w}_0$$

$$y_0 = \bar{w}_3 \bar{w}_2 w_1 \bar{w}_0 + w_3 \bar{w}_2 \bar{w}_1 \bar{w}_0$$









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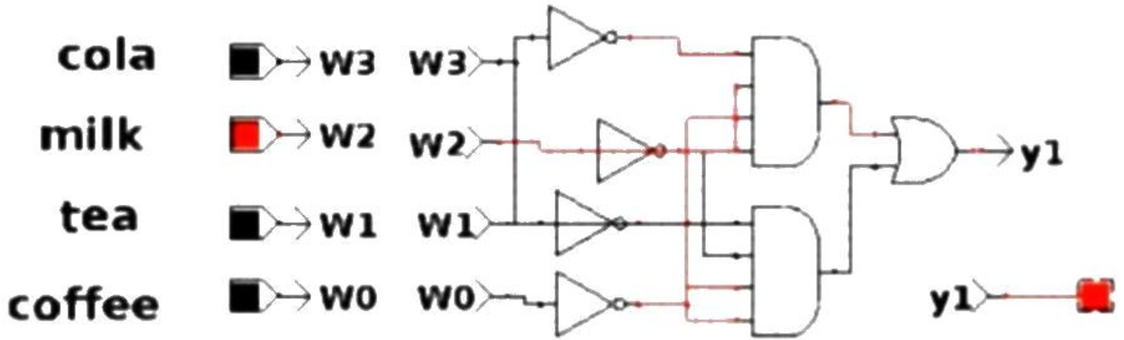

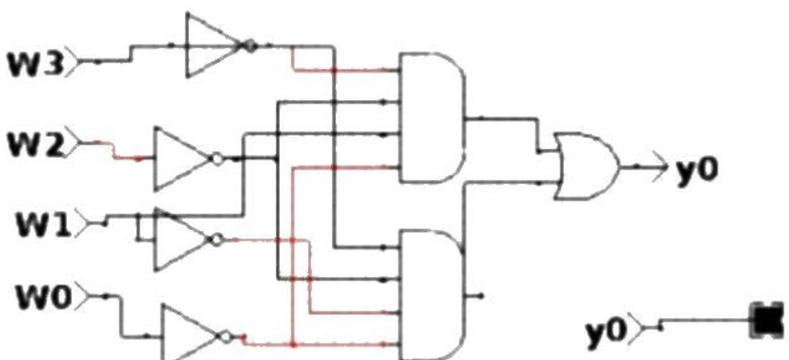

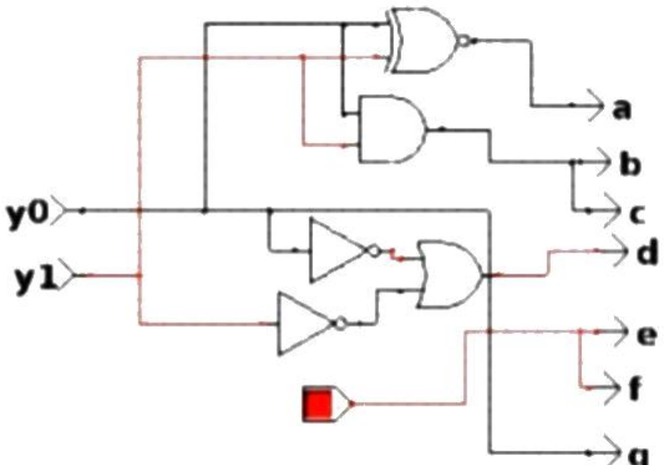

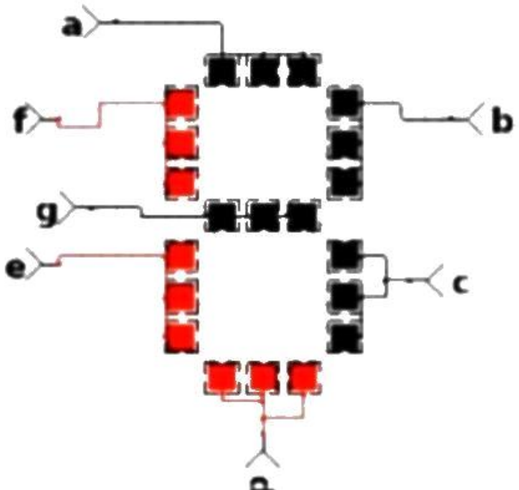

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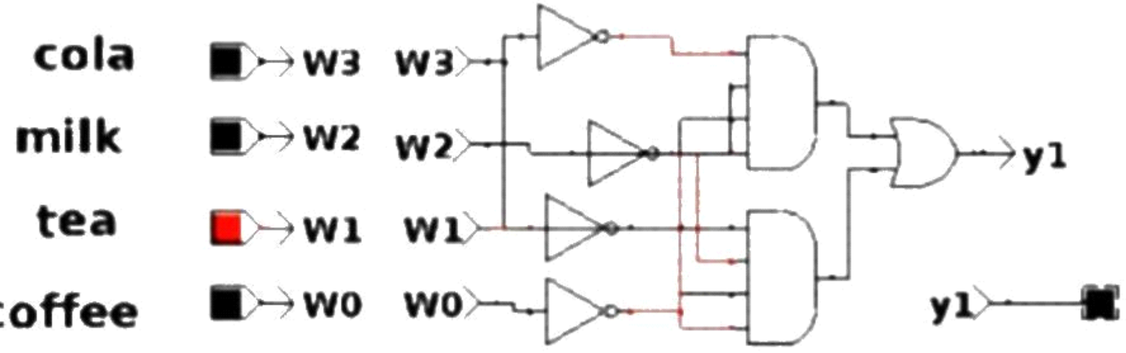

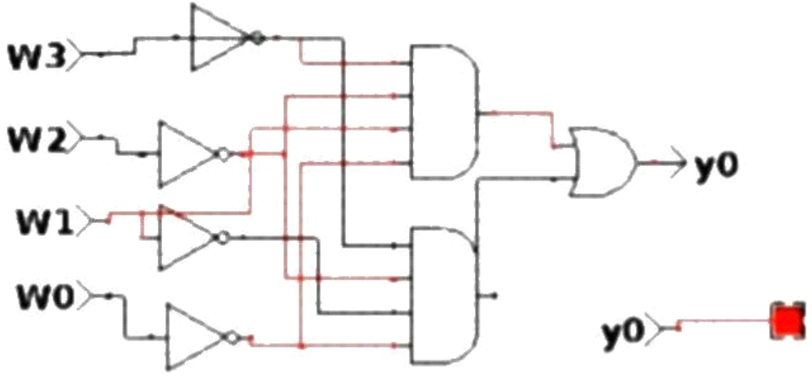

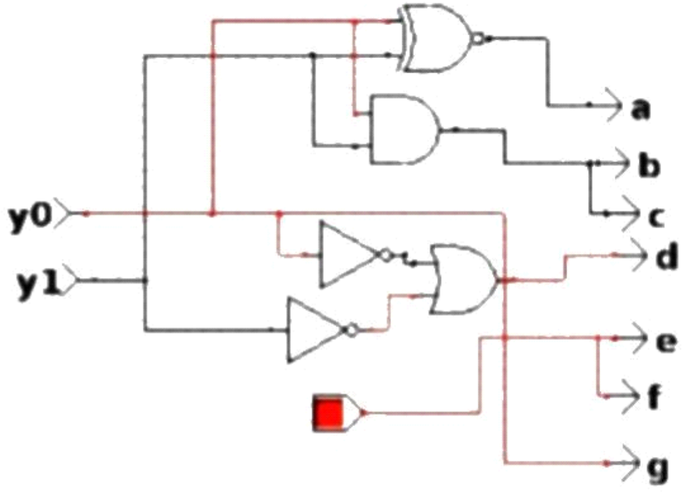

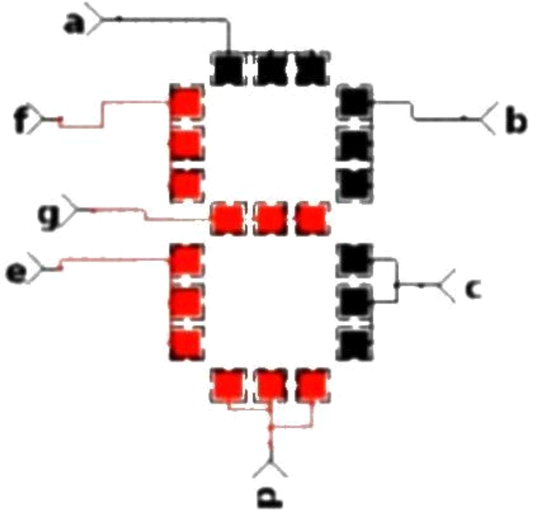

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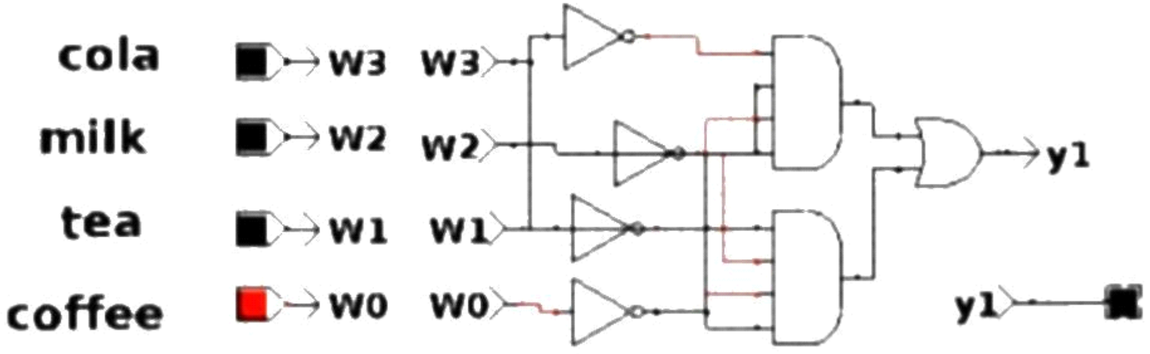

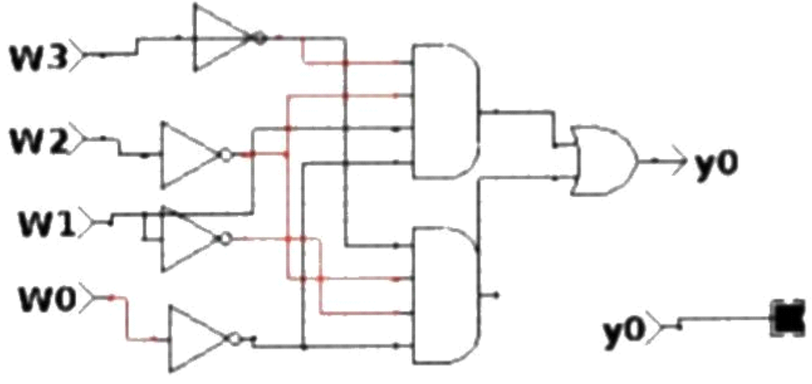

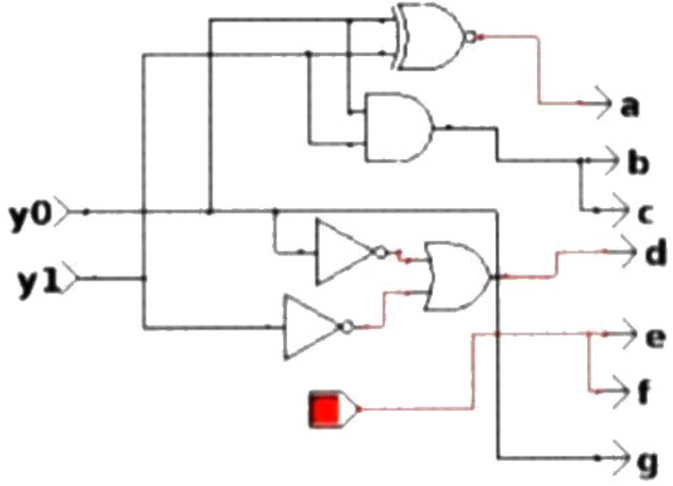

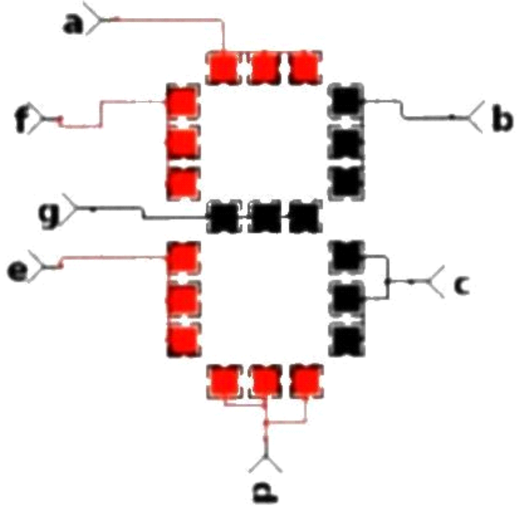

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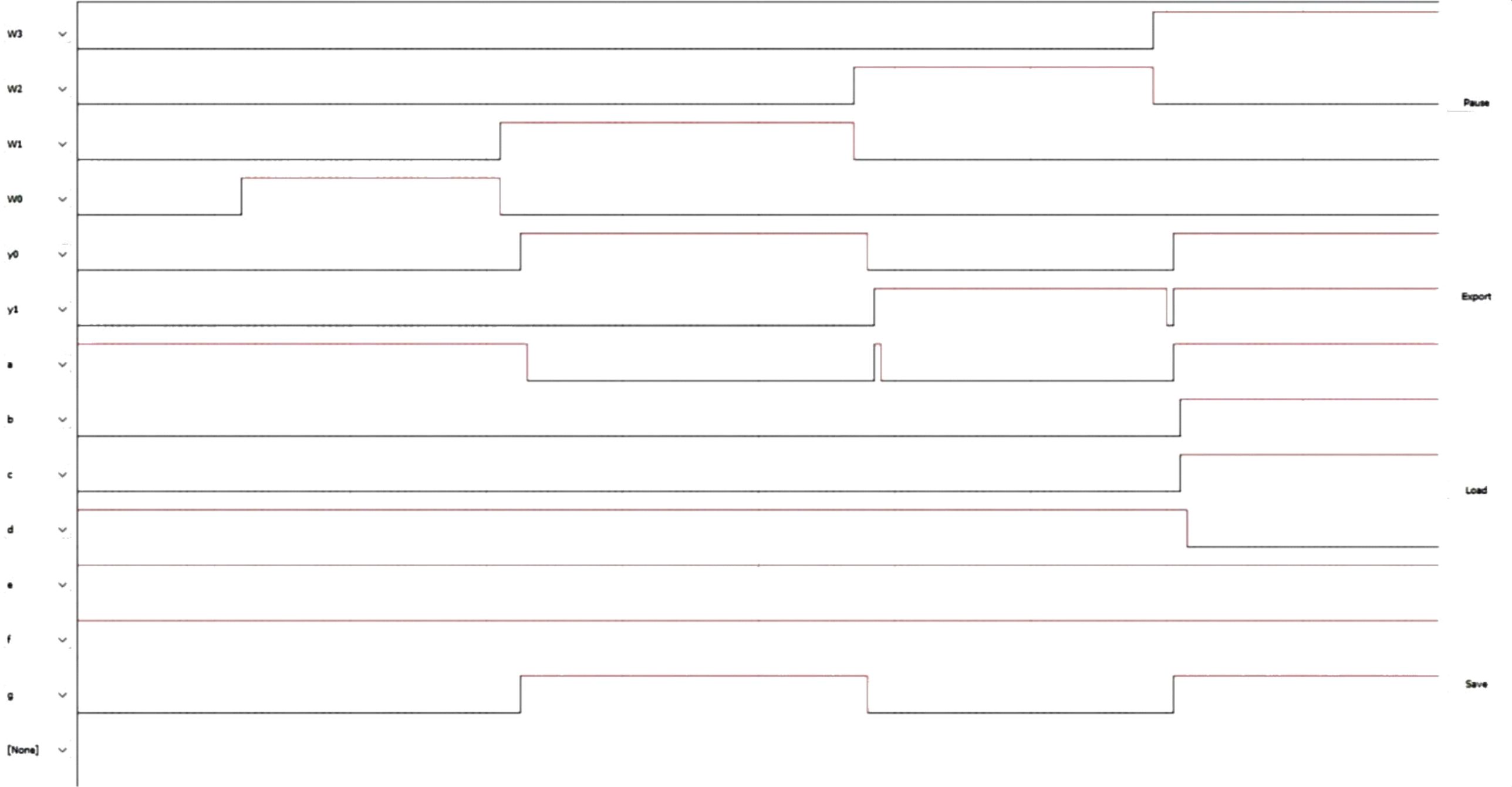
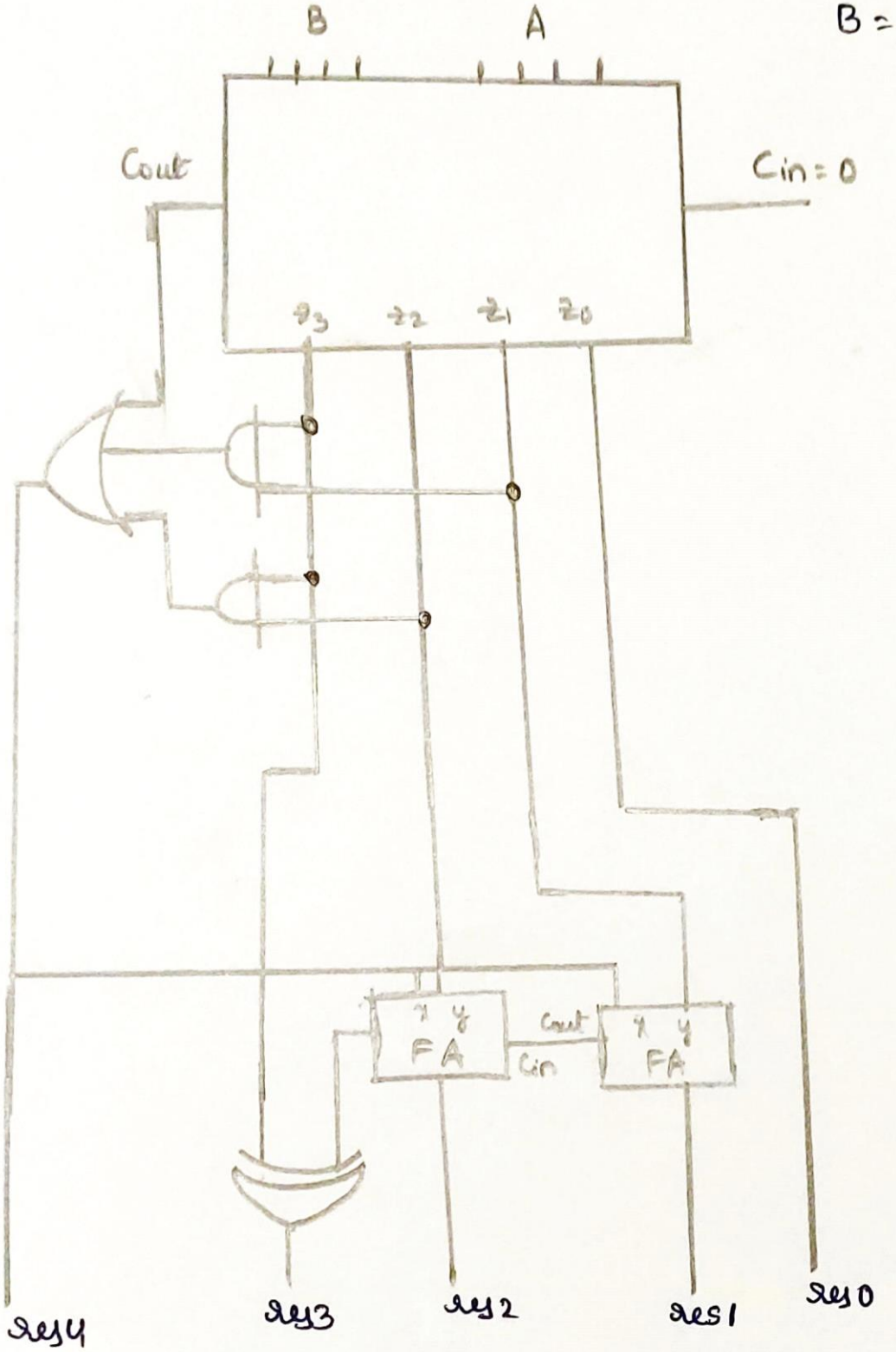

W3
W2
W1
W0
y0
y1
a
b
c
d
e
f
g
[None]
Pause
Export
Load
Save

4.) Designing 1 digit BCD adder

$A = a_3\ a_2\ a_1\ a_0$

$B = b_3\ b_2\ b_1\ b_0$



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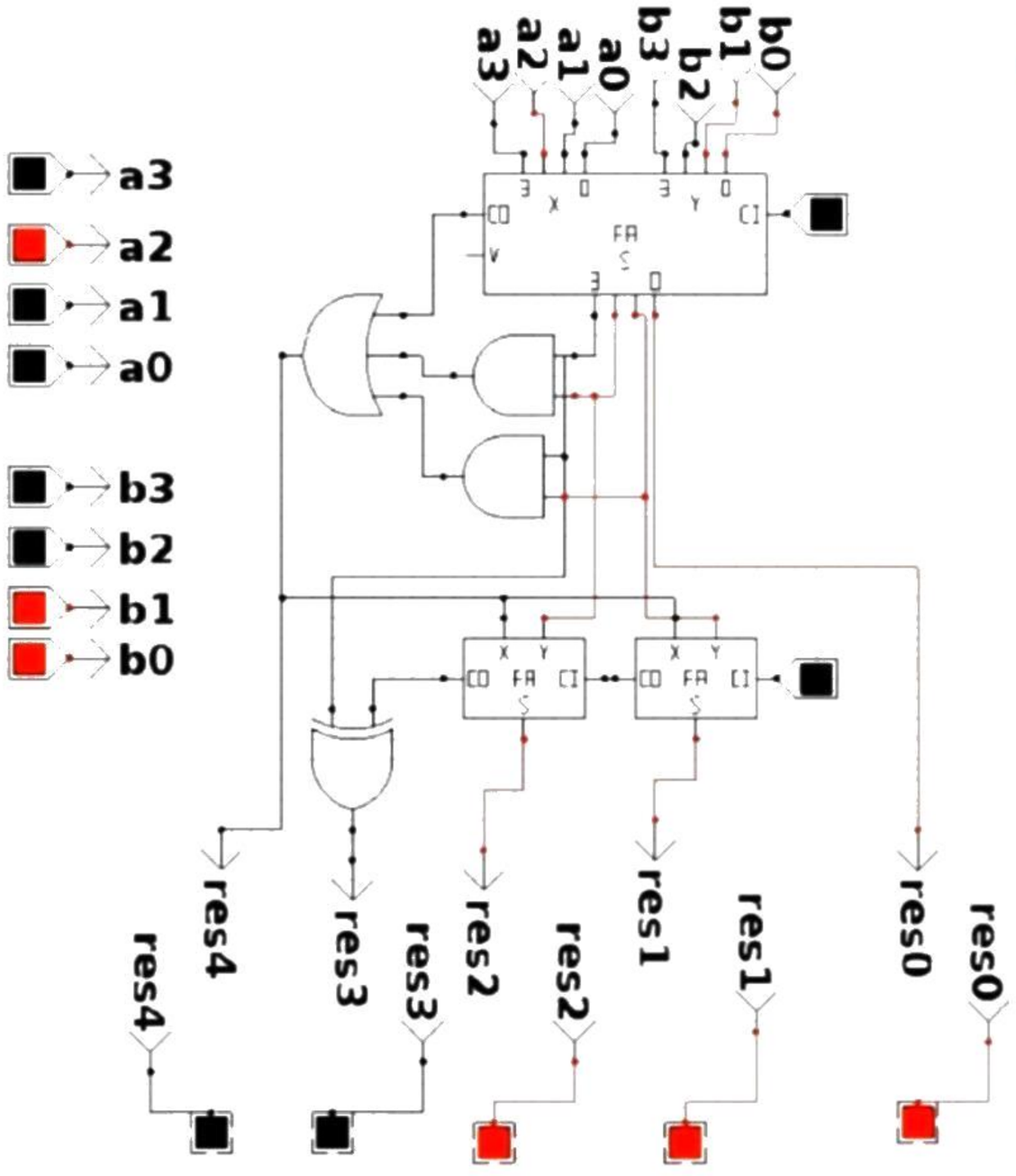
A=4

B=3

res=0 0111



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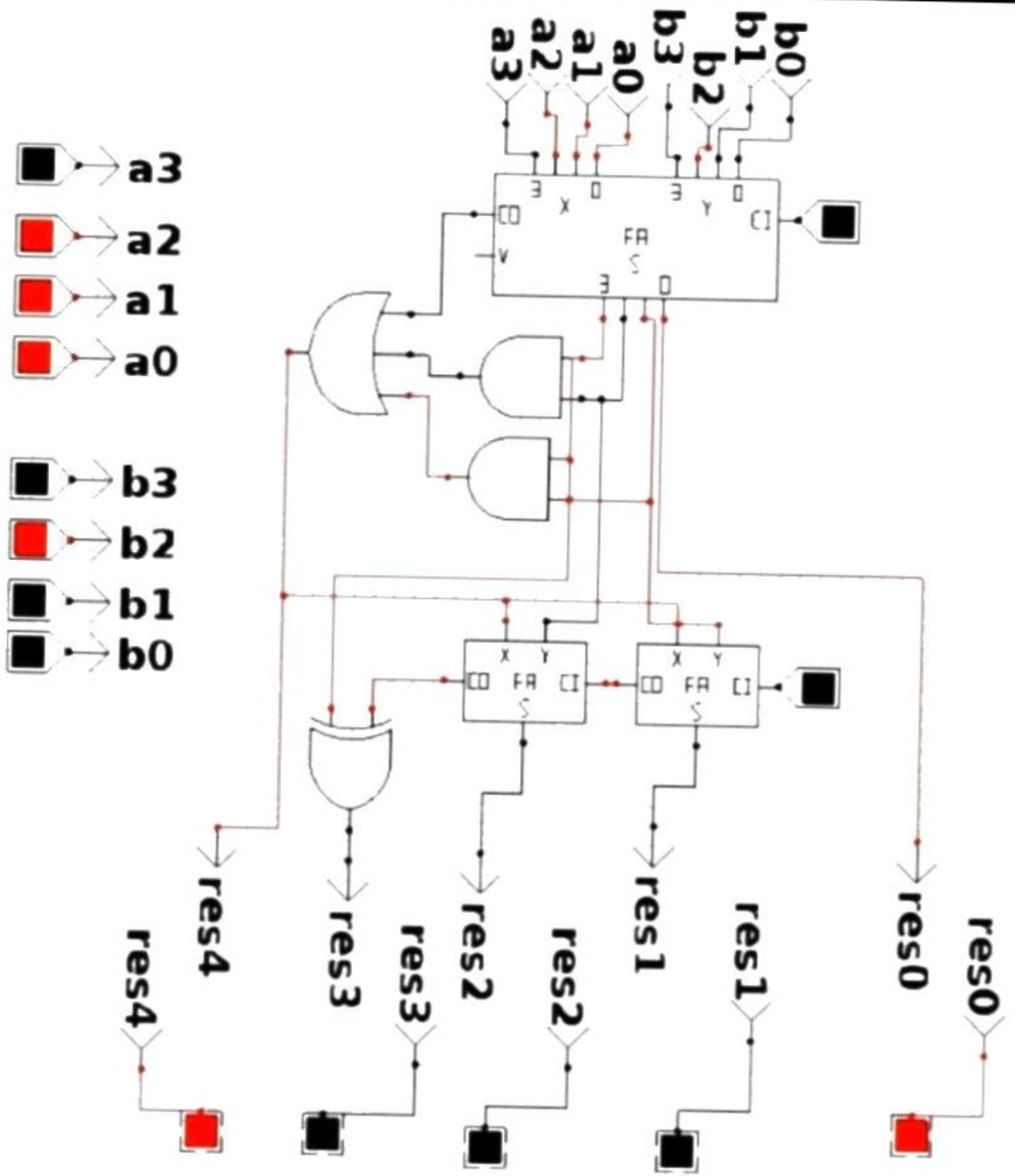
A=7

B=4

res=1 0001



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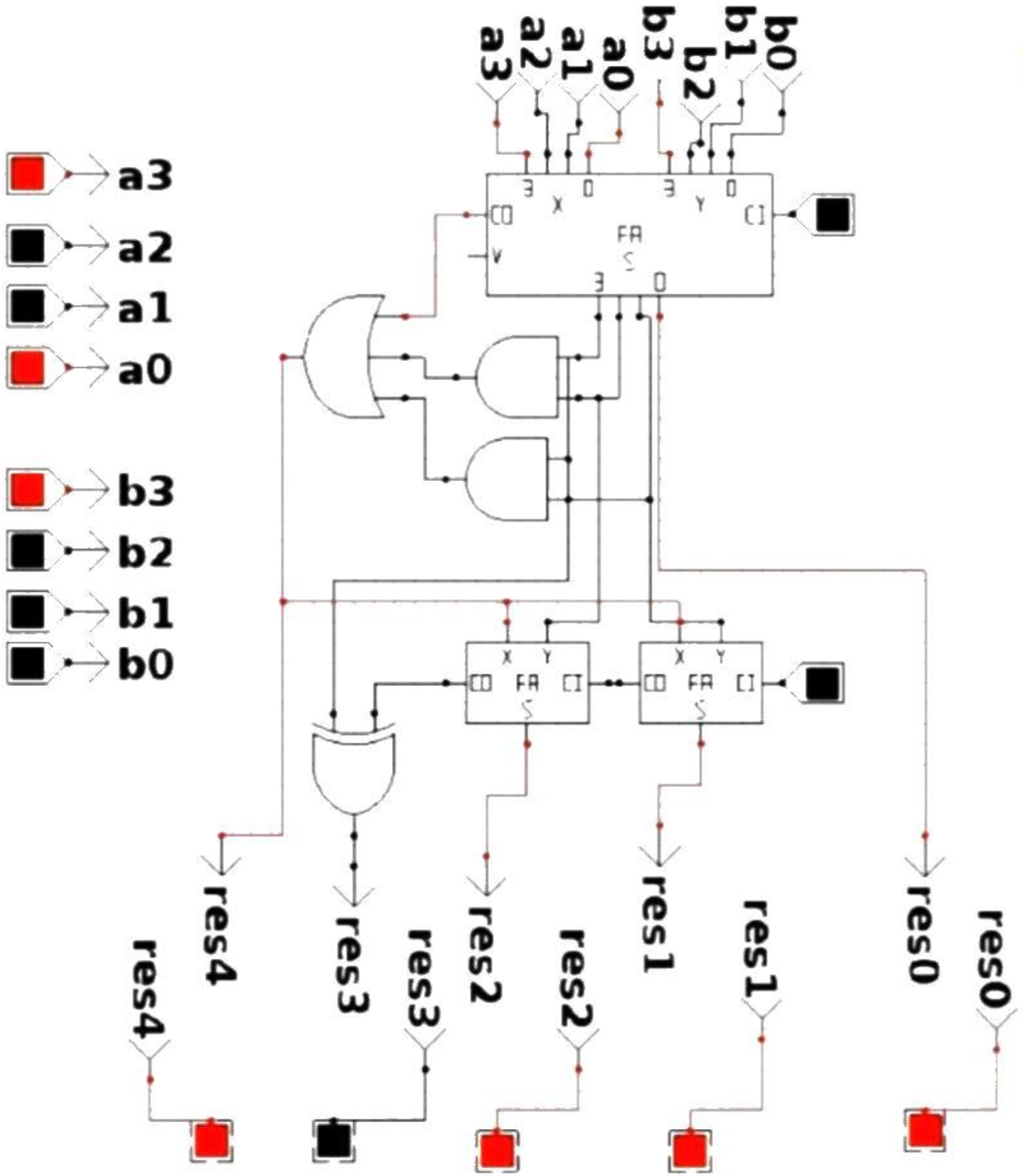
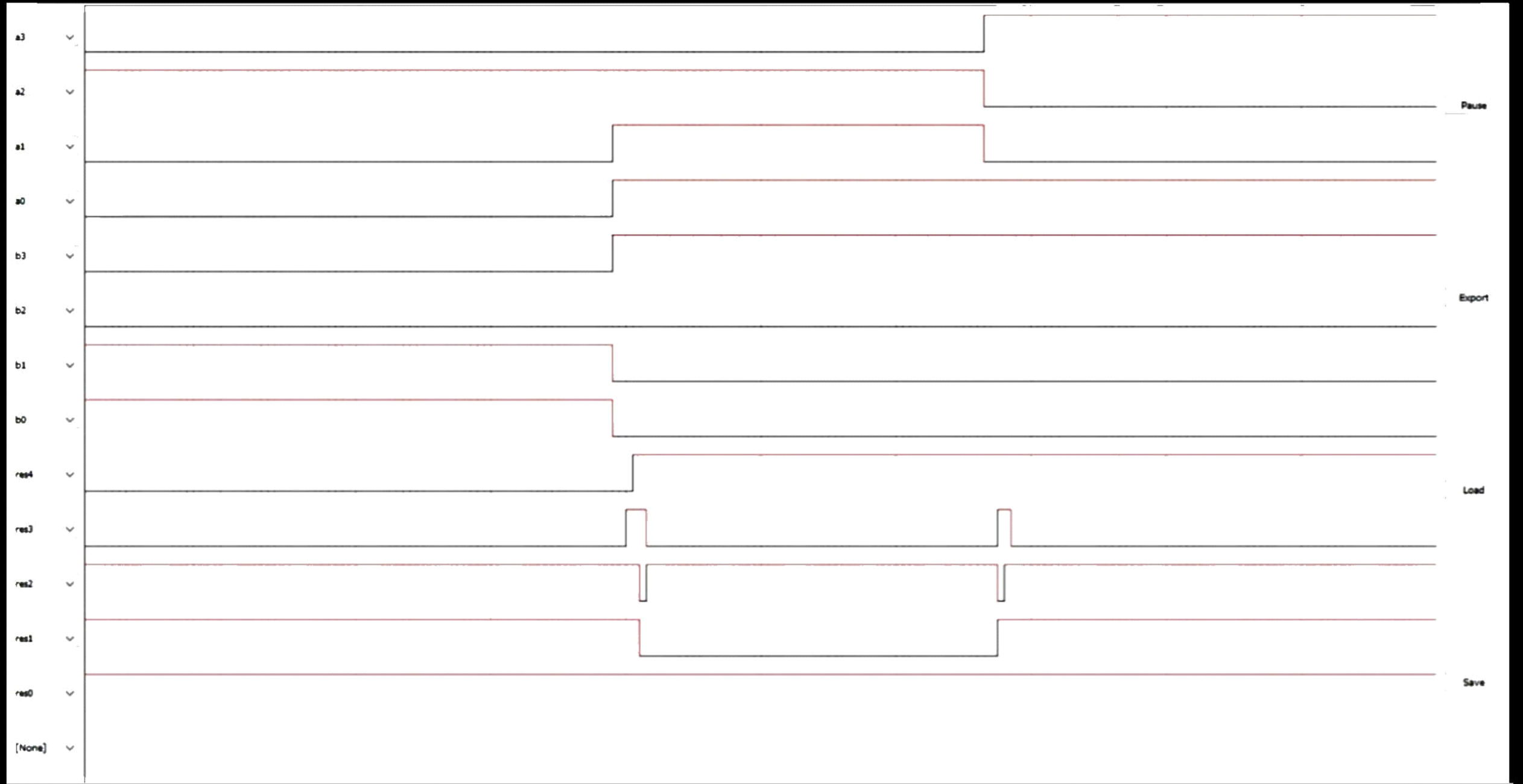
A=9

B=8

res=1 0111

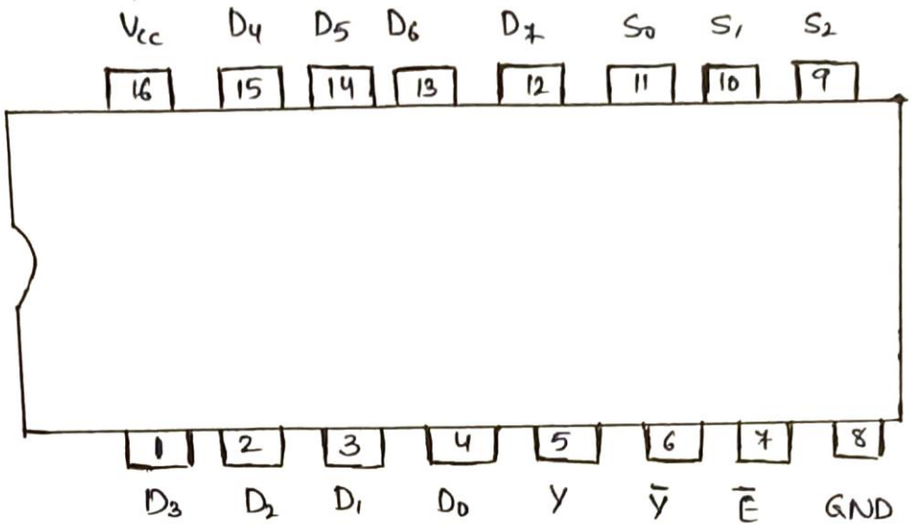



a3
a2
a1
a0
b3
b2
b1
b0
res4
res3
res2
res1
res0
[None]
Pause
Export
Load
Save

5)

(a) 74151 8:1 MUX

(i) Pin Diagram:-



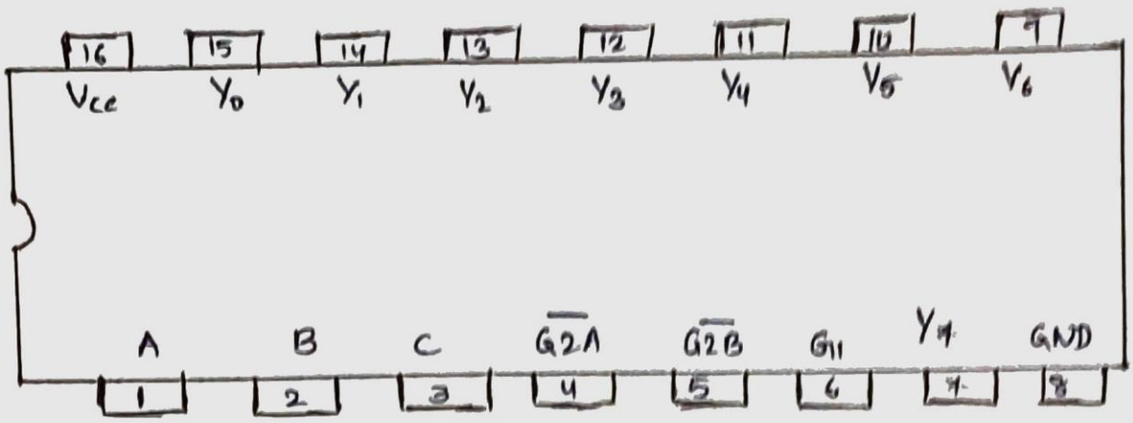
Function Table:-

Enable	Select Input			Output
E	S_2	S_1	S_0	Y
0	x	x	x	0
1	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7

5)

(b) 74138 IC 3:8 decoder

Pin diagram:



Observe in truth table I/p → active high

o/p → active low

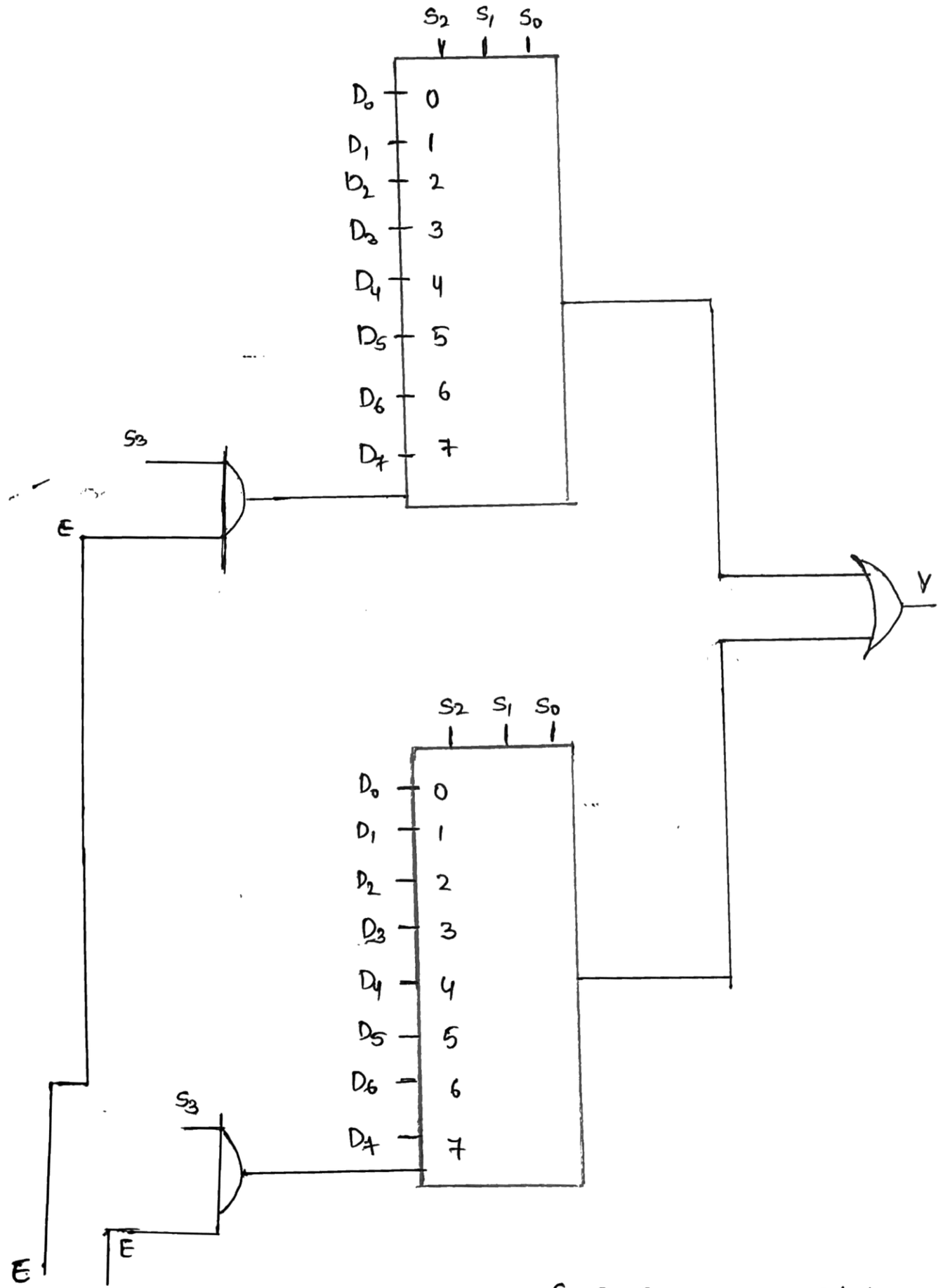
Function Table:

G1	$\overline{G2A}+\overline{G_2B}$		C	B	A		$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
0	X		X	X	X		1	1	1	1	1	1	1	1
X	1		X	X	X		1	1	1	1	1	1	1	1
1	0		0	0	0		0	1	1	1	1	1	1	1
1	0		0	0	1		1	0	1	1	1	1	1	1
1	0		0	1	0		1	1	0	1	1	1	1	1
1	0		0	1	1		1	1	1	0	1	1	1	1
1	0		1	0	0		1	1	1	1	0	1	1	1
1	0		1	0	1		1	1	1	1	1	0	1	1
1	0		1	1	0		1	1	1	1	1	1	0	1
1	0		1	1	1		1	1	1	1	1	1	1	0

$\overline{G2A} + \overline{G2B} = G2$

$\overline{G2A} + \overline{G2B} = G2$

(ii) We can take the help of enable (E) to connect two 8:1 MUX to yield one 16:1 MUX as follows:



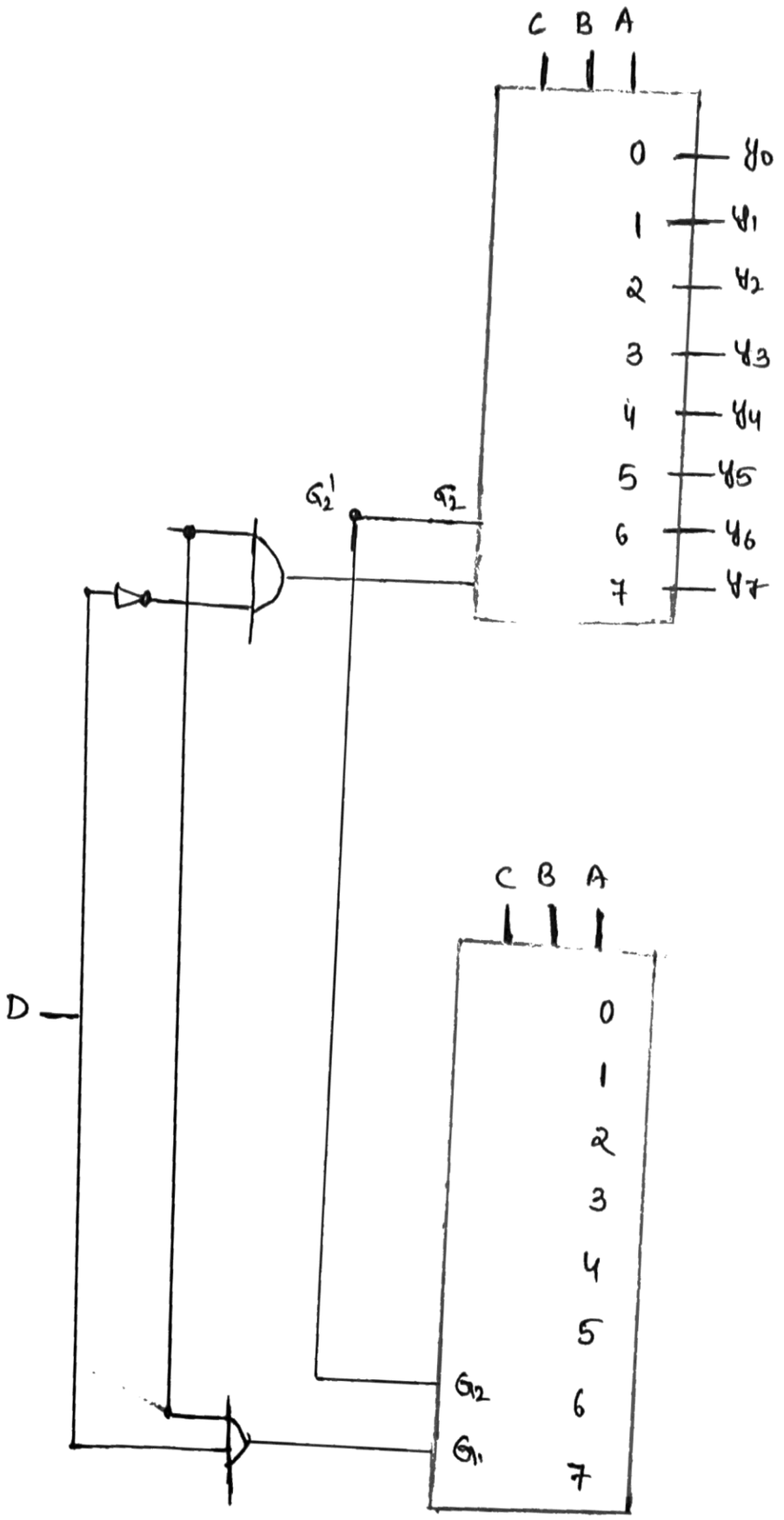
(enable of 16:1 MUX)

S_0, S_3, S_2, S_1 are select inputs of 16:1 MUX

E is enable and

Y is output of 16:1 MUX

(iii) Realizing 4:16 decoder using two 74138 ICs



Hence A, B, C, D are address lines & Y_{is} $0 \leq i \leq 15$ are output terminals of 4:16 decoder.

G_1' is main enable which can be used.