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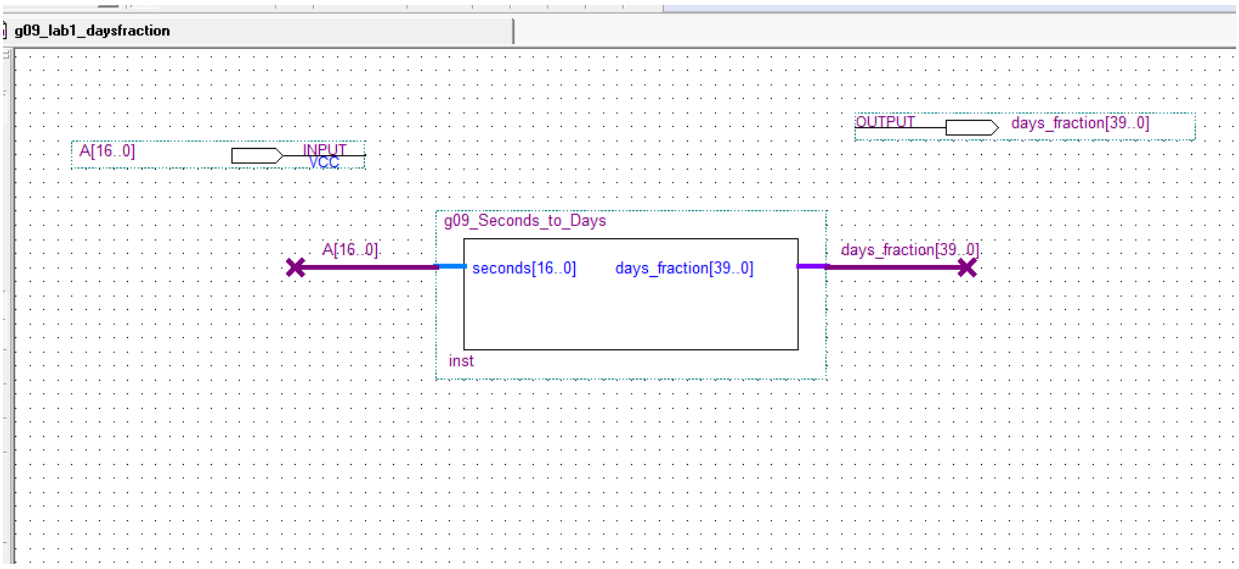
Lab Report 1

In this lab, we designed a 7-bit comparator and seconds-to-days fraction circuits. The latter circuit converts a certain time of day in seconds (N) to a day fraction representation by using the formula d = N/86400.

Input = ‘seconds’ 17-bit (unsigned)

Output = ‘days_fraction’ 40-bit (unsigned)

Symbol diagram:



The above block diagram has been generated using VHDL code. We used 9 adder and 9 shift operators to implement the seconds-to-days fraction circuit. The VHDL description of the circuit is attached.

The 40-bit output was obtained using d ≈ (N*2^23 + N*2^22 + N*2^17 + N*2^13 + N*2^11 + N*2^10 + N*2^9 + N*2^6 + N*2^2 + N).

The figure below shows the hand-written version of the block diagram that was implemented using VHDL code. The 17-bit input passes through 9 shift and 9 adder operators to give a 40-bit output.

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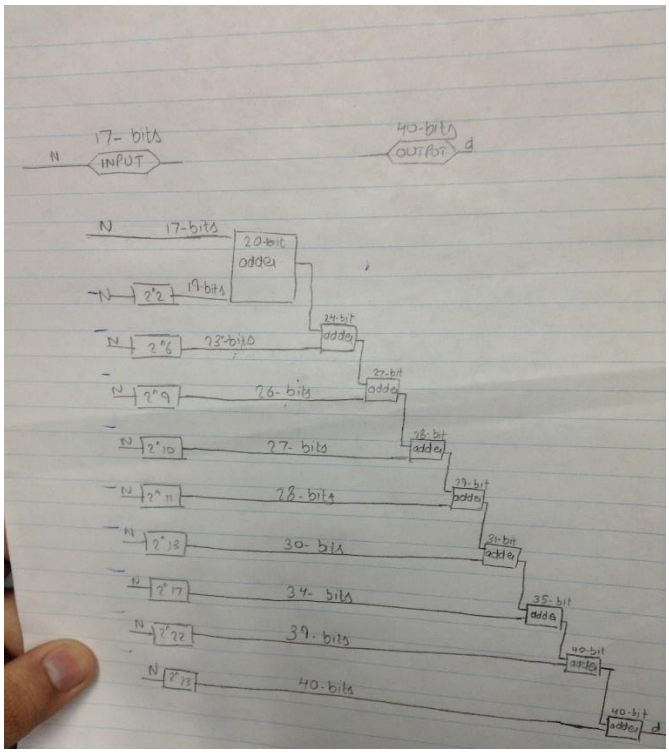


We tested the circuit by running the simulation for 8 different test cases including the two boundary cases. The boundary cases refer to the minimum (0s) and maximum (86400s) values that can be placed as inputs. All 8 input test cases were manually calculated for the ideal day_fraction values and then compared to the outputs generated in the vector waveform file. An example can be seen in the wolframalpha screenshot below for N = 8. The outputs obtained from simulation were equal to the ones obtained through manual calculation. The circuit gave no erroneous results and thus we can conclude that the block diagram designed is accurate.

A screenshot of the simulation for all 8 test cases is attached below:

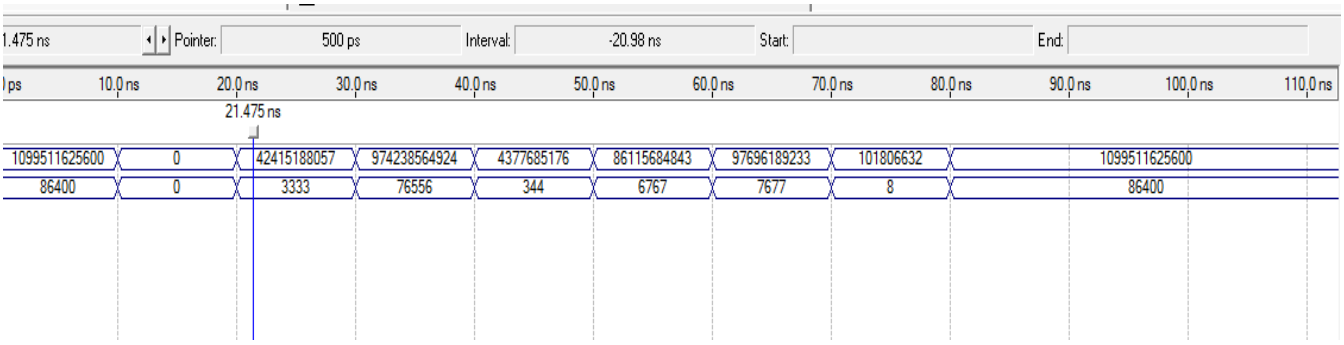
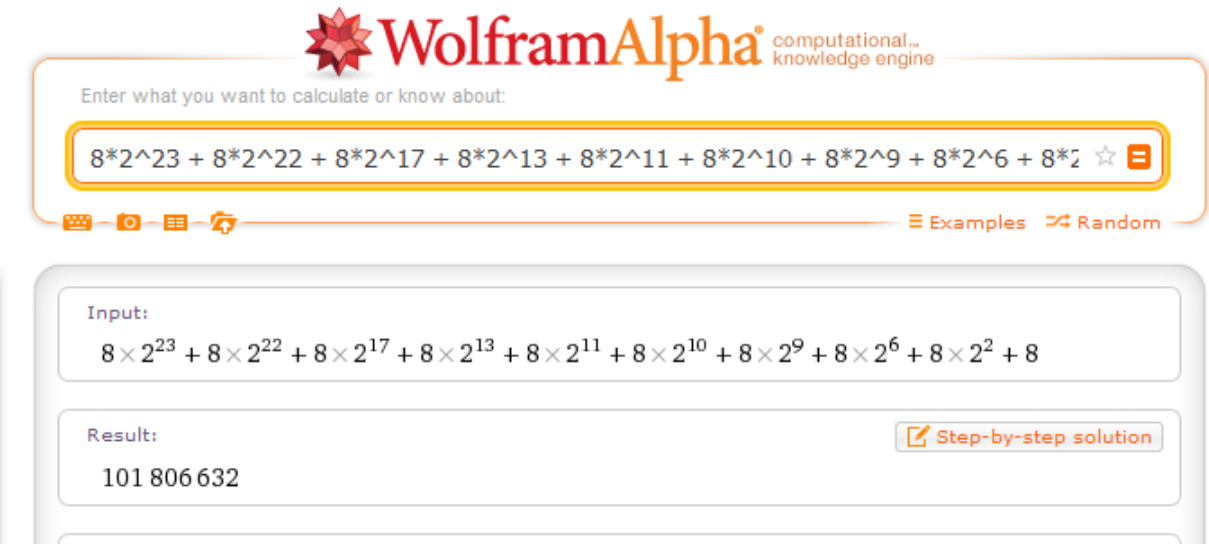
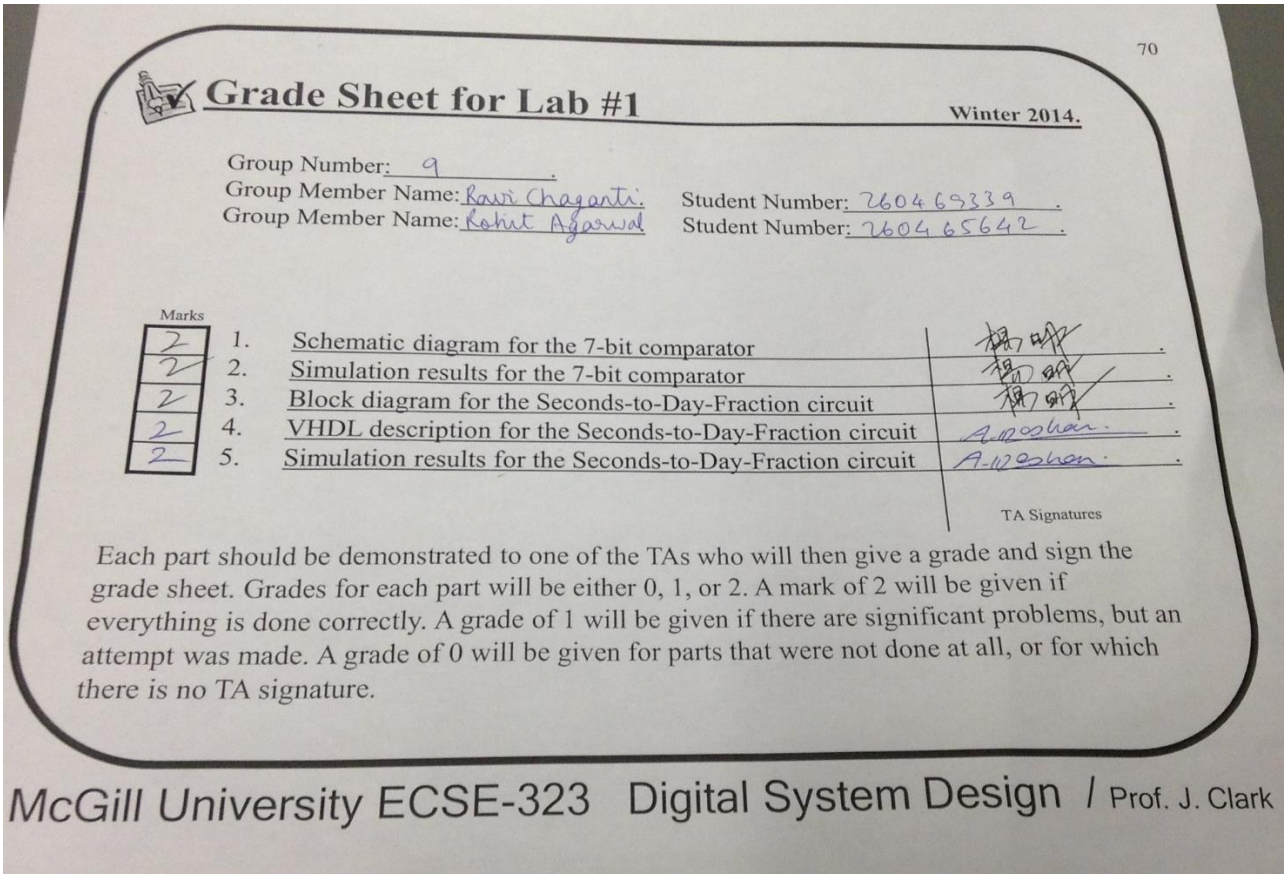


Figure 1: Simulation for 8 test cases



Grade-sheet:



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Grade Sheet for Lab #1 Winter 2014.

Group Number: 9
Group Member Name: Ravi Chaganti. Student Number: 260469339
Group Member Name: Rohit Agarwal Student Number: 260465642

Marks			TA Signatures
2	1.	Schematic diagram for the 7-bit comparator	
2	2.	Simulation results for the 7-bit comparator	
2	3.	Block diagram for the Seconds-to-Day-Fraction circuit	
2	4.	VHDL description for the Seconds-to-Day-Fraction circuit	A. Aroshan.
2	5.	Simulation results for the Seconds-to-Day-Fraction circuit	A. Aroshan.

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.

McGill University ECSE-323 Digital System Design / Prof. J. Clark