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## g09\_Binary\_to\_BCD

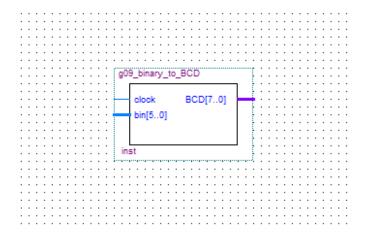
Convert binary input to a Binary Coded Decimal Output

In this lab, we created a circuit that converts a 6 bit binary value to its 2 digit binary-coded-decimal (BCD) representation. For example, the BCD representation of the binary value 110101, a 6 bit unsigned signal (which is 53), is 0101 0011, which is an 8 bit std\_logic\_vector.

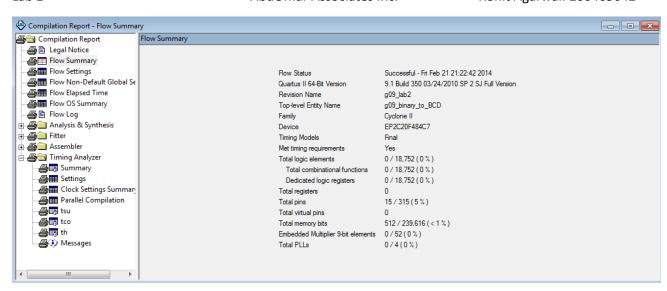
We used a lookup table (LUT) to get a memory unit that has an entry for every possible input pattern. We implemented lpm\_rom component by using its component instantiation statement. After that we created a .mif file (memory initialization file) to specify the contents of the LUT. We stored the values from 0 to 63 as seen in the figure below.

Addr	+0	+1	+2	+3	+4	+5	+6	+7
0	00	01	02	03	04	05	06	07
8	08	09	10	11	12	13	14	15
16	16	17	18	19	20	21	22	23
24	24	25	26	27	28	29	30	31
32	32	33	34	35	36	37	38	39
40	40	41	42	43	44	45	46	47
48	48	49	50	51	52	53	54	55
56	56	57	58	59	60	61	62	63

After that, we created the vhdl file to describe the functions of this converter and made a symbol as seen below:



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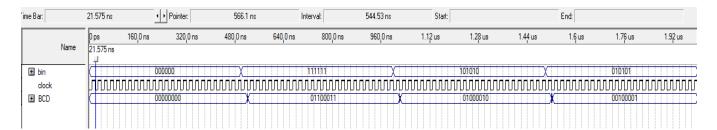


As seen in the compilation report, the number of logic elements used are 0.

T	Timing Analyzer Summary												
	Ty	уре		Required Time	Actual Time	From	То	From Clock		Failed Paths			
1	٧	Vorst-case tsu	N/A	None	4.319 ns	bin[0]	lpm_rom:crc_rom altrom:srom altsyncram:rom_block altsyncram_qs01:auto_gener		clock	0			
, 2	2 1	Vorst-case too	N/A	None	11.825 ns	lpm_rom:crc_rom altrom:srom altsyncr	BCD[3]	clock		0			
3	V	Vorst-case th	N/A	None	-3.558 ns	bin[4]	lpm_rom:crc_rom altrom:srom altsyncram:rom_block altsyncram_qs01:auto_gener		clock	0			
4	T	otal number of failed paths								0			

As seen above, the largest propagation delay is the worst-case tco which is 11.825ns.

We generated two vector waveform files for functional and timing analysis. We used 4 values as test cases: 000000, 111111, 101010, 010101. Please see the timing vector waveform for the results.



As we can see above, the settling time is not the same for every transition. It increases compared to the propagation delay reported by the timing analyzer.