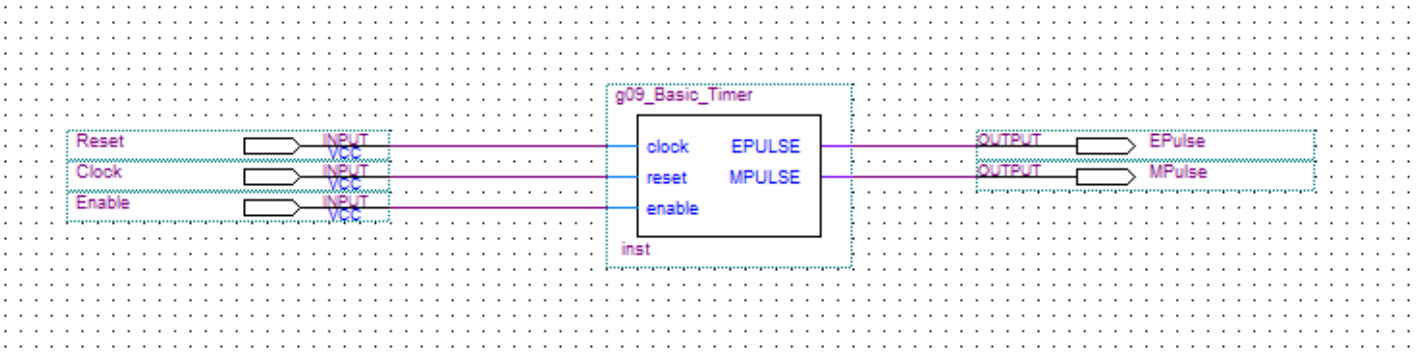
G09_Basic_Timer

Circuit generates the pulse that drives both Earth and Mars clocks

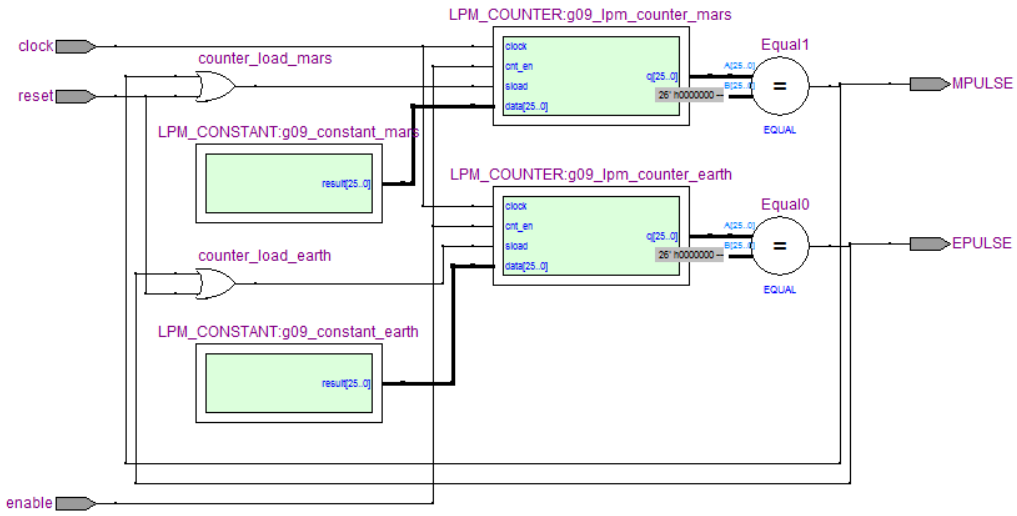
The circuit is a Frequency Divider circuit, which generates one pulse each second. This is done by using a counter that counts down to zero, and as the counter hits zero, the pulse output goes high for one clock period. The circuit also generates pulses for the Mars clock, where 1 Martian second = 1.027 seconds on Earth. It was calculated using the formula: (24*3600+39*60+35.244)/(24*3600).

Inputs: Reset, Clock, Enable

Outputs: EPulse, MPulse



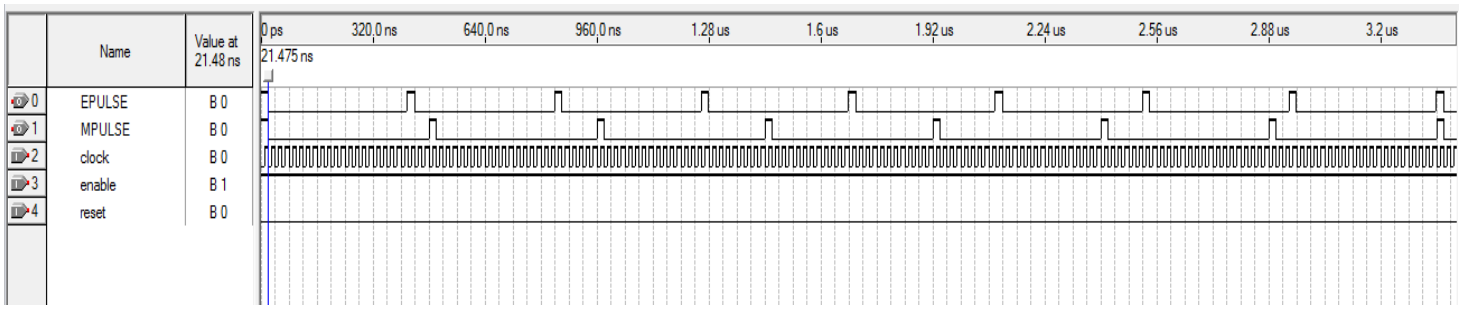
Pinout Diagram



Schematic Diagram

For testing the circuit, we bring down the division ratio and run the simulation for only 100 usec to speed up the simulation. We performed the timing simulation and result obtained is shown below.

Timing Simulation Plot:



As can be seen from the simulation plot, the propagation delay of the EPULSE was around 18.7 ns and the delay for the MPULSE was around 19.5 ns.

Timing Performance Summary:

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time
1	Worst-case tsu	N/A	None	6.525 ns
2	Worst-case tco	N/A	None	11.209 ns
3	Worst-case tpd	N/A	None	2.810 ns
4	Worst-case th	N/A	None	1.566 ns
5	Clock Setup: 'altera_internal_jtag~TCKUTAP'	N/A	None	114.44 MHz (period = 8.738 ns)
6	Clock Setup: 'clock'	N/A	None	192.16 MHz (period = 5.204 ns)
7	Total number of failed paths			

FPGA Resource Utilization:

Flow Status	Successful - Fri Mar 21 16:40:57 2014
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g09_Lab3
Top-level Entity Name	g09_Basic_Timer
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	930 / 18,752 (5 %)
Total combinational functions	507 / 18,752 (3 %)
Dedicated logic registers	793 / 18,752 (4 %)
Total registers	793
Total pins	5 / 315 (2 %)
Total virtual pins	0
Total memory bits	4,864 / 239,616 (2 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)