

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY COMPUTER ORGANIZATION

Course Code: GR22A2073 L/T/P/C: 3/0/0/3

II Year II Semester

Course Outcomes:

- 1. Demonstrate knowledge of register organization of a basic computer system
- 2. IncorporateIn-depth understanding of control unit organization and microprogrammed control.
- 3. Understand the performance of central processing unit of a basic computer system.
- 4. Apply various algorithms to perform arithmetic operations and propose suitablehardware and appraise various methods of communications with I/O devices.
- 5. Analyze and emphasize various communication media in the basic computer system using design of various memory structures and Multiprocessor systems.

UNIT I

Basic Structure of Computers: Computer Types, Functional unit, Data Representation, Fixed Point Representation, Floating – Point Representation, Error Detection codes.

Register Transfer Language and Micro operations: Register Transfer language. Register Transfer, Bus and memory transfers, Micro Operations and its types, Arithmetic logic shift unit.

UNIT II

Basic Computer Organization and Design: Instruction codes, Computer Registers, Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt, Complete Computer Description.

Micro Programmed Control: Control memory, Address sequencing, Micro program example, Design of control unit, Micro program Sequencer, Hard wired control Vs Micro programmed control.

UNIT III

Central Processing Unit Organization: General Register Organization, STACK organization. Instruction formats, Addressing modes. DATA Transfer and manipulation, Program control. Reduced Instruction set computer.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Floating – point Arithmetic operations, BCD Adder.

UNIT IV

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt, Direct memory Access, Input –Output Processor (IOP).

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, Dependencies, Vector Processing.

UNIT V

Memory Organization: Memory Hierarchy, Main memory- RAM and ROM chips, Memory Address map, Auxiliary memory – Magnetic Disks, Magnetic Tapes, Associative Memory – Hardware Organization, Match Logic, Cache Memory – Associative mapping, Direct mapping, Set associative mapping, Writing into cache and cache initialization, Cache Coherence, Virtual memory – Address Space and Memory Space, Address mapping using

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pages, Associative Memory page table, Page Replacement.

Multi Processors: Characteristics or Multiprocessors, Interconnection Structures, Cache Coherence, Shared Memory Multiprocessors.

Teaching Methodologies:

- Power Point Presentations
- Tutorial Sheets
- Assignments

Text Books:

- 1. Computer Systems Architecture M.Moris Mano, 3rd Edition, Pearson/PHI
- 2. Computer Organization Carl Hamacher, ZvonksVranesic, SafeaZaky, 5th Edition, McGraw Hill.

References:

- 1. Computer Organization and Architecture William Stallings 7th Edition, Pearson/PHI
- 2. Structured Computer Organization Andrew S. Tanenbaum, 6th Edition PHI/Pearson
- 3. Fundamentals or Computer Organization and Design, SivaraamaDandamudi SpringerInt. Edition.
- 4. Computer Architecture a quantitative approach, John L. Hennessy and David A. Patterson, 5th Edition Elsevier
- 5. Computer Architecture: Fundamentals and principles of Computer Design, Joseph D. Dumas II, BS Publication.