Project Titled:

Design of 256 Bit SRAM Memory Array

REPORT BY:

Group 13

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Abstract: *The aim of this project is to build an 16x16 array of 8-bit SRAM memory cell, using the 65nm CMOS technology. Using a 4-to-8 decoder, the SRAM array is accessed by a 4-bit address. The SRAM cells are designed to achieve lowest power consumption and suitable for working at the maximum possible frequency, while operating at 1.5GHz Read & Write cycles & it works on supply of 880mV (~1V). The test-bench, the implementation, and the layout of the SRAM array and the decoder are done using software simulations through Cadence Virtuoso's Analog-Design Environment (ADE).*

Keywords: *8T SRAM, Precharge, row and column decoder, Layout.*

Aim: To design & implement a low power 256 bit SRAM array and observe read & write operations.

A. Introduction

Semiconductor memories have always been an essential part of any computer storage system. The regular demand for higher storage space with less power and less area has been the driving force for the development in this field, especially in random-access memories (RAMs), since they offer higher read and write speeds than other types of memories, Among the most common RAM types are the static RAMs (SRAMs) and dynamic RAMs (DRAMs). SRAM plays a vital role as it covers a large area in the chip surface and in SoC design because almost 70% of the Cell area is consumed by SRAM memory cells. Over three decades scaling of CMOS technology has been a preliminary issue to the industry which helps in smaller and quicker operation. During these days transistors which are formed are occupying less than 1% of area and are 20% faster than the other chips. In the proposed system, the 8T SRAM architecture is used. The array is made of 256 bits with the help of 8T cells. Even though SRAMs usually require larger area and are more expensive than DRAMs, they are much faster, compatible with CMOS technology, and don't require periodic-refreshing circuits to keep its data while power supply is on.

B. Stages of implementation

The SRAM array consists of 16 rows; each comprises 16 8T-SRAM cells. One SRAM cell represents 1 bit of data that could be read from, or written to. Each bit, or individual SRAM cell, is accessed by 2 complementary bit lines. The SRAM rows are accessed by a word line, which is activated using a 4-to-16 CMOS decoder. The inputs to the decoder are a 4-bit address that chooses which word line to activate, and an enable. The system operates at 1V, in which the Read or Write information is obtained during half of the cycle, and a refresh operation occurs in the second half.

- The first stage of the project is to construct schematic for all separate circuits such as 4 is to 16 decoder, precharge circuit, 8T SRAM cells and write circuit.
- Second, all these circuits is tested through simulation.
- Later the individual circuit layout has been constructed and is verified against DRC and LVS checks.
- In the fourth stage, the overall circuit has been constructed and transient analysis has been observed.
- The next stage is that all the layouts are aligned and verified against DRC and LVS checks.
- In the final stage, the layout is aligned in the pad frame and a test cell generated for final fabrication.

Block Diagram

The Row Decoder works as the 4 bit wwl input for the 256 cell SRAM Array. Similarly, the column decoder operates as 4 bit rwl input. The series of nmos along witrh a simple precharge circuit is used to generate logic 1 for the wbl and wbl_bar lines of all 256 cells. The output is generated at the end of RBL lines as shown in Fig 1.

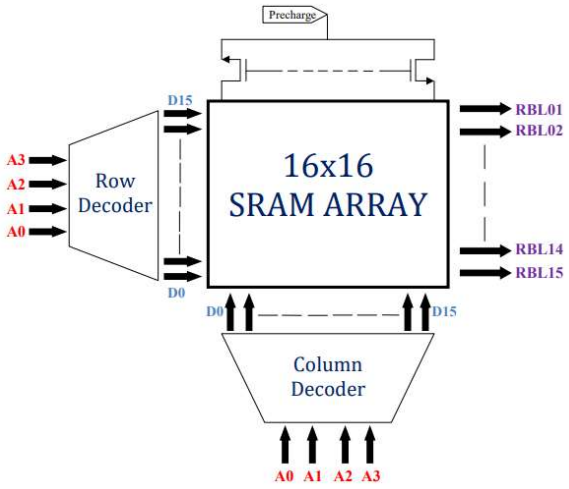


Fig 1. Block Diagram

C. Design components

i. 2 to 4 decoder (with & without enable):

We used hierarchical approach to design 2 to 4 decoder which forms the building block for 4 to 16 row decoder. One 2 to 4 decoder (without enable as shown in fig. 2a) is used to drive four 2 to 4 decoders (with enable as shown in fig. 2b) in the second stage. The decoder consists of AND gate as the latter gives "logic 1" except when all inputs are "logic 1". So in this the output needs to be inverted every time because only one high output is required at a time. A set of two 4 to 16 decoders are used to thrive the inputs of SRAM circuit.

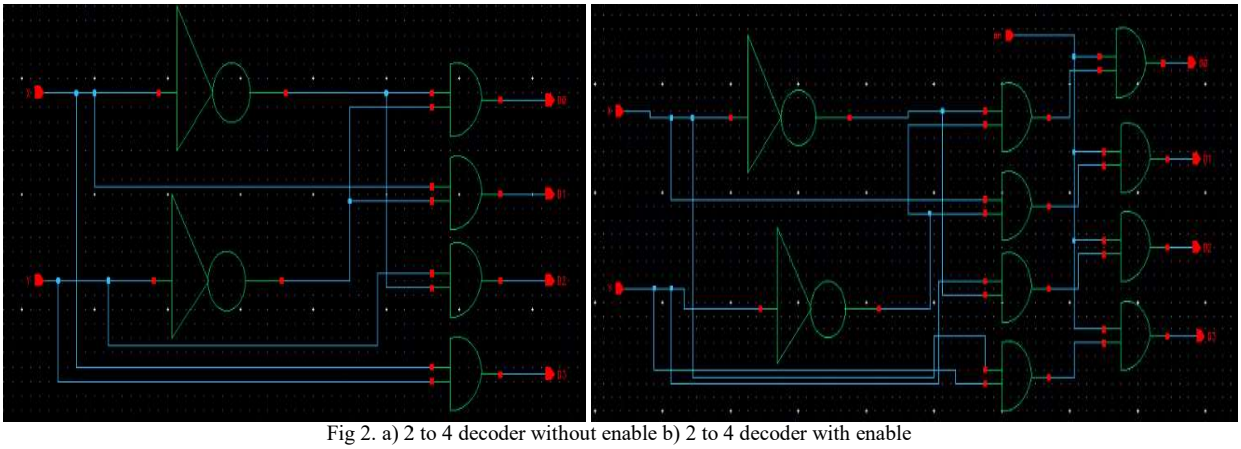


Fig 2. a) 2 to 4 decoder without enable b) 2 to 4 decoder with enable

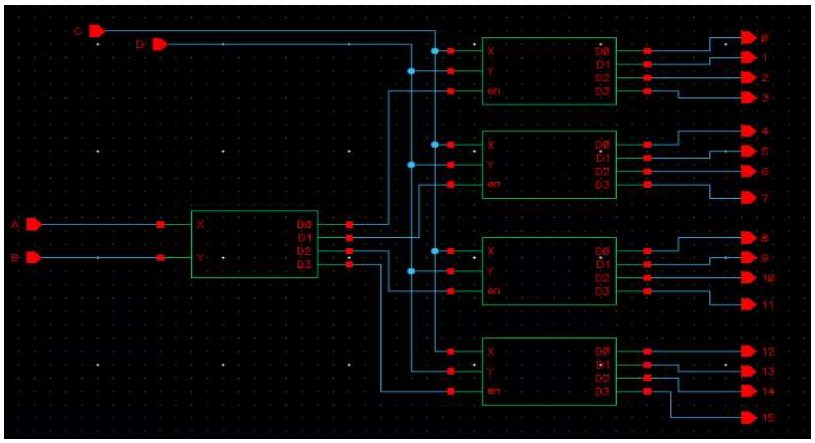


Fig 2. c) 4 to 16 decoder

ii. Precharge circuit:

One pre charging circuit is connected for every column to pre charge the complementary bit-lines, BIT and BITN, to precharged high (1V) state during inactive state of memory as shown in fig. 3. The signal PRECHARGE is used for this purpose. The precharge circuit is isolated from the bit-lines during the memory write and read operation.

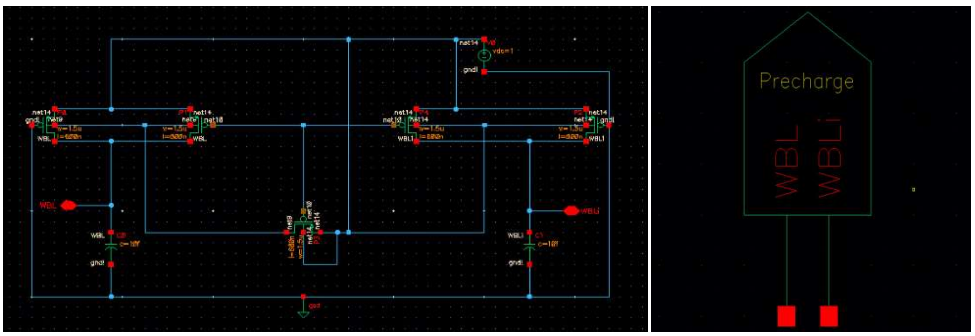


Fig 3) precharge circuit & symbol

iii. A single 8T-SRAM cell:

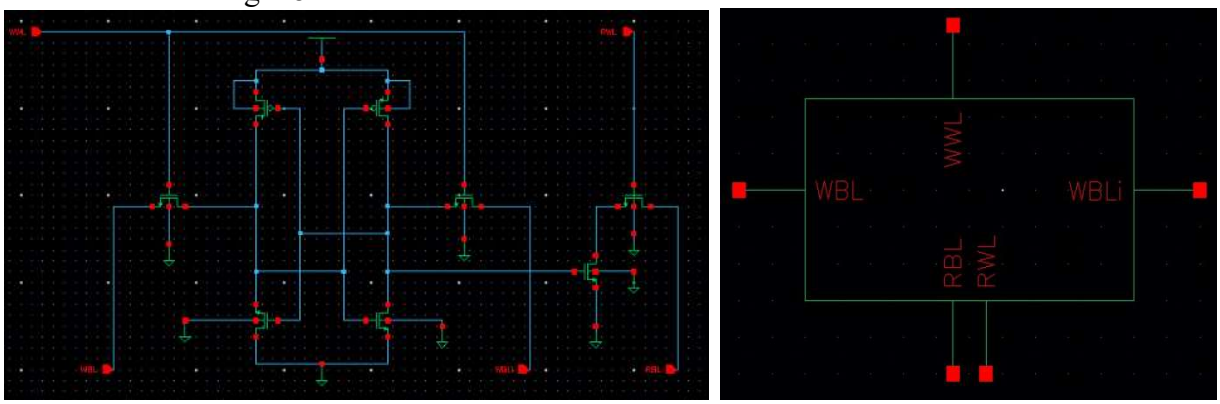


Fig 4) 8T SRAM cell & symbol

The 8T SRAM cell consists of two cross-coupled inverters made up of transistors M1, M3 and M2, M4. The transistors M5, M6 are access transistors. The two additional NMOS transistors M7 and M8, one each in pull down path of cross coupled inverters are used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node Q holds the stored value while other node QN holds its complement. The two complementary bit lines are used to improve speed of write and read operations. The 8T SRAM cell is shown in Fig. 4. The SRAM cell is symmetric and hence M1=M2, M3=M4, M5=M6, and M7=M8.

Write Operation

Write '0' Operation: Writing '0', the bit line has to give zero volts and VDD to the bit line (BLbar). And write word line is asserted which makes both the transistors M3 and M4 ON. Hence the value in the bit line is stored at Q. Hence '0' is stored at Q.

Write '1' Operation: Likewise writing '1' is also carried in the likely same. The bit line has to give a value VDD and bit line bar is given a value 0 volts. As WWL is enabled for write operation, the values in bit lines are store at respective nodes that is at Q will have value logical '1' and logical '0' at Qbar. There is no change in the write operation when compared with the basic SRAM operation.

Read Operation

The read operation is initiated by pre-charging the read bit line to VDD which is required in the conventional one.

Read '0' Operation Read word line (RWL) drives the access transistor M5 ON. If the value stored at Q is '0' then transistor M6 will be ON and RBL is connected to ground directly through M5&M6 transistors discharges. This implies that the value stored at Q in the SRAM is zero.

Read '1' Operation If the value stored at Q is '1', due to M6 transistor will be OFF and there is no discharge path for RBL, and the value in RBL is VDD which shows that value stored at Q is '1'. The circuit diagram of 8T SRAM.

Holding State

The cross-coupled inverters can hold their state as long as power is supplied to the SRAM cell. The feedback loop formed by the inverters helps in retaining the stored data. The stability of the stored state is influenced by various factors, including the size of transistors, technology parameters, and environmental conditions.

iv. 256 bit SRAM:

Combining all the circuits viz, 256 bit 8T SRAM cells, address decoder the precharge circuitry, data write circuitry, 16x16 SRAM array is designed in 65nm technology. The complete setup for data write and read for memory array system is shown in Fig 5. This block diagram shows all the different peripheral circuits combined with the static RAM cells, to form a complete working SRAM 8 x 8 array for write and read operation. Fig. 5 shows the SRAM memory with all input signals; precharge, write enable, , 16 word lines and 16 input data bits. The 16x16 array for SRAM system is implemented using 256, 8T cells.

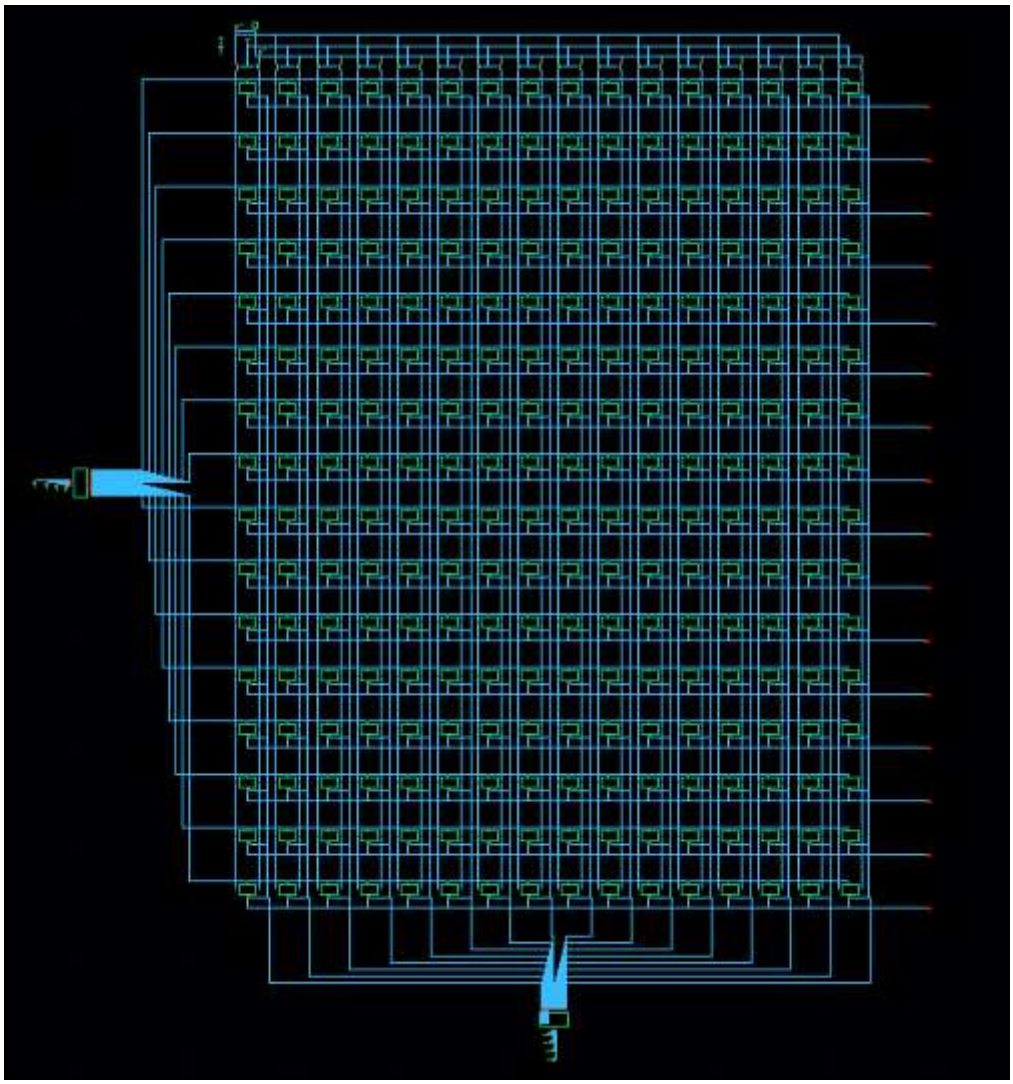


Fig 5) 256 bit 8T SRAM Array

D. Layouts of all Components

a) 2 is to 4 decoder without enable (Fig. 6a)
b) 2 is to 4 decoder with enable (Fig. 6b)
c) 4 is to 16 Decoder (Fig. 6c)
d) Single 8T-SRAM Cell (Fig. 6d)
e) 256 bit SRAM Array (Fig. 6e)

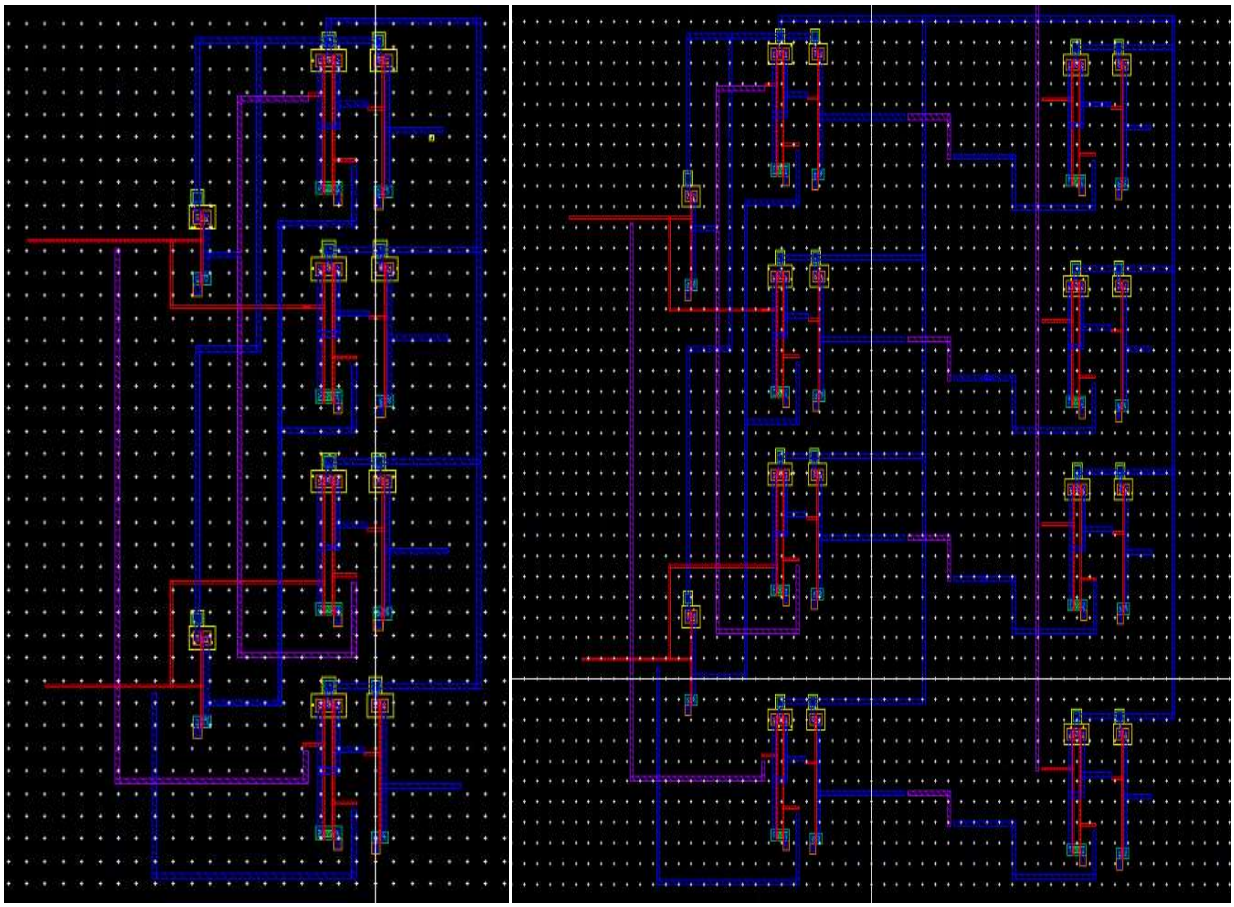


Fig 6a & 6b) 2 to 4 Decoder (with and without enable)

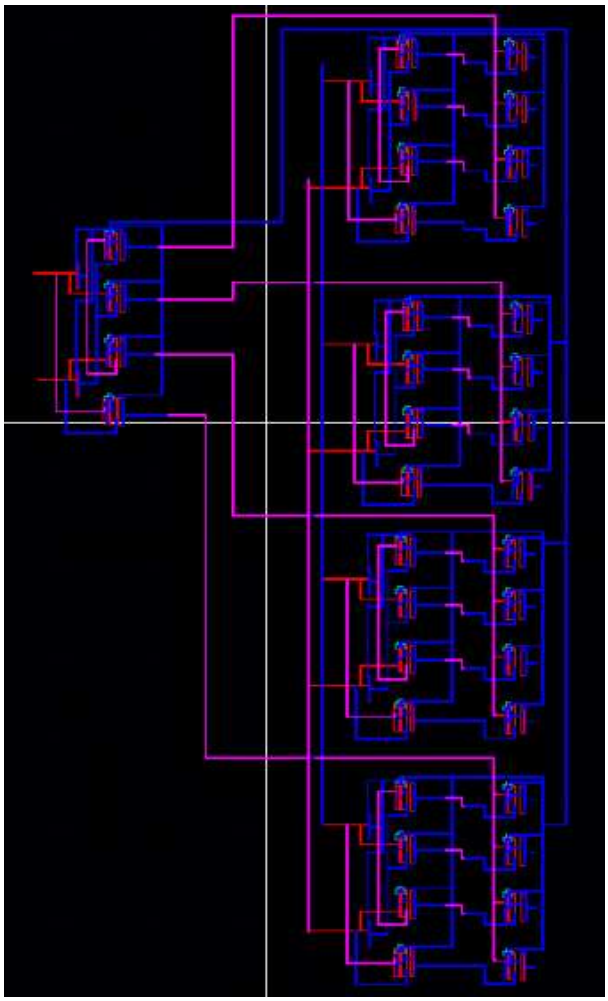


Fig 6c) 4 to 16 Decoder

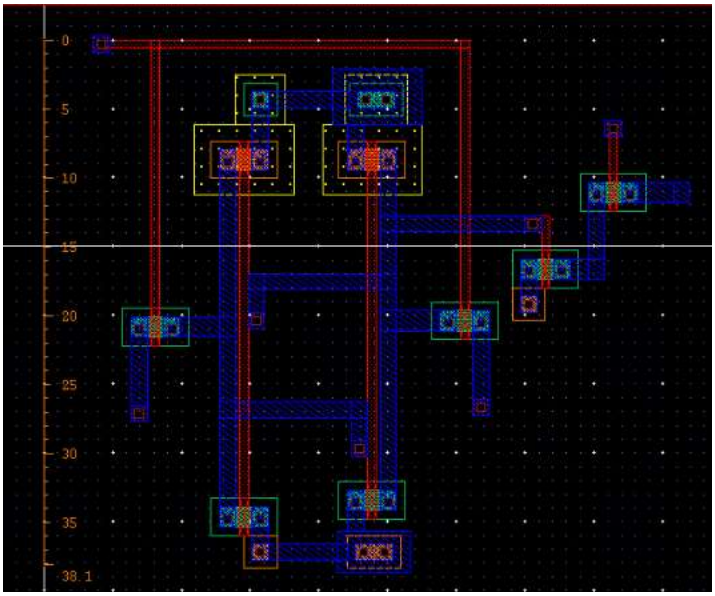


Fig 6d) Single 8T SRAM Cell

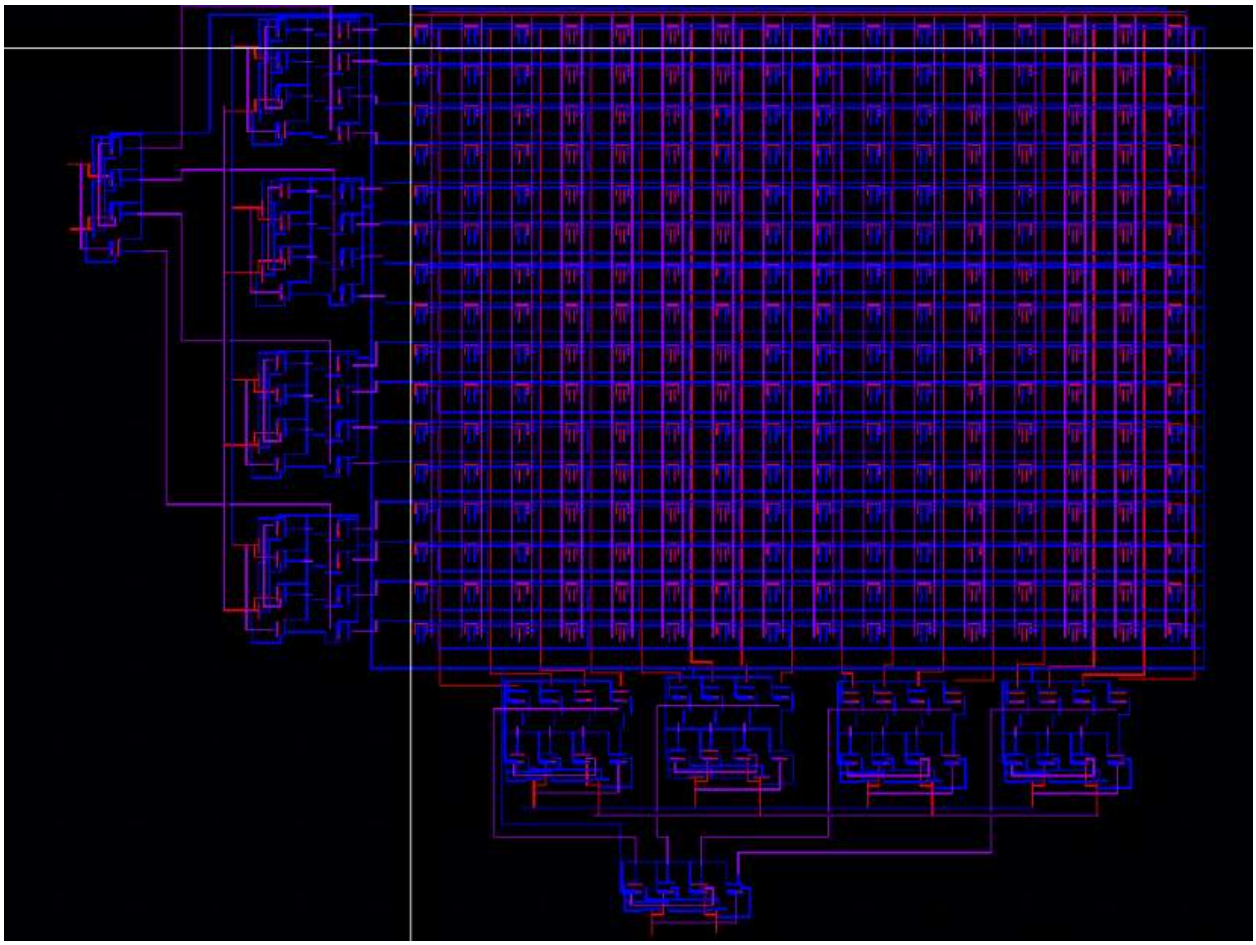


Fig 6e) 256 bit SRAM Memory Array

E. Extracted Parasitic view

I. 2 is to 4 decoder without enable (Fig. 7a)
II. 2 is to 4 decoder with enable (Fig. 7b)
III. 4 is to 16 Decoder (Fig. 7c)
IV. Single 8T-SRAM Cell (Fig. 7d)
V. 256 bit SRAM Array (Fig. 7e)

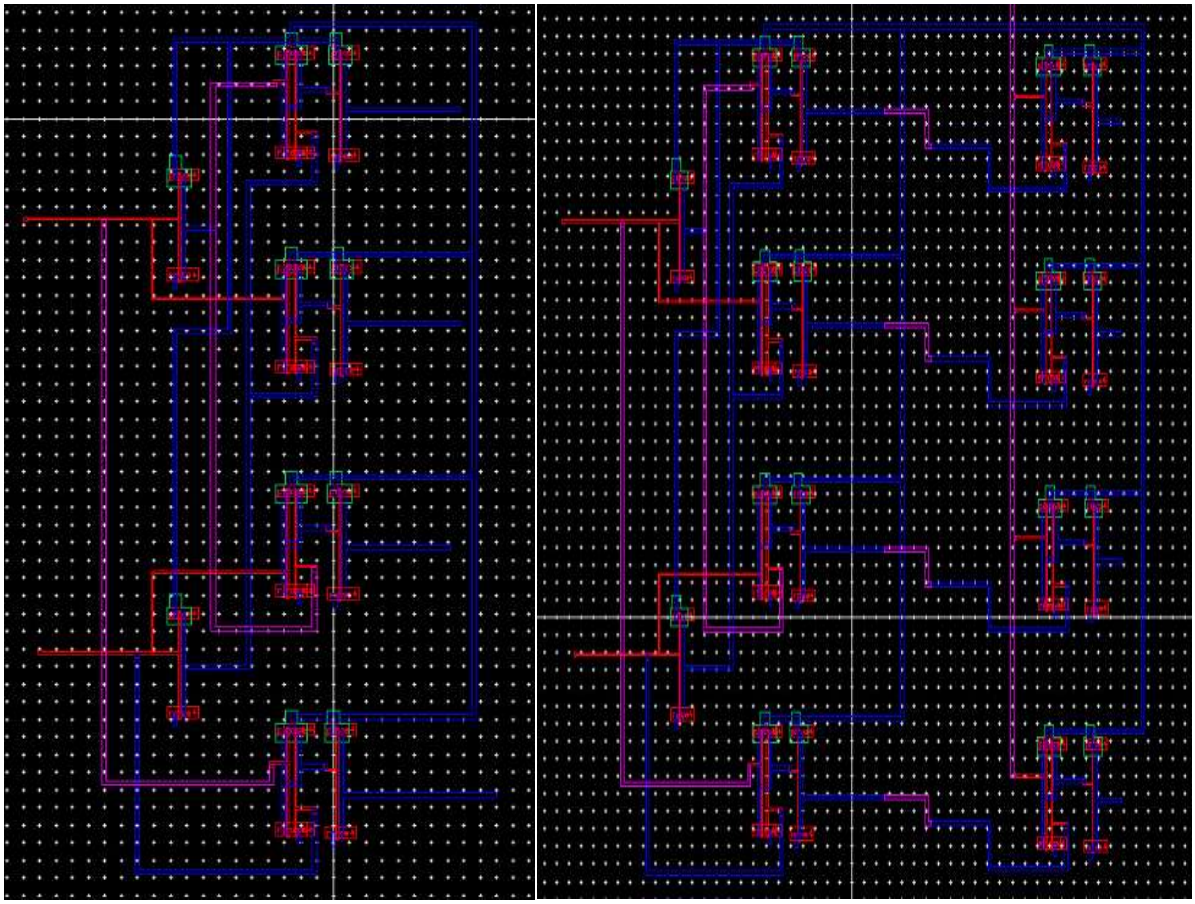


Fig 7a & 7b) 2 to 4 Decoder (with and without enable)

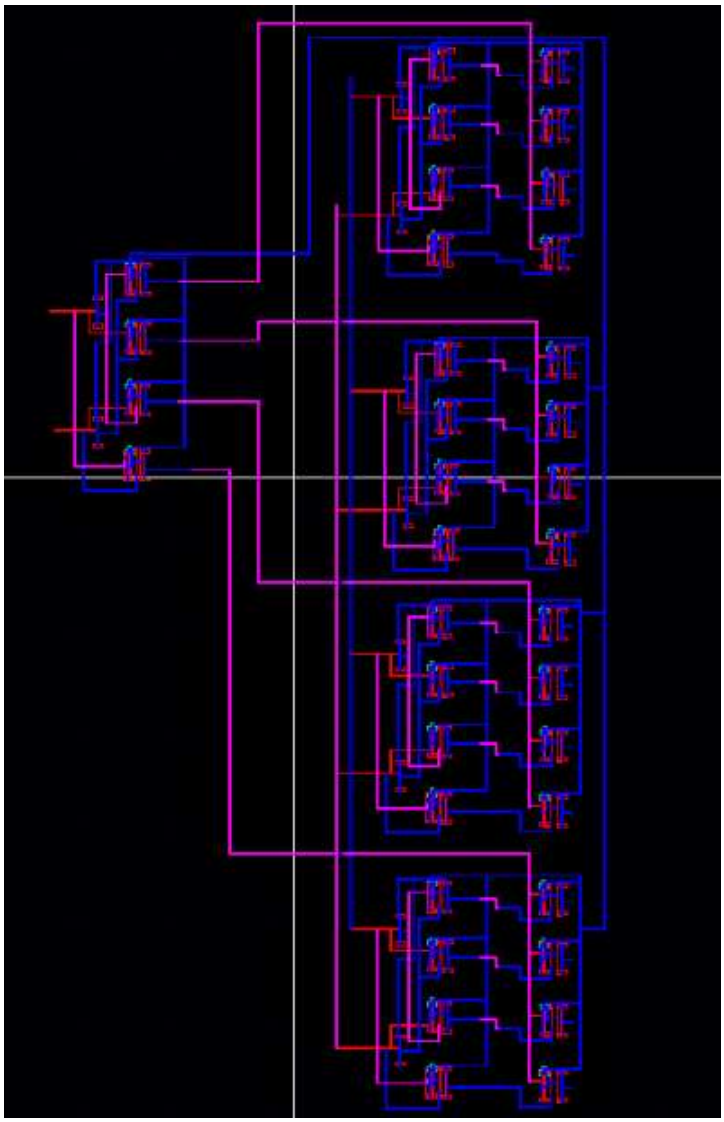


Fig 7c) 4 to 16 Decoder

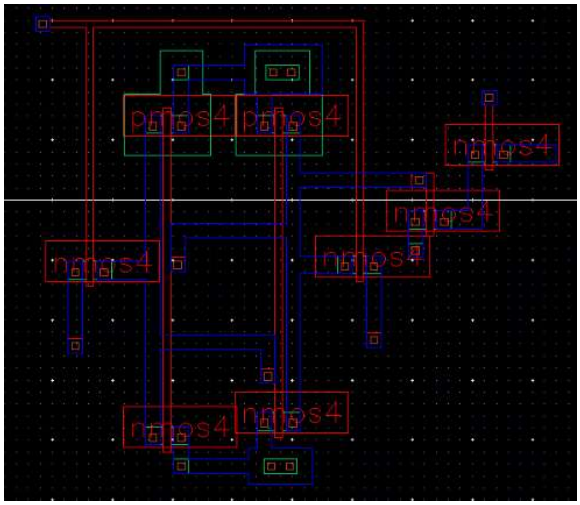


Fig 7d) Single 8T SRAM Cell

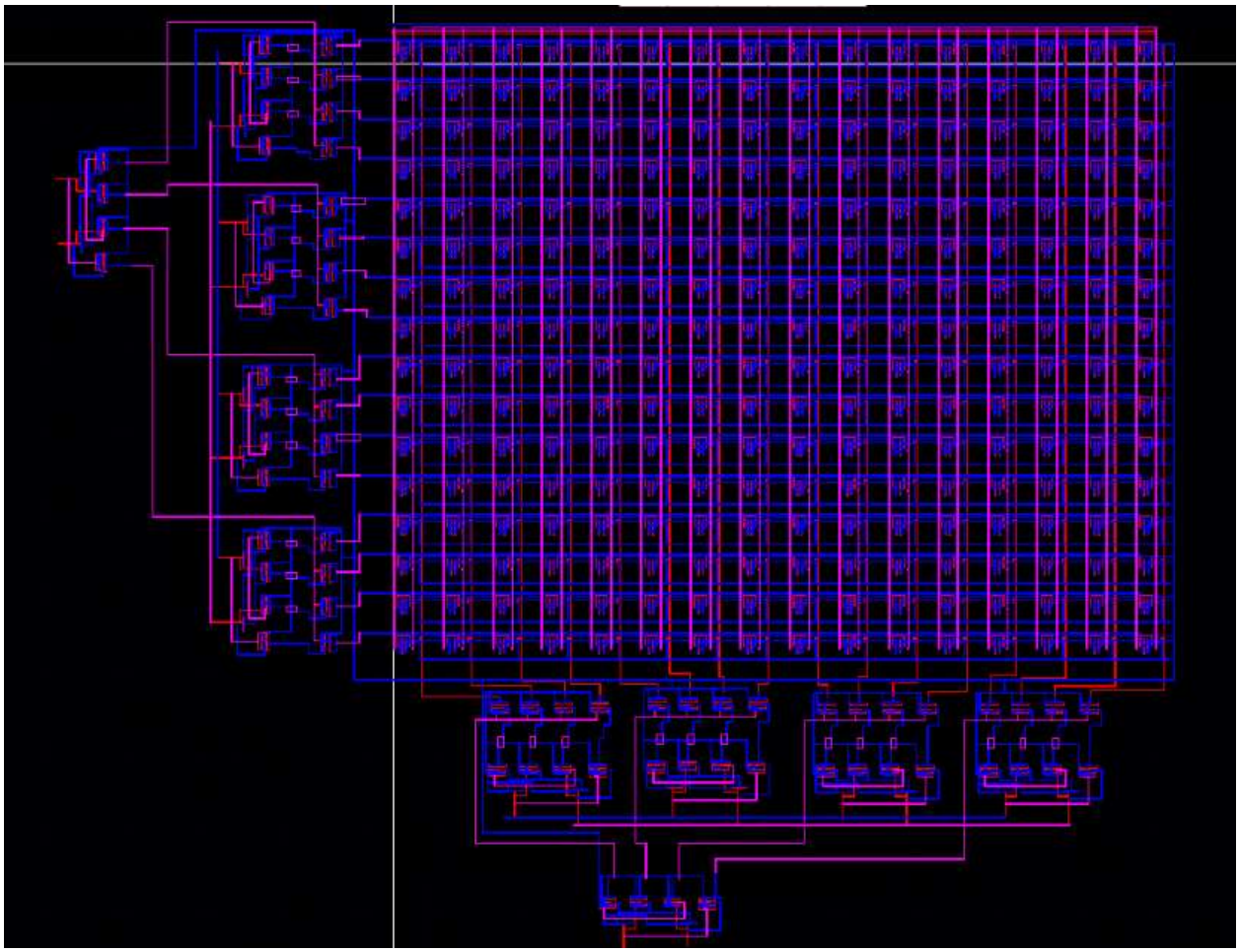


Fig 7e) 256 bit SRAM Memory Array

F. Simulation and Verification

1. 2 is to 4 decoder without enable (Fig. 8a)
2. 2 is to 4 decoder with enable (Fig. 8b)
3. 4 is to 16 Decoder (Fig. 8c)
4. Logic 0 & Logic 1 working for Single 8T-SRAM Cell (Fig. 8d)
5. 256 bit SRAM Array working for Logic 1 (Fig. 8e)

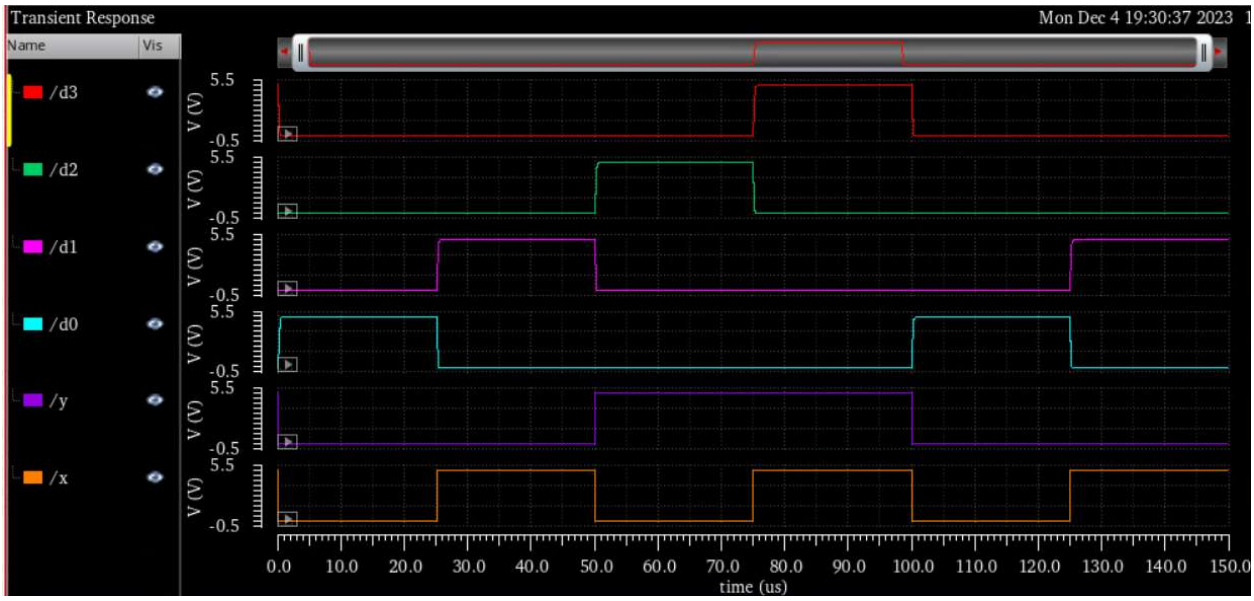


Fig 8a) 2 to 4 Decoder (without enable)

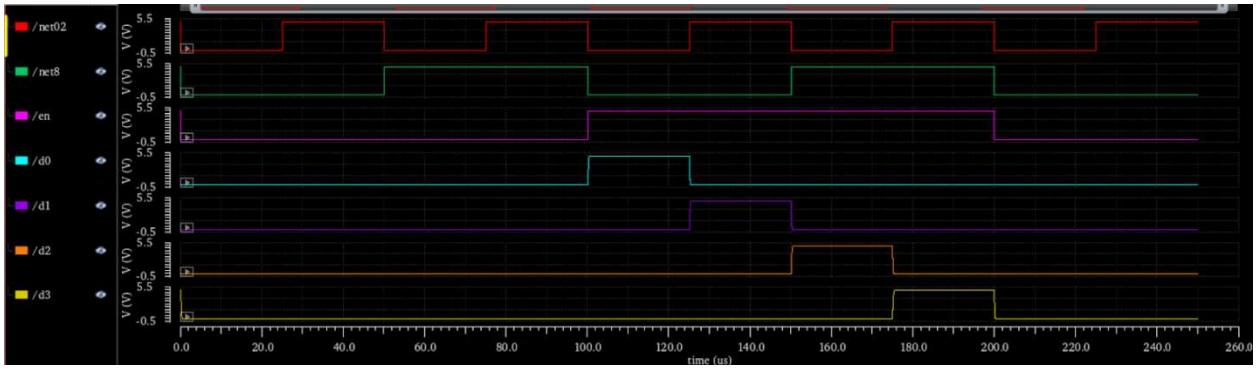


Fig 8b) 2 to 4 Decoder (with enable)

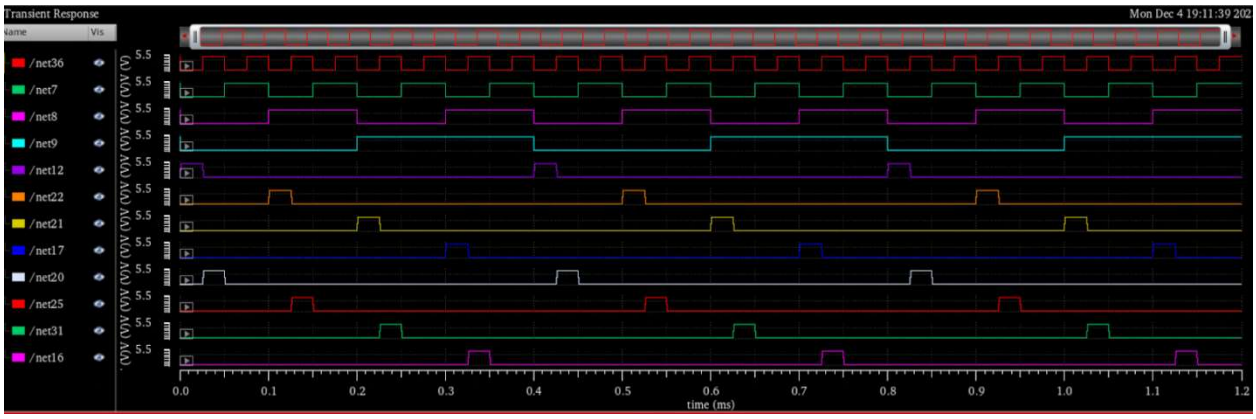


Fig 8c) 4 to 16 Decoder

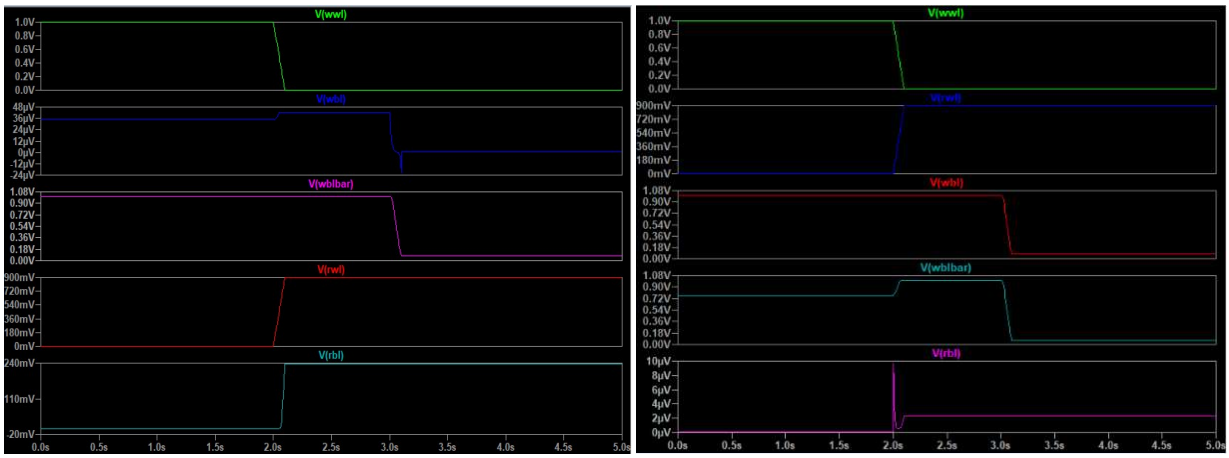


Fig 8d) Logic 1 & Logic 0 working of Single 8T SRAM Cell

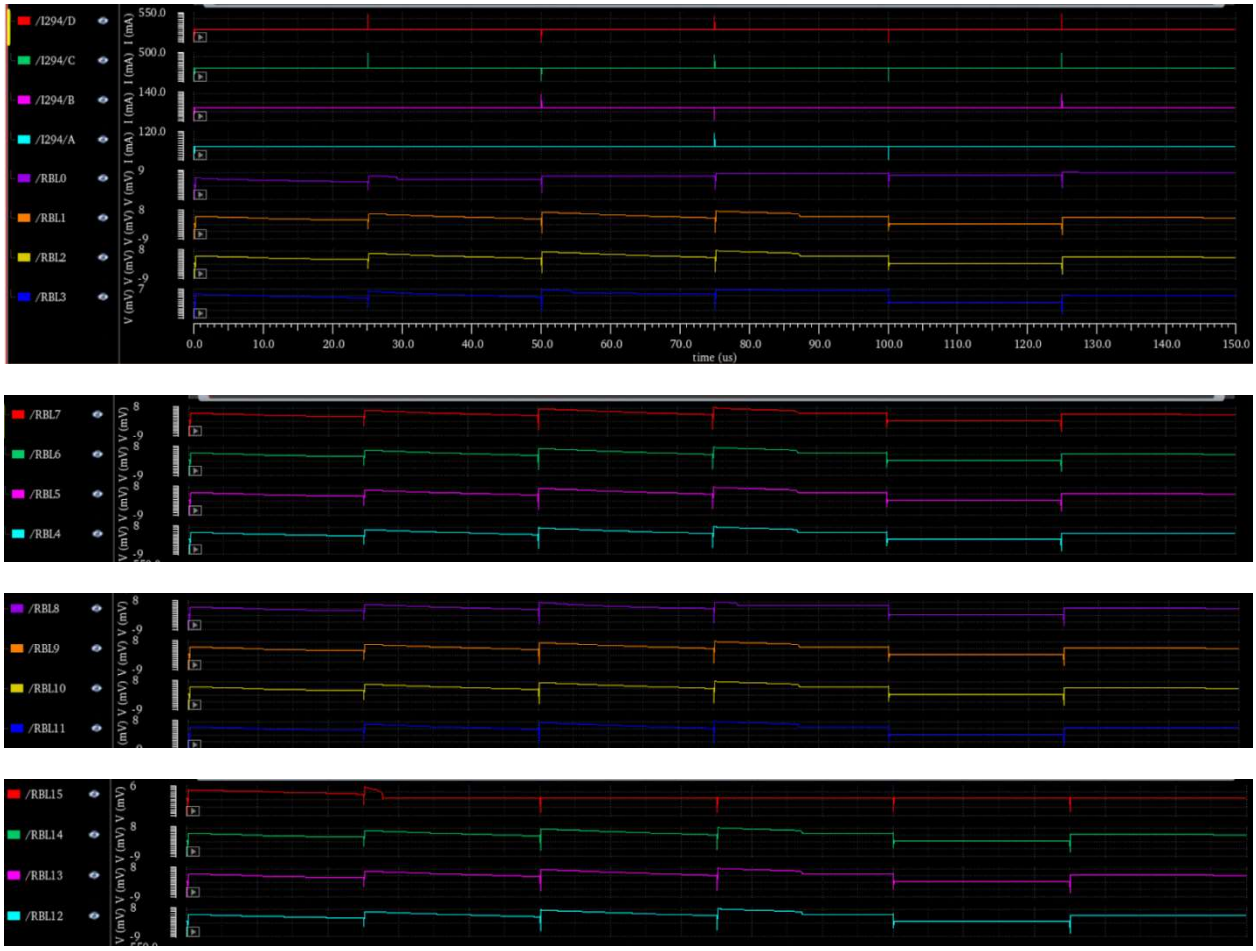
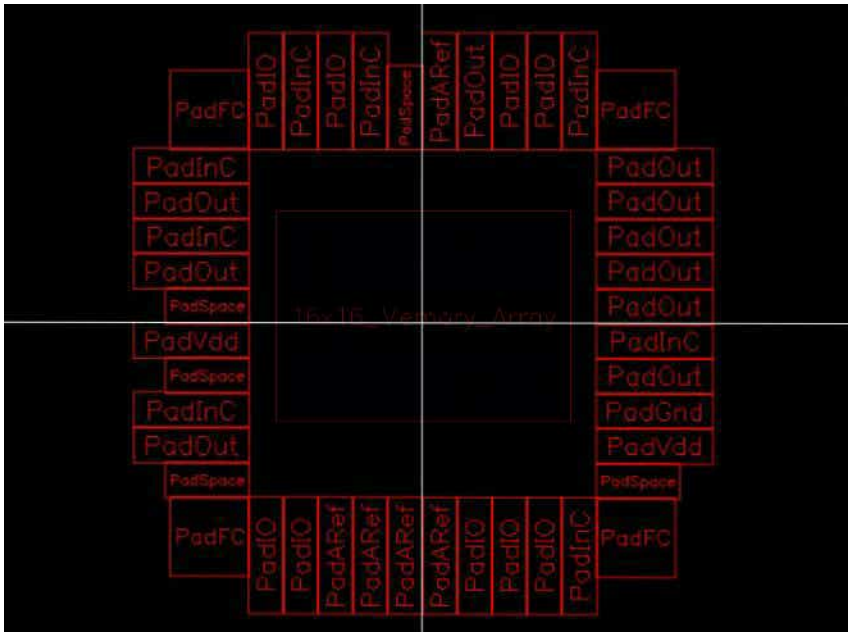
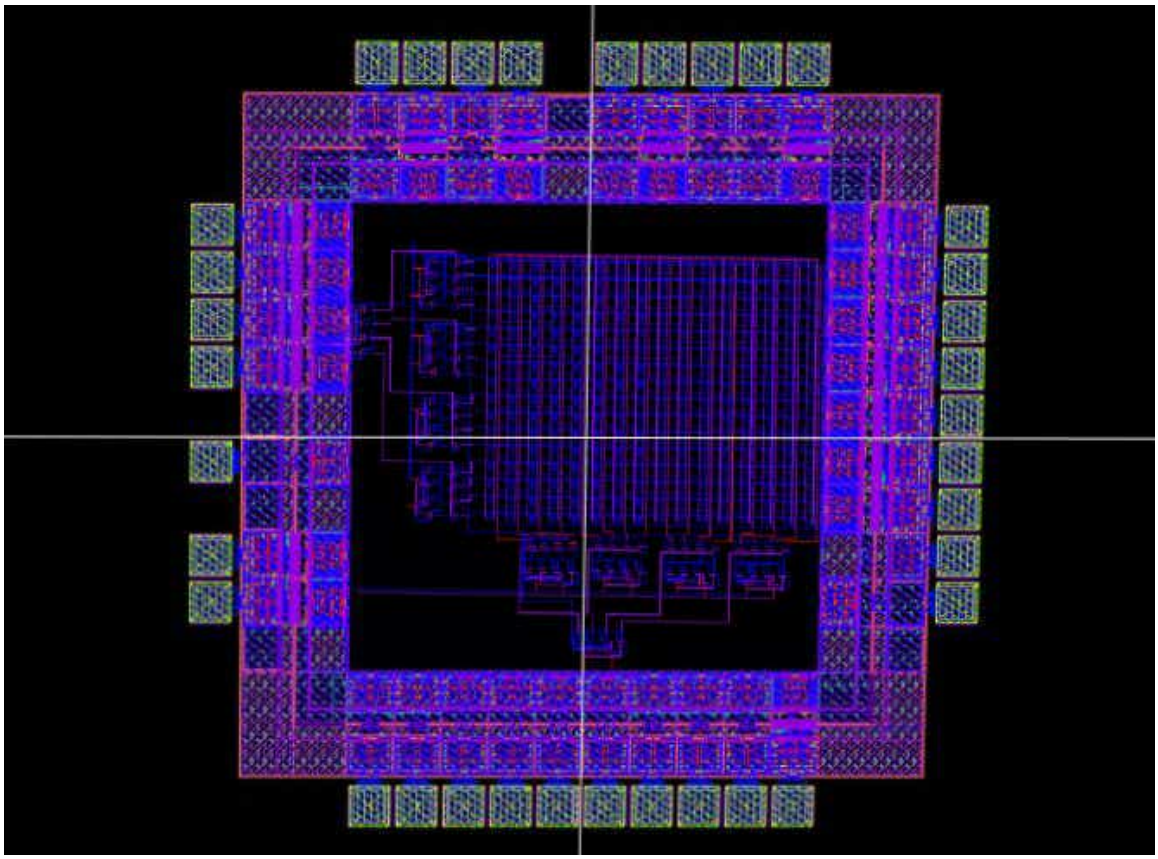


Fig 8e) 256 bit SRAM Memory Array working for Logic 1

G. Padded Frame view





H. Spec Data

Parameter	Value
1. Technology	65nm
2. Supply voltage (Vdd)	1V
3. Operative Freq (f)[theor]	1.5 GHz
4. Power Consumption (P)	110.72uW
5. Area	896.7um

Pins

Input:

4 bit WWL Input A0 A1 A2 A3

4 bit RWL Input B0 B1 B2 B3

Output:

RBL Outputs RBL0 ---> RBL15

I. Conclusion

The presented work introduces the design and the layout of a 16x16 SRAM array with a 4-to-16 decoder that is built using the 65 nm CMOS technology and operates at a power supply of 1V. The total area of the layout is 896.7 µm. Many improvements can be done on this system in future work, like increasing the storage capacity and operating at higher clk frequencies. The system can also be expanded by including sense amplifiers to the bit line and its compliment, which is useful when the capacitance on the bit lines increase from adding more rows and the voltage read from the SRAM cell, is weak.

References:

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